Fastwel

PC/104

DIC324

PC104 Plus Digital I/O Module with Galvanic Isolation

User Manual

IMES.421459.114UM

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Version 1.3

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1.0	Initial version	February 2017
1.1	Paragraphs 3.1.4, 3.1.6, 3.2.3 were changed; in paragraph 1.1 packaged weight was added.	July 2017
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Ownership Rights

Notation and Conventions

Warning, high voltage!

This sign and inscription warn you about the dangers associated with electric discharges (> 60 V) at the time you touch the device or its parts. Noncompliance with the safety precautions, mentioned or prescribed by the rules could endanger your life or health, or lead to product damages. We also recommend you to familiarize with the below subsection dedicated to the high voltage safe handling rules.

Warning!
ESD Sensitive Device!

This symbol draws your attention to the information related to electro static sensitivity of your product and its components. To keep product safety and operability it is necessary to handle it with care and follow the ESD safety directions.

Warning! Hot surface!

This sign marks warnings about hot surfaces. The surface of the heatsink and some components can get very hot during operation. Take due care when handling, avoid touching hot surfaces!

Warning!

Information marked by this symbol is essential for human and equipment safety.
Read this information attentively, be watchful.

Note

This symbol and title marks important information to be read attentively for your own benefit.

Safety requirements

This product is designed and tested for the purpose of ensuring compliance with the electric safety requirements. Its design guarantees long-term failsafe operation. Life cycle of the device can be sufficiently reduced due to improper handling during unpacking and installation. Therefore, for your own safety and in order to ensure the proper operation of the device, you should observe the below recommendations.

High Voltage Safe Handling Rules

Warning!

All the works that involve this device should be carried out by the appropriately qualified personnel.

Warning, high voltage!

Before installing the board into the system make sure that the mains supply is switched off. This also applies to the installation of extension boards.

During installation, repairs and maintenance of the device there is a real danger of exposure to electric shock, therefore you should always disconnect the power supply feeding cable from the socket at the time of works. This also applies to the other power supply feeding cables.

Board Handling Regulations

ESD Sensitive Device!

Electronic boards and their components are sensible to static electricity. This is why you should give special attention to handling
with these devices in order to ensure their integrity and working efficiency.

- - Do not leave the board without protective packaging, when it is not operated.
- - When applicable, always operate the board at the workplace equipped with protection against static electricity. If it is impossible, the user should remove a static discharge before touching the device by hand or using tools. The best way to do it is touch a metal part of system enclosure.
- Observing safety precautions are particularly important during the works associated with replacement of extension boards, memory modules, jumpers etc. If the device is equipped with the batteries for supplying power to memory or real-time clock, do not place the board on such conducting surfaces as antistatic pads or mats. They could cause short-circuit and lead to damages of the battery or board's conductive circuits.

General Board Operation Rules

- To keep the warranty, the product should not be altered or revised in any way. Any alterations or improvements not authorized by Fastwel LLC, except for those specified in this document or obtained from the technical support department of Fastwel LLC as a set of instructions for their implementation, cancel the warranty.

- This device should be installed and connected only to the systems, meeting all the necessary technical and climatic requirements. This above is also true to the operating temperature range of a particular version of the board. You should also consider temperature limitations of the board.

- While performing all the required operations for installation and adjustment, please follow the instructions specified only in this document.

- Keep the original package for subsequent storage of the device and transportation in the warranty event. If it is necessary to transport or store the board, please pack it the same way as it was packed upon delivery.

- Exercise special care when unpacking and handling the device. Act in accordance with the instructions given in the above section and paragraph 1

- Transportation, unpacking and storage.

MANUFACTURER'S WARRANTIES

Warranty liabilities

The manufacturer hereby guarantees that the device meets the technical specification requirements.
"Integrated industrial computer in PC104 format" 4013-004-52415667-05TU provided that the Consumer complies with the conditions of usage, transportation, storage, installation and assembly, set by the accompanying documents.

The Manufacturer hereby guarantees that the products supplied thereby are free from defects in workmanship and materials, provided operation and maintenance norms were observed during the currently established warranty period. The Manufacturer's obligation under this warranty is to repair or replace free of charge any defective electronic component being a part of a returned product.

Products that broke down through the Manufacturer's fault during the warranty period will be repaired free of charge. Otherwise the Consumer will be invoiced as per the current labor remuneration rates and expendable materials cost.

Liability limitation right

The Manufacturer shall not be liable for the damage inflicted to the Consumer's property because of the product breakdown in the process of its utilization.

Warranty period

The warranty period for the products made by Fastwel LLC is 36 months since the sale date (unless otherwise provided by the supply contract).

The warranty period for the custom-made products is 60 months since the sale date (unless otherwise provided by the supply contract.

Limitation of warranty obligations

The above warranty obligations shall not be applied:

- To the products (including software), which were repaired or were amended by the employees, that do not represent the manufacturer. Exceptions are the cases where the customer has made repairs or made amendments to the devices in the strict compliance with instructions, preliminary agreed and approved by the manufacturer in writing;
- To the products, broken down due to unacceptable polarity reversal (to the opposite sign) of the power supply, improper operation, transportation, storage, installation, mounting or accident.

Procedure of device returning for repairs

Sequence of activities when returning the products for repairs:

- Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization;
- Attach a failure inspection report with a product to be returned in the form, accepted by the Manufacturer, with a description of the failure circumstances and symptoms;
- Carefully package the product in the antistatic bag and carton box, in which the product had been supplied. Then package the product in a safe container for shipping. Failure to package in antistatic material will VOID all warranties.
- The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer.

1 Introduction

Digital I/O Module with galvanic isolation DIC324 is implemented in PC/104+ standard on the basis of the stack of DIC122 and DIC123 modules. It has 16 channels of isolated digital input channels and 8 channels of isolated digital output. Electrical parameters of the modules are identical to those of the DIC122 and DIC123 modules. The modules use the Field-Programmable Gate Array (FPGA), which makes it possible to change algorithm of processing inputs and outputs without changing the topology.

All the channels are isolated fro the system and from each other.

The channels use either two-wire or single-wire (with common ground) connection. It is possible to connect signals of the "potential-free" contact type with the use of an external (up to 52 V) power supply source.

Load connection: two-wire/single-wire

1.1 Module technical features

System bus:

- 8-bit ISA bus.

Digital input:

- 16 digital input channels;
- Single-wire or two-wire signal connection;
- Input voltages ±3.2 V ... ±52 V.

Digital output:

- 8 digital output channels;
- Single-wire or two-wire signal connection;
- Switching output voltages/currents: 60V/500mA (with a differential load connection).

LED:

- indication of requests (references).

Main features:

- Delay of input signals: 25 μs;
- Changing frequencies over each channel (up to 30 kHz);
- Optical isolation of inputs/outputs between the channels: 500 V;
- Optical isolation of inputs/outputs between an input and the "ground": 1000 V;
- Generation of hardware interrupts by events at inputs;
- Programmable time interval for de-bouncing at inputs (de-bouncing).

Additional features:

- Five separable lines of hardware interrupts IRQx (where x = 3, 4, 5, 6, 7).
- Possibility for development of its proper configurations (firmware) FPGA

Main control capabilities

- Programming interrupts;
- Setting the range of input voltages.

Module power supply:

- from an external DC power-supply with the voltage of + 5V ± 5 %.
- maximum consumption current value of the module is 160 mA (at switch closures in all the channels).

Software compatibility:

- FDOS, FreeDOS, Linux 2.6, Windows XP (Embedded)

Mean Time Between Failures (MTBF):

- no less than 710,000 hours.

Overall dimensions, mm, no more than:

- 100.0 x 96.0 x 24.0

Operation conditions:

- operating temperature range: from -40° C to +85°C
- relative humidity – up to 80 % (no moisture condensation)

Resistance to mechanical effects:

- Sinusoidal vibrations for frequencies from 10 to 500 Hz: with acceleration no more than 5 g;
- Single shocks with duration 11 ms and peak acceleration of no more than 100 g;
- Multiple shocks with duration 6 ms and peak acceleration of no more than 50 g.

Weight in kg, no more than:

- 0.09

Weight of packaged modules, in kg, no more than:

- 0.176

1.2 Versions

Module's versions and their designations at the time of the order (ordering information) are given in the table below 1-1.

Table 1-1: ORDERING INFORMATON

Name	Conventional designation	Ordering designation	Note
Digital I/O module with galvanic isolation DIC324	DIC324	DIC324-01	-
		DIC324-01 \Coated	Conformal coating option.

1.3 Module delivery checklist

Delivery checklist for all the module versions is given in the Table 1-2

Table 1-2: Delivery checklist

Ordering designation	-	Description
DIC324-01	IMES.421459.114	DIC324 digital I/O module with galvanic isolation
–	–	-
–	–	Packaging.
–	–	Resistive assembly 470 Ohm, 2 pcs

Table 1-3: Additional accessories

Ordering designation	Description
ACS00001	Cable type FC-20, socket IDC-20/Socket IDC-20, length 600 mm
ACS00003	Cable type FC-34, socket IDC-34/Socket IDC-34, length 600 mm
TIB96401	Terminal board, 20-pins (TB20)
TIB96601	Terminal board, 34-pins (TB34)

1.4 External view and location of components

The below figures will help you identify components, their configuration and functions.

1.4.1 Module external view

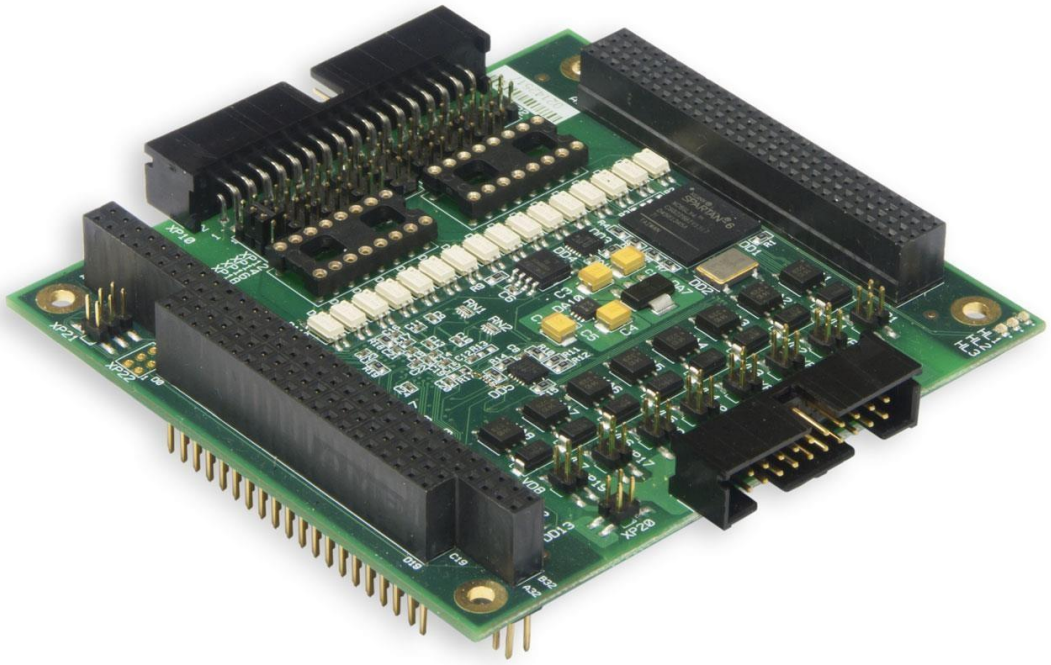


Fig. 1-1: External view of DIC324

Note

External view of module versions could slightly differ from the one shown in the Figures.

1.4.2 Overall and mounting dimensions, location of main components

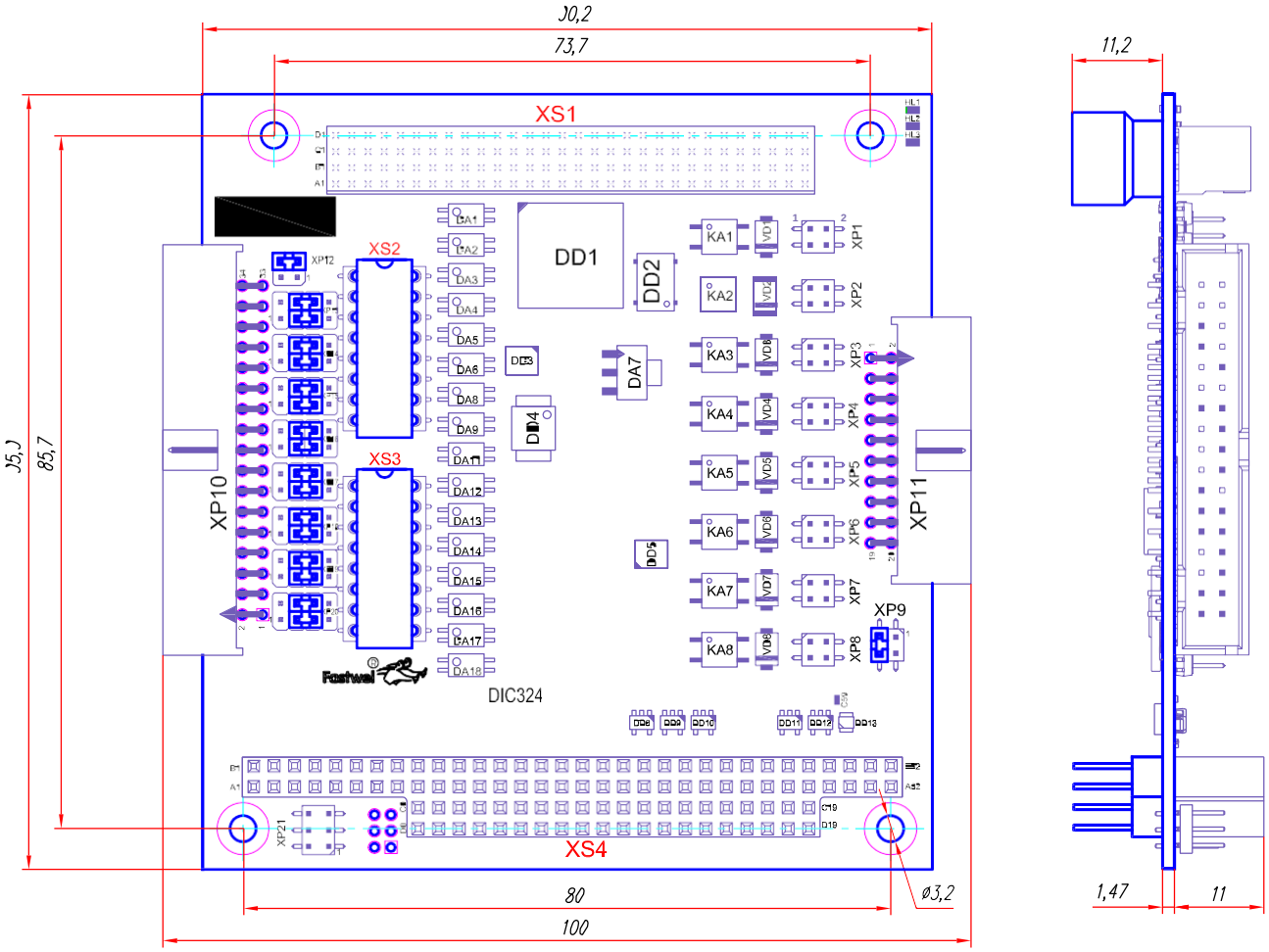


Fig. 1-2: Overall dimensions and location of main components of DIC324

2 Functional description

2.1 Module block diagram

Block diagram of the module is shown in Fig. 2-1

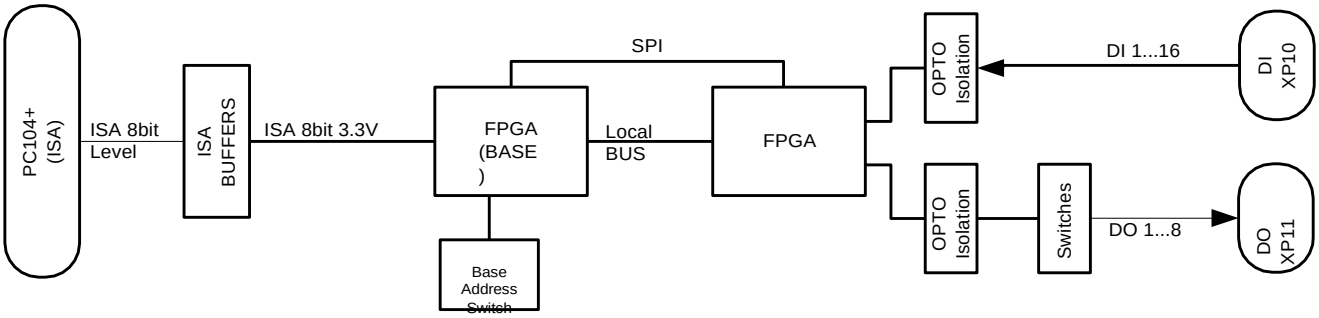


Fig. 2-1: Block diagram of DIC324

The module's block diagram contains main functional elements:

- **FPGA (BASE)** – System FPGA Xilinx XC6SLX4-2CSG225I;
- **FPGA1** – User FPGA Xilinx XC6SLX4-2CSG225I;
- **PC104+ (ISA)** – edge connector of 8-bit ISA bus;
- **Digital_Inputs (DI)** – digital input connector (XP10);
- **Digital_Outputs (DO)** – digital output connector (XP11);
- **OPTO Isolation** – are output buffers with galvanic isolation;
- **Switches** – are the switches for load commutating.

2.2 Location of main components

Location of the main components, connectors that correspond to them, as well as commutator bars of the module is demonstrated in Figure 1-2 (Top view) and Figure 2-2 (Bottom view).

Designations of connectors, switches and jumpers comply with designations on the module's board:

- XP10, XP11 - connectors of module's external connections;
- XP21 - additional process connector for FPGA (Base) microchip programming;
- SA1 - switch of the base address setting;
- XP1-XP8 - installation jumpers of the type of output signals connection in digital output channels;
- XP13-XP20 - installation jumpers of the type of input signals connection in digital input channels;
- HL1 - LED indicator of requests (references) over input/output;

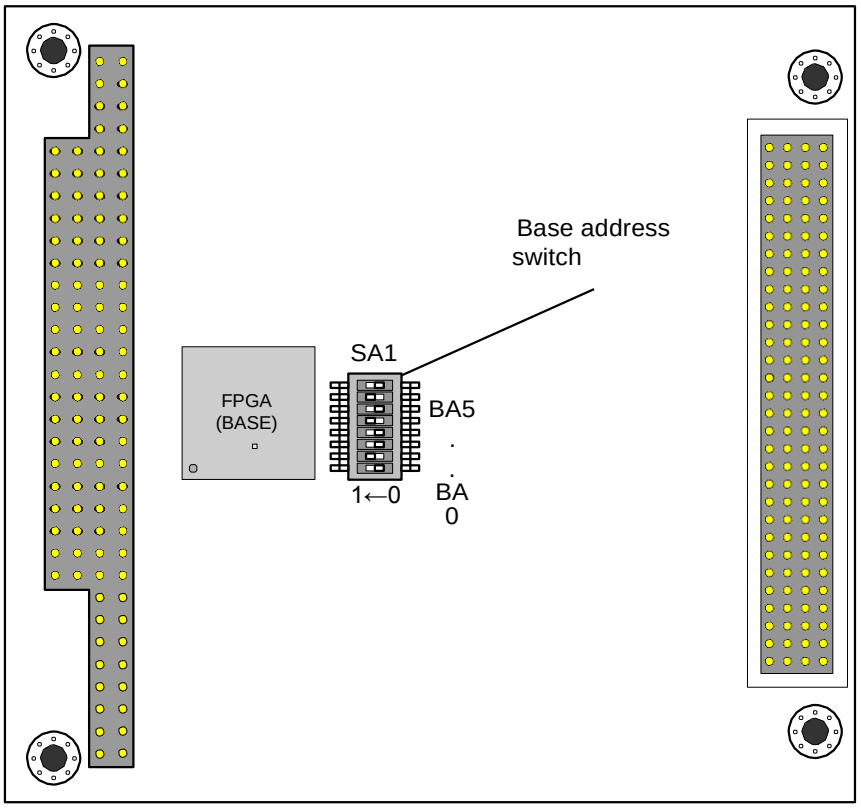


Fig. 2-2: Location of the SA1 base address switch

2.3 Module's functional nodes and interfaces

2.3.1 Base FPGA (BASE)

Base FPGA is a control FPGA of the module. It has implemented: Local Bus generation for communication with the module's node of digital I/O, SPI controller for implementation of in-circuit programming and configuration of this node, as well as module's base address selector and interrupt operating line on ISA bus. As FPGA, Xilinx FPGA of the Spartan 6 (XC6SLX4-2CSG225I) series is used.

2.3.2 System ISA bus

The module is equipped with 8-bit ISA bus

The interface is routed to the XS4 connector. Description of ISA connector contacts (rows A and B) of the module for the connection to the external system ISA bus is shown in the tables below.

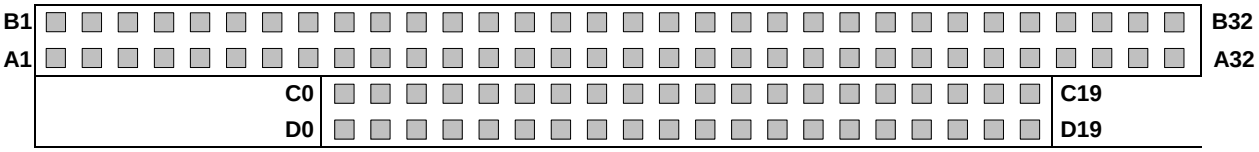
Table 2-1: Identification of ISA bus contacts, row A

Contact	Signal	State	Contact	Signal	State
A1	/IOCHK	–	A17	SA14	Input
A2	SD7	Input / Output	A18	SA13	Input
A3	SD6	Input / Output	A19	SA12	Input
A4	SD5	Input / Output	A20	SA11	Input
A5	SD4	Input / Output	A21	SA10	Input
A6	SD3	Input / Output	A22	SA9	Input
A7	SD2	Input / Output	A23	SA8	Input
A8	SD1	Input / Output	A24	SA7	Input
A9	SD0	Input / Output	A25	SA6	Input
A10	IOCHRDY	Output	A26	SA5	Input
A11	AEN	Input	A27	SA4	Input
A12	SA19	Input	A28	SA3	Input
A13	SA18	Input	A29	SA2	Input
A14	SA17	Input	A30	SA1	Input
A15	SA16	Input	A31	SA0	Input
A16	SA15	Input	A32	GND	Power supply

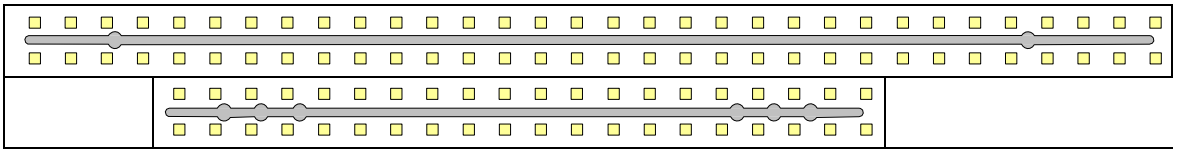
Table 2-2: Identification of ISA bus contacts, row B

Contact	Signal	State	Contact	Signal	State
B1	GND	Power supply	B17	/DACK1	Input
B2	RESET	Input	B18	DRQ1	Output
B3	+5V	Power supply	B19	/REFRESH	Input
B4	IRQ9	Output	B20	BCLK	Input
B5	-5V	Power supply	B21	IRQ7	Output
B6	DRQ2	Output	B22	IRQ6	Output
B7	-12V	Power supply	B23	IRQ5	Output
B8	0WS	Output	B24	IRQ4	Output
B9	+12V	Power supply	B25	IRQ3	Output
B10	GND	Power supply	B26	/DACK2	Input
B11	/SMEMW	Input	B27	TC	Input
B12	/SMEMR	Input	B28	BALE	Input
B13	/IOW	Input	B29	+5V	Power supply
B14	/IOR	Input	B30	OSC	Input
B15	/DACK3	Input	B31	GND	Power supply
B16	DRQ3	Output	B32	GND	Power supply

NOTE: IN TABLE 2-1 AND TABLE 2-2 THE FOLLOWING DESIGNATIONS OF STATES OF CONNECTOR'S SIGNAL CONTACTS HAVE BEEN ACCEPTED: Input – INPUT, "OUT." – OUTPUT, "I / O" – INPUT/OUTPUT (BIDIRECTIONAL), "POWER SUPPLY" – MODULE'S POWER SUPPLY DURING INSTALLATION TO THE RELEVANT PC/104+ CONNECTORS



a)



b)

Fig. 2-3: Numbering of XS4 connector contacts

a) Top view

b) Module's bottom view with organizer installed into the connector

2.3.3 Digital input ports (Digital_Inputs)

Digital input connectors are input buffers with galvanic isolation. Input buffers support differential input and ensure galvanic isolation up to 500 V per channel and 1000 V between the channel and "ground" (GND) of the module.

In terms of structure, the modules are represented by IDC XP10 connector.

External view and designation of digital input connectors' (XP10) contacts are shown in Figure 2-4 and tables below.

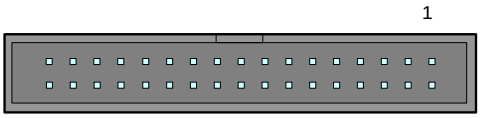


Fig. 2-4: Digital input connector

Table 2.3: XP10 connector contacts

Contact	Name	Contact	Name
1	+DI0	18	-DI8
2	-DI0	19	+DI9
3	+DI1	20	-DI9
4	-DI1	21	+DI10
5	+DI2	22	-DI10
6	-DI2	23	+DI11
7	+DI3	24	-DI11
8	-DI3	25	+DI12
9	+DI4	26	-DI12
10	-DI4	27	+DI13
11	+DI5	28	-DI13
12	-DI5	29	+DI14
13	+DI6	30	-DI14
14	-DI6	31	+DI15
15	+DI7	32	-DI15
16	-DI7	33	**-Vin (+*Vin*)***
17	+DI8	34	-Vin

* - is installed to XP12 by the jumper. **"-*VIN*" : XP12[3-4]; "+*VIN*": XP12[1-2]**

2.3.4 Input channel diagram

The wiring diagram of input channel (number x) is shown in Figure 2-5. Using a limiting resistor, input signal is transferred to optron. Jumpers XP13-XP20 enable to change the connection type (two-wire, single-wire, potential-free contact). Output signal from optron is received at FPGA matrix input.

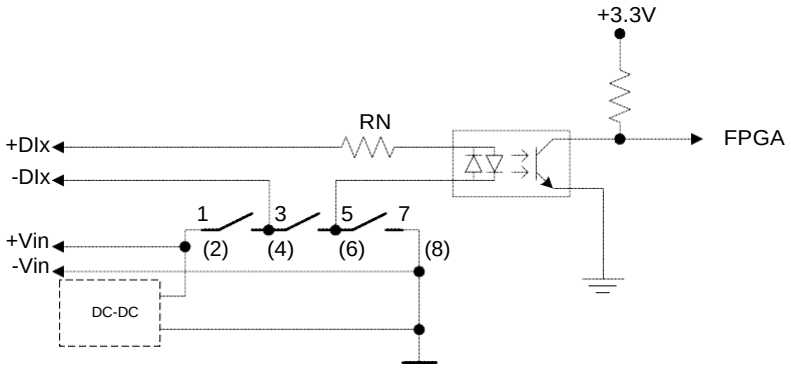


Fig. 2-5: Diagram of DIC324 input channel

For galvanic isolation, the following optrons are used: TCMT-1600 (Vishay). Input channel implementation, similar to the one of DIC112/DIC122.

Switches (jumpers):

- Selection of input signal connection mode. Jumpers (XP13-XP20) of changing the signal connection type make it possible to set the type of input signal: differential, single-wire, potential-free contact

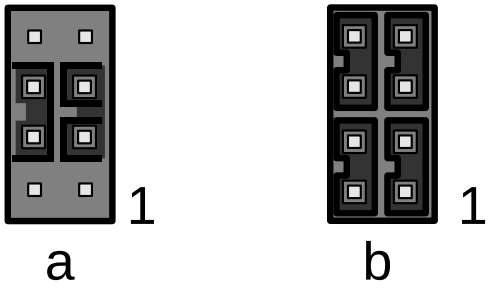


Fig. 2-6: Connection type jumpers

a) – differential (set at the time of delivery); b) – single-wire.

- Selection of contact connection 33 connectors XP10: +Vin or –Vin, is set using the jumper at XP12 connector.

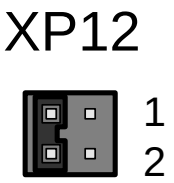


Fig. 2-7: XP12 jumper

(Set to XP12[3-4] at the time of delivery)

2.3.5 Resistive assemblies

Assemblies of RN1, RN2 resistors are used for setting trigger threshold per each group of eight input channels. The delivery contains two types of resistor assemblies with the rate: 470 Ω, 2.2 kΩ. The assemblies could be installed to the relevant pads XS2, XS3.

2.3.6 Digital output port (Digital_Outputs)

In terms of its structure, digital input port is represented by IDC XP11 connector. It is made as a solid-state relay with galvanic isolation.

External view and designations of digital output connector's (XP11) contacts are shown in the figures and in the table below.

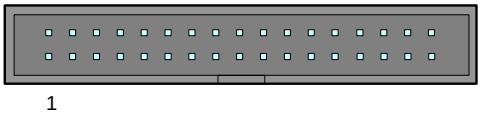


Fig. 2-8: Digital output connector

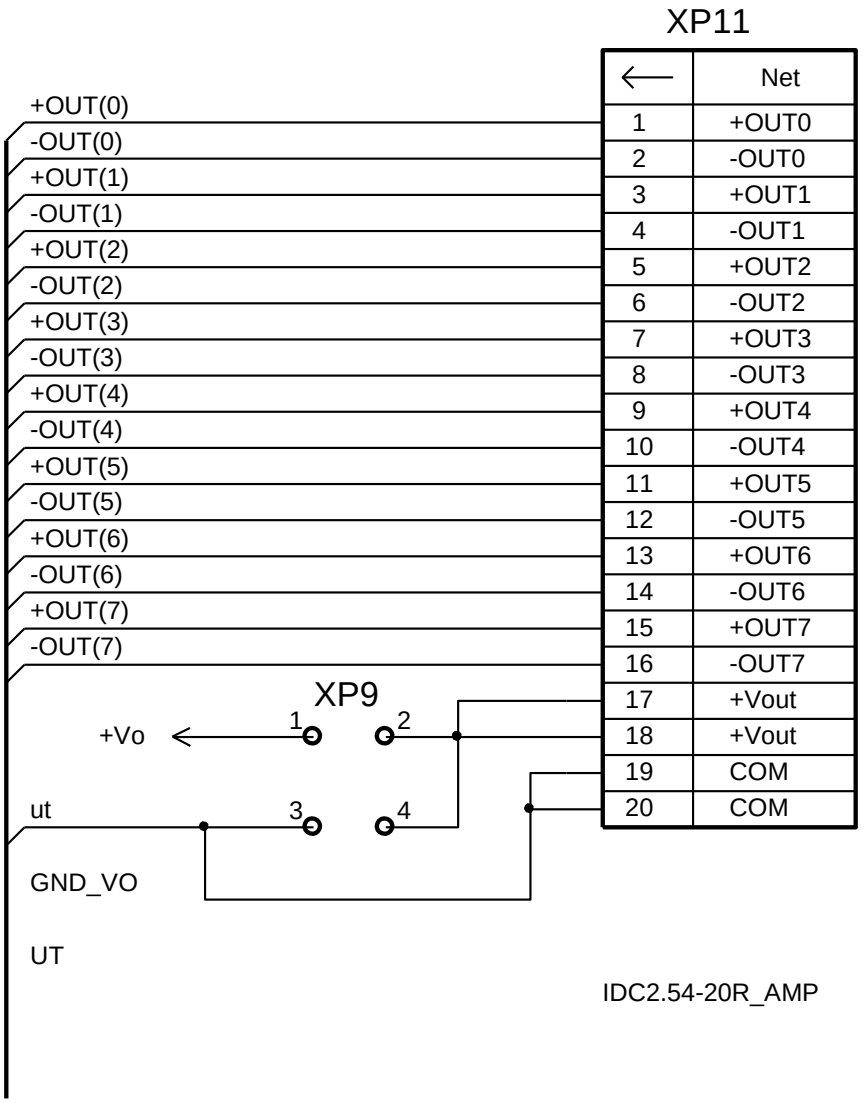


Fig. 2-9: Diagram of the connector's ports' outputs

Table 2-4: Table of XP11 connector contacts

Contact	Name
1	+OUT0
2	-OUT0
3	+OUT1
4	-OUT1
5	+OUT2
6	-OUT2
7	+OUT3
8	-OUT3
9	+OUT4
10	-OUT4
11	+OUT5
12	-OUT5
13	+OUT6
14	-OUT6
15	+OUT7
16	-OUT7
17	**GND_VOUT (+Vout)***
18	**GND_VOUT (+Vout)**
19	COM
20	COM

* - is installed to XP9 by the jumper. **“*GND_VOUT*” : XP9[3-4]; “+Vout”: XP9[1-2]**

2.3.7 Solid-state relays

The module is equipped with eight solid-state relays (KA), which are intended for control of outputs of constant voltage up to 60 V and current up to 1 A of digital output port. The also ensure galvanic isolation up to 500 V per channel, and 1000 V – between a channel and "ground" (GND) of the module.

The wiring diagram of output channel is shown in Figure 2-10.

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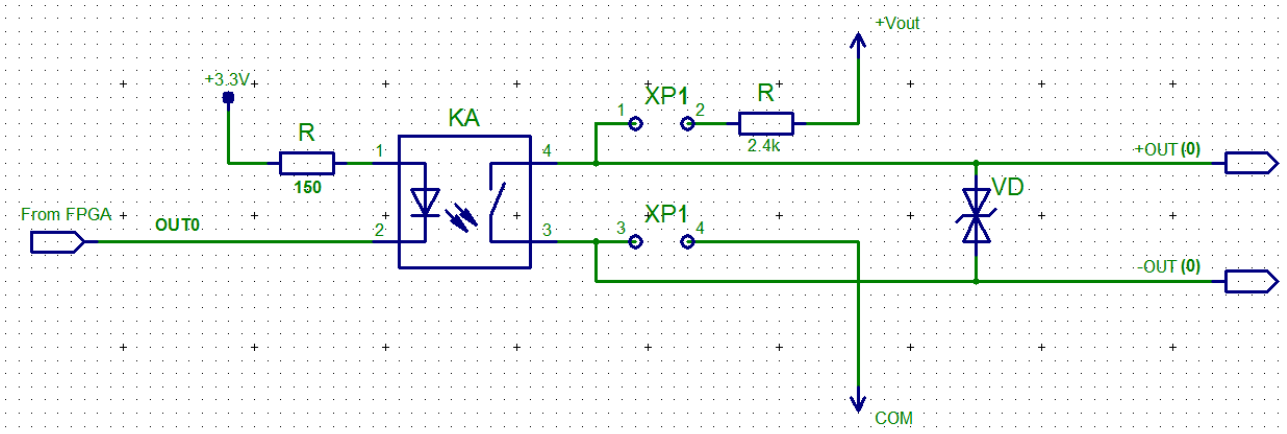


Fig. 2-10: Input channel 1 diagram

2.3.8 Base address switch

Figure 2-11 shows the switch of base address and module addressing mode setting (SA1) and location of its separate engines at the time of module's delivery.

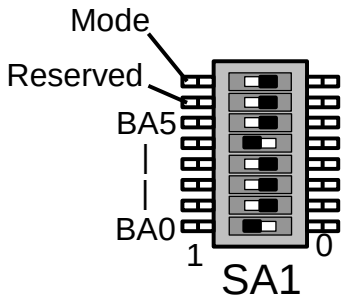


Fig. 2-11: SA1 base address setting switch

2.3.9 LEDs

The module is equipped with an orange LED HL1, which is intended for indication of requests (references) to the module.

2.3.10 Module power supply

Module's power supply (over system bus, contacts: B3, B29 – "+5 V" and B1, B31 – "GND") should be fed from an external DC power supply source with a voltage of + 5 V ± 5 %.

Maximum consumption current value of the module is 160 mA (at switch closures in all the channels).

3 Module use

3.1 Module preparation for use

3.1.1 General requirements

When handling DIC324, you should strictly follow the below safety requirements. Manufacturer shall not be liable for any damages, arising out as a result of non-observance of such requirements:

- all the installation and preparation works on the module, any additional external devices (including installation, removal and connection) should be performed only when the module's power supply is off and when there are no voltages at connectors of additional external devices to be connected to the module;
- all possible replacements of module's elements and maintenance works should be performed only after the power supply cable of the module and any additional external devices is disconnected;
- module's installation to PC/104-plus connectors should be carried out in strict adherence to orientation instructions.

ATTENTION: **IN ORDER TO PREVENT MODULE BREAKDOWNS IT IS REQUIRED TO STRICTLY COMPLY WITH THE GENERAL REQUIREMENTS WHEN PREPARING THE MODULE FOR USE!**

3.1.2 Electrostatic safety requirements

All installation and preparation works, replacement of elements and module maintenance should be carried out only with the use of special tools and technical accessories (e.g. electrostatic discharge straps etc.), free of electrostatic discharge and magnetization properties.

3.1.3 External inspection

Prior to module operation, an external inspection of consumer packaging and module's static protective packaging should be performed, make sure there are no mechanical damages to specific elements and module as a whole.

NOTE: If any of the components from the delivery checklist is lacking or has external mechanical damages, please contact the official distributor that sold you this module.

NOTE: Retain the original antistatic and consumer packaging of the module till the end of the guarantee service life period.

3.1.4 Readiness check

Prior to working with the module, you should:

- become familiar with the module's structure and this User Manual;
- check that the base address switch (p.3.2.1) and jumpers (p. 3.2.2, 3.2.4) have been set properly;
- install the- DIC324 I/O Module onto the CPU module using the PC/104+ connectors, in compliance with the installation instructions (p.3.1.5), general requirements (p.3.1.1) and electrostatic safety requirements (p.3.1.2) when preparing the module for the use;
- connect the necessary additional external devices to module connectors in accordance with the connection type in use for input digital signals and with a model list (p. 3.1.7);
- switch on the power supply.

NOTE: **LOCATION OF MAIN COMPONENTS, CONNECTORS, SWITCHES AND JUMPERS OF THE MODULE IS SHOWN IN FIGURE 1-2**

3.1.5 Installation of DIC324

The Module could be installed into the relevant PC/104-Plus connectors. You can install the modules one above the other in order to get highly-integrated systems.

ATTENTION: **PC/104 AND PC/104-PLUS MODULES ARE INSTALLED AFTER POWER IS TURNED OFF.**

ATTENTION: **WHEN INSTALLING THE PC/104-PLUS MODULES TRY NOT TO BEND OR DEFORM THE BOARD OF DIC324 AND CPU's MODULE. PROPERLY MATCH THE CONTACTS AND USE THE NECESSARY FASTENERS.**

General characteristics of external power supply source and current consumption values (excluding signal currents), required for module's stable operation, are shown in p.2.3.10.

ATTENTION: **NON-COMPLIANCE WITH THE PERMITTED POWER SUPPLY VOLTAGE VALUE COULD LEAD TO MODULE'S BREAKDOWNS OR COULD CAUSE ITS UNSTABLE OPERATION!**

3.1.6 Module's default configuration

The default configuration of the module is made with consideration of initial setting of switches and jumpers to the default state. Setting the switches and jumpers of the module to the default state should be performed under workshop conditions at the quality assurance stage.

Setting the switches and jumpers at the time of delivery is shown in Figure 2-6 and 2-7. Figure

3.1.7 Connection to the module

Additional external devices should be connected to the module only in accordance with the type of connection used for input digital signals (p. 3.2.2) and with the model list of accessories and terminal boards, specified below.

The external devices should have interfaces with the voltage levels from 3.2 to 52 Volts, in this case the relevant voltage range of input digital signals is set by resistor assemblies to the relevant pads XS2, XS3 (p. 3.2.3).

Connection of signal sources to the IDC XP10, XP11 type connectors of the module is carried out using the connection cable ACS00003 (type FC34-60) and cable ACS00001 (type FC20-60) respectively.

For screw-type connection of signal sources to the module terminal boards Fastwel® TIB96601/TIB96401.

3.1.8 Module configuration

Module configuration involves an independent setting of switches and jumpers by the user.

Proper setting of all the groups of switches and jumpers is required for correct and proper installation of the module. General description of setting the switches and jumpers is shown below.

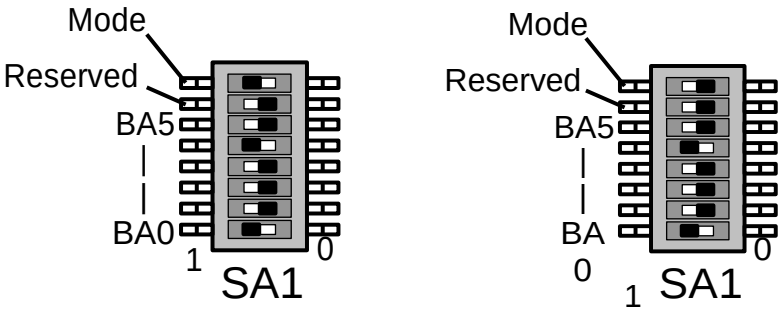
ATTENTION: **IT IS REQUIRED TO MAKE SURE THAT ALL THE GROUPS OF SWITCHES AND JUMPERS PRIOR TO THE FIRST MODULE'S ACTIVATION HAVE BEEN SET PROPERLY!**

3.2 Main control capabilities

The module is controlled using the registers via I/O ports, which designations depend on the type of the diagram loaded (**D11** – basic option) within the FPGA1 matrix.

3.2.1 Setting base address

Selection of the base address on ISA bus (Figure3-1), as well as the addressing method (BASE Address Switch, Address mode) is performed with the use of SA1 switch; The switch has 8 engines. Engines BA[5:0] of SA1 switch (which are specified in the Figure as: BA0 … BA5) are intended for setting the base address (BA) of the module or segment of address SA[9:4] in the I/O area (I/O), which will make the module available for the system. The engine of the switch 8 is responsible for the type of addressing in DIC324 with regard to the I/O address space with or without an offset.



A) **B)**

Fig. 3-1: SA1 base address setting switch

Option: A)

The module uses an extended addressing and decryption of 20-bit system ISA-bus addresses (SA19 – SA0). The module is being addressed when the base address (BA) of the module (BA is assigned by setting the engines BA[5:0] of SA1 switch) are matched with the bits of addresses SA[9:4] in the I/O area (at the state of bits SA[15:12] = 0h). The ports occupy 16 bytes in the I/O area.

Option: B)

The module uses an extended addressing and decryption of 20-bit system ISA-bus addresses (SA19 – SA0). The module is being addressed when the base address (BA) of the module (BA is assigned by setting the engines BA[5:0] of SA1 switch) are matched with the bits of addresses SA[9:4] in the I/O area (at the state of bits SA[15:12] = Ah). The ports occupy 16 bytes in the I/O area.

NOTE: DELIVERIES OF DIC324 MODULE BY DEFAULT, WITH BASE ADDRESS CONFIGURATION – A110 (COMPLIES WITH FIG. 3-1 B)

When addressing to the module, the LED for indication of requests (references) is activated for a short period.
The table below shows the options of setting the base address (BA).

Table 3-1: SA1 switch setting

Base address (Hex) (Hex) SA1-8 = 1	Base address SA1-8 = 0	SA1-6 (BA5)	SA1-5 (BA4)	SA1-4 (BA3)	SA1-3 (BA2)	SA1-2 (BA1)	SA1-1 (BA0)
000h	A000h	0	0	0	0	0	0
010h	A010h	0	0	0	0	0	1
…	…	…	…	…	…	…	…
100h	A100h	0	1	0	0	0	0
110h	**A110h**	**0**	**1**	**0**	**0**	**0**	**1**
…	…	…	…	…	…	…	…
150h	A150h	0	1	0	1	0	1
…	…	…	…	…	…	…	…
200h	A200h	1	0	0	0	0	0
…	…	…	…	…	…	…	…
3E0h	A3E0h	1	1	1	1	1	0
3F0h	A3F0h	1	1	1	1	1	1

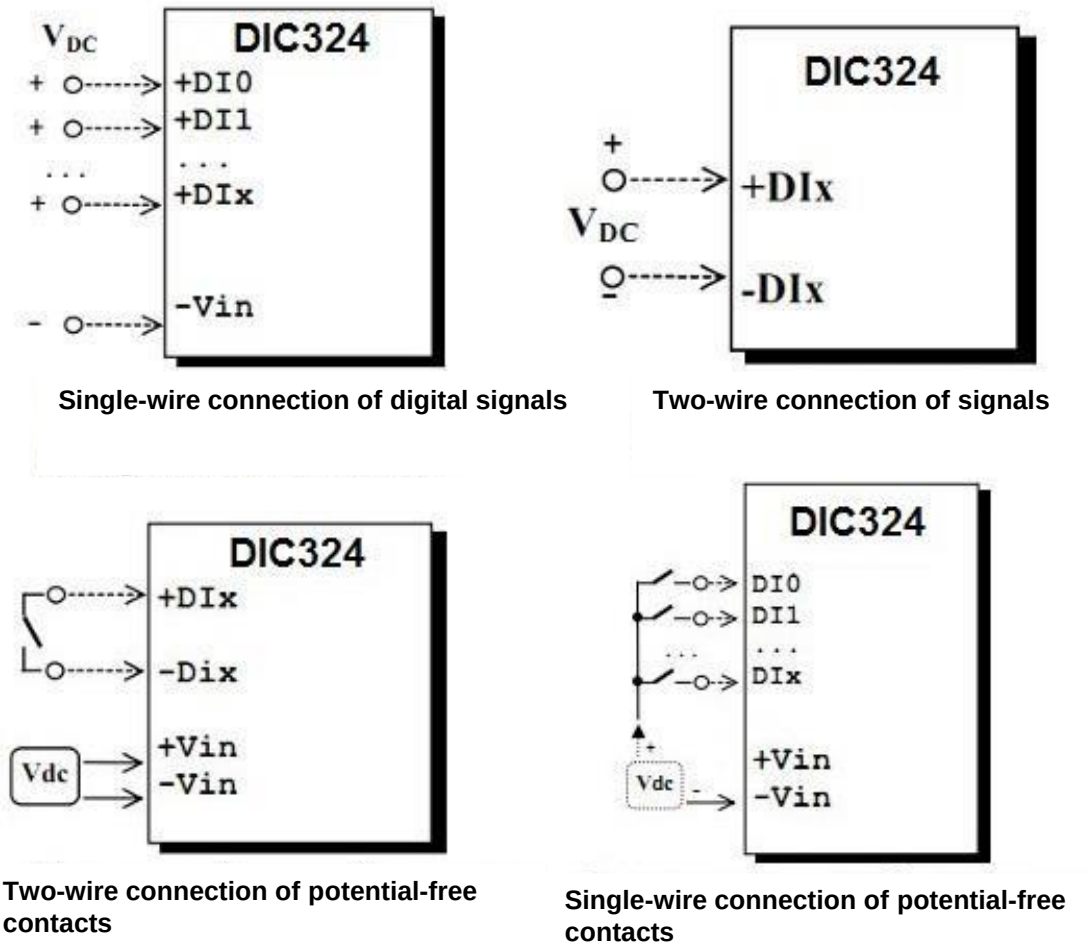
ATTENTION: **INCORRECT SETTING OF THE BASE ADDRESS COULD CAUSE COLLISIONS DURING MODULE'S OPERATION WITH SYSTEM'S EQUIPMENT. PRIOR TO THE FIRST MODULE ACTIVATION YOU NEED TO MAKE SURE THAT THE SET BASE ADDRESS IS NOT USED WITHIN THE SYSTEM!**

3.2.2 Jumpers for the installation of input signal connection type

Signals are connected to the DIC324 Module via XP10 connector (type IDC-34).

Connection types:

1. Single-wire connection of digital signals
2. Two-wire connection of digital signals
3. Two-wire connection of potential-free contacts
4. Single-wire connection of potential-free contacts



Single-wire connection of digital signals

Two-wire connection of signals

Two-wire connection of potential-free contacts

Single-wire connection of potential-free contacts

Fig. 3-2: Connection to the module

In case of changing a type of signal connection, the jumpers should be reset according to the below table.

Table 3-2: Type of inputs

Input number	Two-wire digital input	Single-wire digital and potential-free contact	Two-wire potential-free contact
0	XP20[3-5]	XP20[5-7]	XP20[1-3] & XP20[5-7]
1	XP20[4-6]	XP20[6-8]	XP20[2-4] & XP20[6-8]
2	XP19[3-5]	XP19[5-7]	XP19[1-3] & XP19[5-7]
3	XP19[4-6]	XP19[6-8]	XP19[2-4] & XP19[6-8]
4	XP18[3-5]	XP18[5-7]	XP18[1-3] & XP18[5-7]
5	XP18[4-6]	XP18[6-8]	XP18[2-4] & XP18[6-8]
6	XP17[3-5]	XP17[5-7]	XP17[1-3] & XP17[5-7]
7	XP17[4-6]	XP17[6-8]	XP17[2-4] & XP17[6-8]
8	XP16 [3-5]	XP16[5-7]	XP16[1-3] & XP16[5-7]
9	XP16[4-6]	XP16[6-8]	XP16[2-4] & XP16[6-8]
10	XP15 [3-5]	XP15[5-7]	XP15[1-3] & XP15[5-7]
11	XP15[4-6]	XP15[6-8]	XP15[2-4] & XP15[6-8]
12	XP14[3-5]	XP14[5-7]	XP14[1-3] & XP14[5-7]
13	XP14[4-6]	XP14[6-8]	XP14[2-4] & XP14[6-8]
14	XP13 [3-5]	XP13[5-7]	XP13[1-3] & XP13[5-7]
15	XP13[4-6]	XP13[6-8]	XP13[2-4] & XP13[6-8]

Two-wire connection of signals

With such a connection, the input signals are isolated from each other and the system. Each input signal is connected to the contacts by a couple of wires (without a common wire): +DIx, -DIx , where x=0...15.

Single-wire connection of digital signals

Such a connection can be used if signals have a common wire (ground or other potential), in which case the input channels are isolated only from the system. Each signal is connected to the relevant contact +DIx, where x=0..15, and a common wire to one of the contacts -Vin of the XP10 connector.

Two-wire connection of potential-free contacts

With the two-wire connection, the potential-free contact is connected to the contacts: +DIx, -DIx, where x=0..15. For supplying the potential-free contacts with power, an external source Vdc connected to contacts +Vin and -Vin of the XP10 connector will be used.

Single-wire connection of potential-free contacts

With the single-wire connection, the signal is connected to the relevant contact +DIx, where x=0..15. Using an external power supply source, the common wire is connected with the + of the external power supply source, and - to be connected with the contact -Vin at the XP10 connector.

3.2.3 Setting the range of input voltages.

Module DIC324 can be used for operation with voltages from 3.2 to 52 Volts (in two ranges see the table). Trigger threshold per each group of eight input channels is determined by assemblies of RN resistors, which are installed into the pads XS2, XS3.

Table 3-3: Trigger threshold per each group of eight input channels

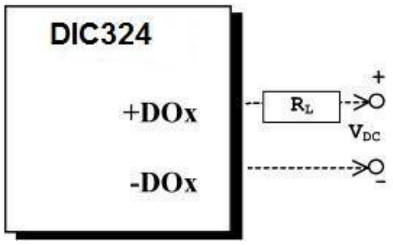
Subrange	Actuation voltage, V	RN assembly resistance rating
1	3.2 ÷20	470 Ω
2	4÷52	2.2 KΩ

3.2.4 Jumpers for the installation of switching load type

Connection of the load to the module DIC324 is carried out using the XP11 connector(type IDC-20).

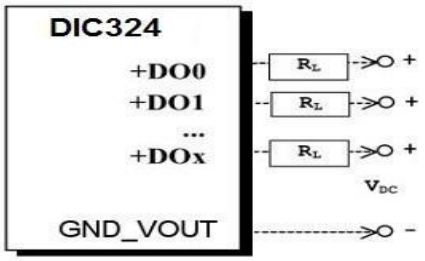
Connection types:

1. Single-wire connection;
2. Two-wire connection;
3. Digital output mode (level is set by the voltage +Vout)



Two-wire load connection

With such a connection, each switching signal is connected to the contacts via a couple of wires:
+DOx и -DOx , where x=0..7.



Single-wire load connection

Such a connection can be used if the voltages are switched with regard to the common ground of other overall potential, in this case each signal is connected to the contact +DOx (x=0...7), and the common wire - to the contact GND_VOUT of XP11 connectors or any contact -DOx.

Digital output mode

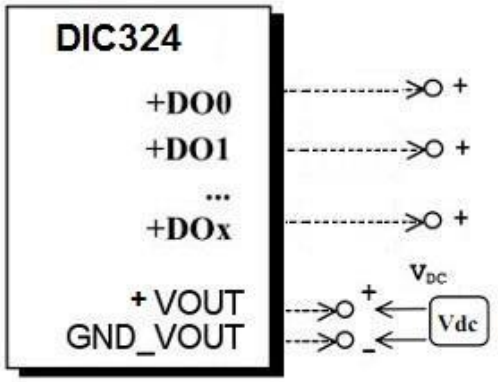


Table 3-4: Setting the load type connection

Connection type setting			
Output	Two-wire	Single-wire	Single-wire with an external power
0	**OFF**	XP1[3-4]	XP1[1-2] & XP1[3-4] & XP9 [1-2]
1	**OFF**	XP2[3-4]	XP2[1-2] & XP2[3-4] & XP9[1-2]
2	**OFF**	XP3[3-4]	XP3[1-2] & XP3[3-4] & XP9[1-2]
3	**OFF**	XP4[3-4]	XP4[1-2] & XP4[3-4] & XP9[1-2]
4	**OFF**	XP5[3-4]	XP5[1-2] & XP5[3-4] & XP9[1-2]
5	**OFF**	XP6[3-4]	XP6[1-2] & XP6[3-4] & XP9[1-2]
6	**OFF**	XP7[3-4]	XP7[1-2] & XP7[3-4] & XP9[1-2]
7	**OFF**	XP8[3-4]	XP8[1-2] & XP8[3-4] & XP9[1-2]

Warning!

In case of the load single-wire connection, it should be considered that despite the fact that each module's channel is able to switch currents with the load up to 500 mA, total current, returnable via GND_VOUT contacts, should not exceed the values 4A (2A per each GND_VOUT contact).

Warning!

Despite the fact that the module is able to switch the current load up to 500 mA within the entire temperature range (from - 40°C to +85°C), when using the module with the high environment temperature (from +75°C to +85°C), it is not recommended to activate maximum current load in adjacent channels. In this case you should either lower the load current down to 400 mA, or assume simultaneous activation of maximum load via channel, e.g. only in even or odd channels.

3.3 Description of registers and D11 user configuration

Below is the description of main ports' registers of the basic module configuration (D11):

– register of outputs (BA+0);

– register of inputs' states (BA+1, BA+2);

– register of interrupts (BA+Dh);

– register of diagram code identifier (BA+Eh, BA+Fh).

3.3.1 Configuration FPGA D11 – Digital_Inputs

D11 – basic option of the diagram for processing inputs. It represents a device that generates event interrupts with a programmable de-bouncing of contacts and a 16-channel frequency meter.

It enables to implement the following capabilities:

- programmable de-bouncing per each group of eight inputs: **40 ns, 400 ns, 4.5 ms, 140 ms**;
- programmable event edge per each group of eight inputs: 1→ 0, 0→ 1, (1→ 0 + 0→ 1);
- generation of maskable interrupt from each group of eight inputs;
- 32-x channel frequency meter;
- measuring method: filling with reference frequency;
- programmable period of filling frequency: (2...256) × 40 ns;
- programmable number of periods of measured frequency: 1...255;
- accuracy: up to 16 bit;
- generation of an interrupt from the frequency meter.

3.3.1.1 Integrated parts of the diagram

Matrix diagram involves the following function blocks:

- De-bouncing (DEB) unit
- Input register (RG)
- Event (EV) registration unit
- Programmable pulse gate generator of N- periods of
- measured frequency (T)
- programmable filling frequency generator (G):
- frequency meter (F)

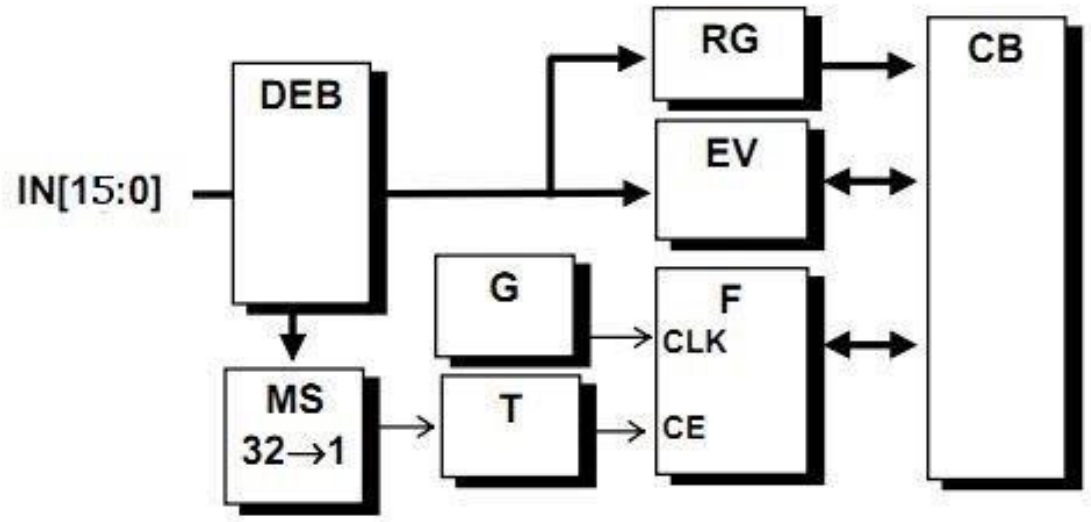


Fig. 3-3: Matrix diagram

Below is the description of DIC324 ports (*Code of "D11" diagram*) with the Base Address **BA.**

Control register is available by writing via port with the address BA+5 and has a format:

Table 3-5: Control register

Address	D7	D6	D5	D4	D3	D2	D1	D0
BA + 5	$FR1_1$	$FR0_1$	$FR1_0$	$FR0_0$	$CK1_1$	$CK0_1$	$CK1_0$	$CK0_0$

CK[1:0]$_X$ De-bouncing time codes for groups of inputs (see Table 3-7).

FR[1:0]$_X$ Event front edge codes for groups of inputs (see Table 3-6).

Table 3-6: Event front edge codes for groups of inputs

Groups of inputs	Inputs
0	IN[7:0]
1	IN[15:8]

Table 3-7: De-bouncing time codes for groups of inputs

FR[1:0] x	Event front edge in the group of
0	-
1	↑
2	↓
3	↑ + ↓

Table 3-8: Control register

CK[1:0] x	De-bouncing time in the group of channels x
0	40 ns ± 0.002 %
1	400 ns ± 0.002 %
2	4.5 ms ± 30 %
3	140 ms ± 30 %

Register of interrupts. Line of separable interrupts is set via the byte port with the address **BA + Dh**. The port is available when recording, has the following format:

Table 3-9: Register of interrupts

Address	D7	D6	D5	D4	D3	D2	D1	D0
BA + Dh	-	-	*GRP1*	*GRP0*	*INTF*	*LN2*	*LN1*	*LN0*

LN[2:0] Code of interrupt line (LN[2:0] = 3…7). Connection of interrupt line is carried out by writing of the code corresponding to the number of line IRQ3…IRQ7.

INTF Permit of interrupt from the frequency meter. During setting the bit the interrupts are permitted from the frequency meter.

NOTE: INTERRUPT FROM FREQUENCY METER - BIT INVERSION ST_RDY.

GRP1,0 Permission of interrupts from input groups (byte-wise). When setting the bits it is permitted, accordingly, to perform interrupts from input groups IN[15:8], IN[7:0].

Warning!

Interrupt signal reset will be carried out only after reset of the relevant bits in the *register of events.*

Reset of bits prohibits generation of interrupts.

Register of inputs is available **by reading via** byte ports with addresses **BA+1, BA+2**:

Table 3-10: Register of inputs

Address	D7	D6	D5	D4	D3	D2	D1	D0
BA + 1	*ST7*	*ST6*	*ST5*	*ST4*	*ST3*	*ST2*	*ST1*	*ST0*
BA + 2	*ST15*	*ST14*	*ST13*	*ST12*	*ST11*	*ST10*	*ST9*	*ST8*

ST[15:0] Status bits of inputs. Bits of register reflect the state of the relevant input (IN15.IN0) with the delay for the period of de- bouncing.

Register of events is available **by reading via** byte ports with addresses **BA+3, BA+4** and has the format:

Table 3-11: Register of events

Address	D7	D6	D5	D4	D3	D2	D1	D0
BA + 3	*EV7*	*EV6*	*EV5*	*EV4*	*EV3*	*EV2*	*EV1*	*EV0*
BA + 4	*EV15*	*EV14*	*EV13*	*EV12*	*EV11*	*EV10*	*EV9*	*EV8*

EV[15:0] Register of events Register bits are set when the status of the relevant input IN[15:0] is changed (edge of events is defined by bits $FR[1:0]_X$).

Warning!

Only one event per each input will be stored. For registration of the next event you will have to reset the relevant bit of the register of **events (writing 1** to the bit, where the event occurred).

Frequency meter **F** has two registers: *control register and data register.*

Control register is available via byte ports with addresses **BA+7..BA+9** and has the format:

Table 3-12: Control register

Address	D7	D6	D5	D4	D3	D2	D1	D0
BA + 7	*ST_RDY*	*ERR*	*-*	*-*	*CH3*	*CH2*	*CH1*	*CH0*
BA + 8	*T7*	*T6*	*T5*	*T4*	*T3*	*T2*	*T1*	*T0*
BA + 9	*G7*	*G6*	*G5*	*G4*	*G3*	*G2*	*G1*	*G0*

CH[3:0] Code of input, connected to the frequency meter (0 ... 15).

ERR Measuring error. The bit is set if the frequency meter is overfilled (F[15:0]> 0xFFFF). The bit is reset in case of any writing to the port BA+7.

ST_RDY Bit Start / Frequency meter readiness. Bit setting starts the frequency measurement process, bit reset interrupts the measurement process (in which case, the state of the *data register* **is not determined!**). Bit is reset automatically if the measurement is successful (N-periods of the measured frequency are obtained, starting from the falling edge), or meter is overfilled. Bit reading enables to determine meter readiness to the next measurement (state 1-ready, 0- busy).

T[7:0] Code of the number of periods of the frequency measured (from 1 to 255, **code** T[7:0]=

0 is not used).

Warning!

Code of time intervals is not saved after measuring and should be set before each measuring.

G[7:0] Filling frequency code (from 1 to 255, code 0 is not used).

Filling frequency in MHz is determined using the formula: **F=25 / (G[7:0]+1);**

E.g., in order to get the filling frequency of 1 MHz, the code G[7:0] = 24 should be set.

16-bit register of data is available through the reading via the word port with the address **BA+Ah** and has a format:

Table 3-13: Register of data

Address	D15	D14	D13	…	D3	D2	D1	D0
BA + Ah	*F15*	*F14*	*F13*	*…*	*F3*	*F2*	*F1*	*F0*

F[15:0] 16-bit code of duration of **N-periods** of the measured frequency (number of the measured frequency periods is set

by the code T[7:0]). Value of the least significant bit corresponds to the filling frequency period (in accordance with code G[7:0] - from 80 ns to 10.24 μs).

3.3.2 Configuration FPGA D11 - Digital_Outputs

Basic option of controlling the outputs enables to implement the following capabilities:

- 8 digital output channels;
- Single-wire or two-wire signal connection;
- Switching output voltages/currents: 60 V / 500 mA (where the differential type of load connection is used);
- automatic reset through power supply activation and hardware RESET;
- Control of outputs states (up to optical isolation).

3.3.2.1 Integrated parts of the diagram

The block diagram of digital output includes:

- output register (RG)
- output buffer (BUF)
- optical isolation unit (Opt)
- output switches (OUT)

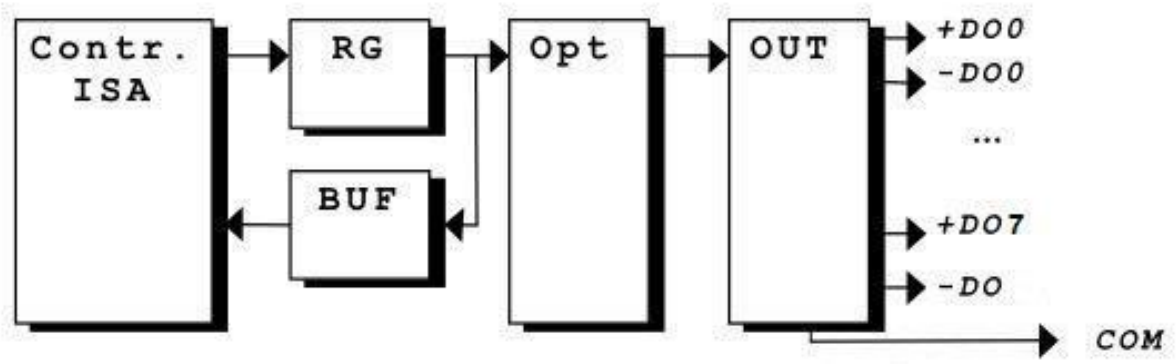


Fig. 3-4: Integrated parts of the block-diagram

3.3.2.2 Designation of outputs ports

Control of DIC324 is carried out via the I/O ports. Addresses of the ports are set with regard to the Base Address (BA), set by the SA1 switch.

Register of outputs is available through recording and reading via the port with BA+0 address.

Switching the output ***x*** of the board is carried out by setting the relevant bit in the register of outputs. Reading the buffer if outputs makes it possible to determine the current state of outputs (1 - closed, 0 - open).

Table 3-14: Register of outputs

Address	D7	D6	D5	D4	D3	D2	D1	D0
BA + 0	*DO7*	*DO6*	*DO5*	*DO4*	*DO3*	*DO2*	*DO1*	*DO0*

3.3.3 Module identification

TheFPGA1 has its own identifier, which coincides with the code of the diagram, loaded to the FPGA. The identifier could be read via the byte ports with addresses BA+Eh, BA+Fh (where BAx – base address of the FPGA1).

NOTE: **THE MODULE IS DELIVERED WITH A WORKING CODE OF THE "D11" DIAGRAM BY DEFAULT.**

NOTE: **SOME VERSIONS OF THE DIAGRAMS LOADED TO THE FPGA MAY NOT HAVE ITS OWN IDENTIFIER (SHALL BE ADDITIONALLY AGREED IN THE RELEVANT TEXT FILES OF DESCRIPTIONS OF THE LOADED DIAGRAMS' VERSIONS).**

Register of the diagram code identifier is available through the byte ports with addresses BA+Eh, BA+Fh.

Designation of register bits for ports with addresses BA+Eh, BA+Fh is shown in the tables below.

Table 3-15: Port (BA+Eh) through reading

Bit	Notation Conventions	Purpose
D0–D7	‘a … z’	ASCII code of Latin capital letters from “a” to “z” [1)]
[1)] Identifier letter (conventional symbol of the diagram type): “c” – counters, “f” – frequency meters, “g” – signal generators, “t” – timers, “x” – special custom options of diagrams.		

Table 3-16: Port (BA+Fh) through reading

Bit	Notation Conventions	Purpose
D0–D7	SN[7:0]	Diagram number code from “0” to “255” [1)]
[1)] Identifier digits (sequence number of the diagram type):		

Programming example for reading the FPGA1 identifier in “C” language shall be viewed as follows:

```
printf ("DIC324 Diagram Code:\"D11\"     FASTWEL, 2016\n");

   // -- Determine Base Address ---- for

   (BA=0x110;BA<0x400;BA+=0x10)

    if ((inportb(BA+0xA00E)=='D')&&(inportb(BA+0xA00F)==11)) break;

   if (BA==0x400) { printf("Diagram Code\"D11\"not loaded !");return;

   } else printf("Base address of DIC324 module is

   determined:%Xh\n",BA);
```

3.3.4 Reprogramming user FPGA configuration

Module's hardware and software makes it possible to program the user's FPGA configuration directly in the system, via MicroPC bus (ISA). In this case, it is possible to program both - directly FPGA itself (configuration is not saved in case of power supply failures), and to program loading EEPROM (FPGA configuration is automatically loaded from EEPROM with the power on).

FPGA configuration reprogramming is carried out using the programs, which can be found at Fastwel FTP-server.

To program FPGA directly the following utility is used: **isa_jtag.exe**. The example is shown below:

```
-------------------------------------------
writing configuration to DIC324:
-------------------------------------------
isa_jtag.exe SB=[XX]  [file name]
                  |       |
                  |       |
                  |       +-----  File .XSV created using the program
ISE
                  |               iMPACT
                  +-------------  Module base address(hex)
```

The utility can also work with the following keys:

isa_jtag.exe xxx - output of codes and configurations using the base address of the module, where xxx is the base address of the module;

isa_jtag.exe /? - output of the help line

NOTE: AT FASTWEL FTP-SERVER YOU CAN FIND ".XSV" FILE, DESIGNED FOR PROGRAMMING FPGA1 BY DEFAULT CONFIGURATION

To program EEPROM the following utility is used: **eeprog.exe**. The required configuration is programmed to the user FPGA1 by starting the utility eeprog.exe with the relevant parameters specified in the example below:

```
-------------------------------------------
writing configuration to DIC324:
-------------------------------------------
eeprog.exe SB=[XX][file_name] FPGA1
           |       |       |
           |       |       |
           |       |       + FPGA1 matrix
           |       +-------- Name of the programming BIN-file
           +---------------- Module base address
```

E.g. for programming FPGA1 the default configuration in the module configured to the base address 0xA110, you should specify:

```
eeprog.exe SB=A110 usercfg.bin FPGA1
```

The utility can also work with the following keys:

eeprog.exe SB=[XX] [file name] FPGA1 /v – verification of the programmed configuration; **eeprog.exe SB=[XX] FPGA1 /e** - deleting EEPROM in the selected FPGA; **eeprog.exe SB=[XX] /r** – output of information on the current version
Base FPGA configuration (Starting from utility eeprog 1.1);
eeprog.exe xxx - output of configuration codes via module's base address, where xxx is the module's base address;
eeprog.exe /? - output of the help line

NOTE: CONFIGURATION FILES FOR FPGA WITH DESCRIPTIONS AND EXAMPLES OF "C" PROGRAMMING CAN BE FOUND AT FASTWEL FTP-SERVERS.

4 Transportation, unpacking and storage

4.1 Transportation

The module should be transported in a separate packaging box (transport packaging) of the manufacturing facility, which consists of an individual antistatic bag and a cardboard box, in the closed transport (automobile, railway, air transportation in heated and pressurized compartments) in storage conditions 5 defined in the GOST standard 15150-69 (IEC 721-2-1 standard) or in storage conditions 3 during sea transportation.

It is possible to transport modules, packaged in individual antistatic packages, in multiple packaging (transport packaging) of the manufacturing facility.

The packaged modules should be transported in accordance with the shipping rules, operating with this particular type of transport.

During handling and transportation operations, the packaged modules should not undergo sharp pounding, falls, shocks and exposure to atmospheric precipitation. The packaged modules should be stored in a carrier vehicle in such a manner which will prevent their moving.

4.2 Unpacking

Prior to unpacking, before transportation at subzero temperature of ambient air the modules should be kept within 6 hours under storage conditions 1 defined in the GOST standard 15150-69 (IEC 721-2-1 standard).

It is prohibited to place the packaged module close to the heat source, prior to unpacking.

While unpacking, it is required to comply with all safety precautions, which ensure its safety, as well as marketable condition of consumer packaging of the manufacturing company.

At the time of unpacking it is required to check the module that it has no external mechanical damages after transportation.

4.3 Storage

Module storage conditions for group 1 are defined in the GOST standard 15150-69 (IEC 721-2-1 standard).

ANNEX A

DISCLAIMER

This Disclaimer contains special operating conditions of Fastwel in the following areas: intellectual property, warranty policy, conditions of the order and delivery.

1 INTELLECTUAL PRORETY

1.1 If any infraction, interference, improper use, illegitimate exploitation and/or violation of the industrial and/or intellectual property rights of any third party and/or property, exploitation during the use of Fastwel Embedded Module will take place – Fastwel does not guarantee to replace the materials, computer programs, procedures or equipment affected by the complaint and under no circumstances doesn't bear responsibility in any form for possible refusal in case of such a replacement.
1.2 Use of the Fastwel products as well as the objects of intellectual property containing in them, in the ways and for the purposes, not provided by the present user manual and datasheet isn't allowed without preliminary written approval of Fastwel.
1.3 Fastwel is not responsible for possible incidents and losses, related to the operation of end devices, in which the original Fastwel equipment is used.

2 WARRANTY POLICY

2.1 When the detected flaws in an element can be corrected without decreasing the foreseen technical features and functionality for it, User may demand Fastwel the urgent correction of the failures in additionally agreed period and an increasing of the period of the guarantee of the element equal as the time elapsed from the formal request to repair the failures, until the receipt of the repaired element. All costs associated to the correction of failures, included those of assembly, dismantle, transport, tests, etc, if they exist, shall be prosecuted according the Warranty Policy of Fastwel.

3 ORDER AND DELIVERY CONDITIONS

3.1 The general rule is that all Fastwel equipment prices are determined with due consideration of delivery under the EXW terms and conditions (Incoterms 2010). Delivery of the products under other terms and conditions should be preliminary agreed and stated in writing between the parties.
3.2 Unless otherwise expressly agreed with Fastwel, all the deliveries of Fastwel equipment will be carried out only after the official purchase order is obtained and provided that the ordered products have been prepaid in full. Other terms and conditions of cooperation should be made in writing.
3.3 Any delivery of Fastwel electronics is submitted with the right package in accordance with the current rules and standards in the Member States of the European Economic Area. The purchaser independently bears all risks regarding the compliance of package and marking of Fastwel products with legislation requirements being in effect at the place of purchased products destination (in the buyer's country). The specified condition excludes unequivocally any liability of Fastwel for possible non-compliance of package and marking of products with the requirements of legislation of the country of products destination.
3.4 In general, all components of the supply are properly protected with respect to freight, in order to avoid any damage to the supply, third parties, environmental damages or unrelated goods, as consequence of wrong packaging.
3.5 Each package unit is labeled on the exterior area with the indications of product's Part Number and Serial Number.
3.6 The support documents for the order should be made either in English or in Russian unless otherwise agreed between parties in writing.
3.7 Fastwel does not pay penalties and does not cover costs associated with delay in the delivery of the products caused by actions of the third parties, force-majeure etc. - Fastwel doesn't bear any responsibility for non-execution or inadequate execution of the obligations in a case when it is caused by actions of the third parties (for example producers or suppliers of accessories), force majeure etc.
3.8 Fastwel declares that independently and at any time without damage, it has an exclusive right to define and change functionality architecture, bill of materials of its products without any preliminary coordination and approvals of the third parties.

4 OTHER CONDITIONS

4.1 Fastwel has the obligation to respect the current Russian legislation (including, but not limited to environmental, labor, social laws) in each moment and to apply it to its embedded electronics considering all and each execution phase, that is to say, from the design until the commissioning and subsequent maintenance. In this regard Fastwel is not liable to the user or other persons in connection with possible changes of the company's rules (including, but not limited to warranty, ordering policy) caused by changes of the Russian legislation.
4.2 Unless otherwise expressly agreed in writing, Fastwel provides no training for assembly\installation\adjustment\operation of its equipment.