DIC551 I/O Module

User Manual

Revision 1.3
January 2017

The product described in this manual is compliant with all related CE standards.

Product Title: **DIC551**
Document name: **DIC551 User Manual**
Manual version: 1.3

Revision Record

Revision No	Brief description of changes	Board index	Revision date
1.0	**Initial version**	**DIC551**	**September 2015**
1.1	**Annexes B,C,D,E,F were changed. Added information on the front/rear input. Version DIC551-03 (Evaluation Kit) was added.**	**DIC551**	**February 2016**
1.2	**Information on MIC1002, MIC1003, MIC1004 was added. Dimensions and weight of the devices were changed.**	**DIC551, DIC551RC, MIC1002, MIC1003, MIC1004**	**May 2016**
1.3	**Compliance assessment**	**DIC 551**	**January 2017**

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Notation Conventions

Warning!
ESD Sensitive Device!

This symbol draws your attention to the information related to electro static sensitivity of your
product and its components. To keep product safety and operability it is necessary to handle it with care and follow the ESD safety directions. Also see the section below, dedicated to instructions on how to handle the board and unpacking procedure.

Warning!

Information marked by this symbol is essential for human and equipment safety.
Read this information attentively, be watchful.

Note

This symbol and title marks important information to be read attentively for your own benefit.

This User Manual (hereinafter referred to as the User Manual) is designed for getting information on the device, its operation principle and other key information, required for putting it into operation, intended use and maintenance of the devices: DIC551 I/O Module, DIC551RC I/O Module (hereinafter referred to as the module), as well as the mezzanines MIC1002, MIC1003, MIC1004 installed on the modules.

Safety requirements

This product is designed and tested for the purpose of ensuring compliance with the electric safety requirements. Its design guarantees long-term failsafe operation. Life cycle of the device can be sufficiently reduced due to improper handling during unpacking and installation. Therefore, for your own safety and in order to ensure the proper operation of the device, you should observe the below recommendations.

High Voltage Safe Handling Rules

Warning!

All the works that involve this device should be carried out by the appropriately qualified personnel.

Warning, high voltage!

Before installing the board into the system, make sure that the mains supply is switched off.

During installation, repairs and maintenance of the device there is a real danger of exposure to electric shock, therefore you should always disconnect the power supply feeding cable from the socket at the time of works. This also applies to the other power supply feeding cables.

General Board Operation Rules

- To keep the warranty, the product should not be altered or revised in any way. Any alterations or improvements not authorized by Fastwel LLC, except for those specified in this document or obtained from the technical support department of Fastwel LLC as a set of instructions for their implementation, cancel the warranty.
- This device should be installed and connected only to the systems, meeting all the necessary technical and climatic requirements.
- While performing all the required operations for installation and adjustment, please follow the instructions specified only in this document.
- Keep the original package for subsequent storage of the device and transportation in the warranty event. If it is necessary to transport or store the board, please pack it the same way as it was packed upon delivery.
- Exercise special care when unpacking and handling the device. Act in accordance with the instructions given above and in the paragraph 5 Transportation, unpacking and storage.
- Do not leave the board without protective packaging, when it is not operated.

MANUFACTURER'S WARRANTIES

Warranty liabilities

The Manufacturer hereby guarantees that the products supplied thereby are free from defects in workmanship and materials, provided operation and maintenance norms were observed during the currently established warranty period. The Manufacturer's obligation under this warranty is to repair or replace free of charge any defective electronic component being a part of a returned product.

Products that broke down through the Manufacturer's fault during the warranty period will be repaired free of charge. Otherwise the Consumer will be invoiced as per the current labor remuneration rates and expendable materials cost.

Liability limitation right

The Manufacturer shall not be liable for the damage inflicted to the Consumer's property because of the product breakdown in the process of its utilization.

Warranty period

The warranty period for the products made by Fastwel LLC is 24 months since the sale date (unless otherwise provided by the supply contract).

The warranty period for the custom-made products is 36 months from the date the Product was fist purchased (unless otherwise provided by the supply contract).

Limitation of warranty obligations

The above warranty obligations shall not be applied:

- To the products (including software), which were repaired or were modified by the employees, that do not represent the manufacturer. Exceptions are the cases where the customer has made repairs or made modifications to the devices in the strict compliance with instructions, preliminary agreed and approved by the manufacturer in writing;
- To the products, broken down due to unacceptable polarity reversal (to the opposite sign) of the power supply, improper operation, transportation, storage, installation, mounting or accident.

Procedure of device returning for repairs

Sequence of activities when returning the products for repairs:

- Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization;
- Attach a failure inspection report with a product to be returned in the form, accepted by the Manufacturer, with a description of the failure circumstances and symptoms;
- Carefully package the product in the manufacturer's antistatic bag (carton box), in which the product had been supplied. Failure to package in antistatic material will unilaterally VOID all warranties.
- The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer.

1 Introduction

GENERAL INFORMATION

1.1. Purpose and Technical Features

1.1.1. Purpose

Universal carrier-board (DIC551xx) of analog and digital I/O modules is designed for operation using CompactPCI® Serial Bus. The module is created with mezzanine technology, using the carrier-board and a set of mezzanines (MIC1002 – MIC1004). Module's functional capabilities are determined by the installed mezzanines. The module is designed for the use in real-time control, production monitoring, data acquisitions systems etc.

Mezzanines carrier (module) is carried out in the standard CompactPCI® Serial 4HP 3U PCIe x1 for DIC551 and CompactPCI® Serial 5HP 4U PCIe x1 for DIC551RC. The module ensures placement in Eurocard form-factors and form-factors with conduction cooling (PICMG CPCI-S.0 R1.0, section 3). `It can be equipped with up to 2 mezzanine boards and ensures possibility of rear or front output of signals from mezzanine, according to the version.

The mezzanine is functionally complete board that ensures analog or digital I/O. Mezzanine versions doesn't depend on the computer's system bus used, communication between mezzanine and carrier board is carried out with the use of "simple" serial and parallel communication channels (SPI, SPORT, UART etc.). Communication of the "simple" communication channels and system bus is carried out by the carrier-board.

Output type rear/front:

Notation·	Output	Note
DIC551-01· DIC551RC-	Front	Mezzanines·MIC100x-**01**·are·installed
DIC551-02· DIC551RC-	Rear	Mezzanines·MIC100x-**02**·are·installed
MIC1002-01,· MIC1003-	Front	
MIC1002-02,· MIC1003-	Rear	

1.1.2 Technical features

Carrier-board technical features

- Parallel port of type 1 – 2 pcs.
- Parallel port of type 2 – 1 pcs.
- Module for operation with the serial-access memory and interrupts – 1 pcs.
- Serial port of type 1 (SPI) – 4 pcs.
- Serial port of type 2 (SPORT). Transmitting module – 2 pcs.
- Serial port of type 2 (SPORT). Receiving module – 2 pcs.
- Serial port of type 3 (UART) – 4 pcs.
- Timer module - 1 pcs.
- Wishbone bus – 1 pcs

Technical features of RS485/422/232 interfaces mezzanine MIC1002:

- 4x independently configured RS232 or RS422\RS485 channels;
- galvanic isolation, 750 V;
- ESD protection;
- interface is compatible with UART 16550A.

Technical features of the digital I/O mezzanine MIC1003:

- 48 x digital I/O lines;
- output levels 5V CMOS;
- ESD protection.
- possibility to get interrupts by changing the state of the line;
- galvanic isolation, 750 V;
- De-bouncing of contacts;
- Frequency measurement function;
- possibility to connect UART to any mezzanine output (only RX, TX lines).

Technical features of the MIC1003 mezzanine of current loop interfaces:

- 4 x independently configured "current loop" channels;
- galvanic isolation, 750V;
- ESD protection;
- Maximum transmission speed: 19200 baud;
- interface is compatible with UART 16550A;
- active\passive operation mode.

Module power supply:

- Power supply voltage +12V, in accordance with the standard CompactPCI® Serial.;

Power supply of mezzanines:

- Power supply of mezzanines from the carrier-board: +12V, +3.3V.

Operation conditions:

- operating temperature range: from - 40° C to +85° C for DIC551;
- operating temperature range: from - 50°C to +85°C (on the cassette) for DIC551RC, MIC1002, MIC1003, MIC1004;
- relative humidity – from 5 to 95 % at +25° C (without condensation);

Mechanical features:

MTBF:

- DIC551, DIC551RC: 680000 hours;
- MIC1002: 250000 hours;
- MIC1003: 730000 hours;
- MIC1004: 140000 hours;

Electromagnetic compatibility (EMC):

- radio interference industrial, from information technology equipment – does not exceed the values according to the GOST standard 30805.22 for A-class industrial units;
- EMI resistance – in accordance with the GOST CISPR 24.

Dimensions, no more than:

- DIC551: 131.0 mm x 214.0 mm x 21.0 mm;
- DIC551RC: 183.5 mm × 134.0 mm x 25.4 mm;
- MIC1002: 146.0 mm × 42.0 mm x 20.32 mm;
- MIC1003: 146.0 mm × 42.0 mm x 20.32 mm;
- MIC1004: 146.0 mm × 42.0 mm x 20.32 mm.

Note – MTBF values are calculated according to the Telcordia Issue 1 computational model (calculation method - Method I Case 3) for continuous operation in case of the on-ground placement, under conditions corresponding to the Moderately Cold Climate 4 climatic category, in accordance with the GOST 15150-69, at the ambient temperature of + 30 °C.

1.2 MODULE STRUCTURE AND OPERATION

1.2.1 Location of main components

Location of main components (including connectors for module's external connections) is shown in figure 1.1. Reference designators of the connectors in the figure correspond to the ones on the module's board.

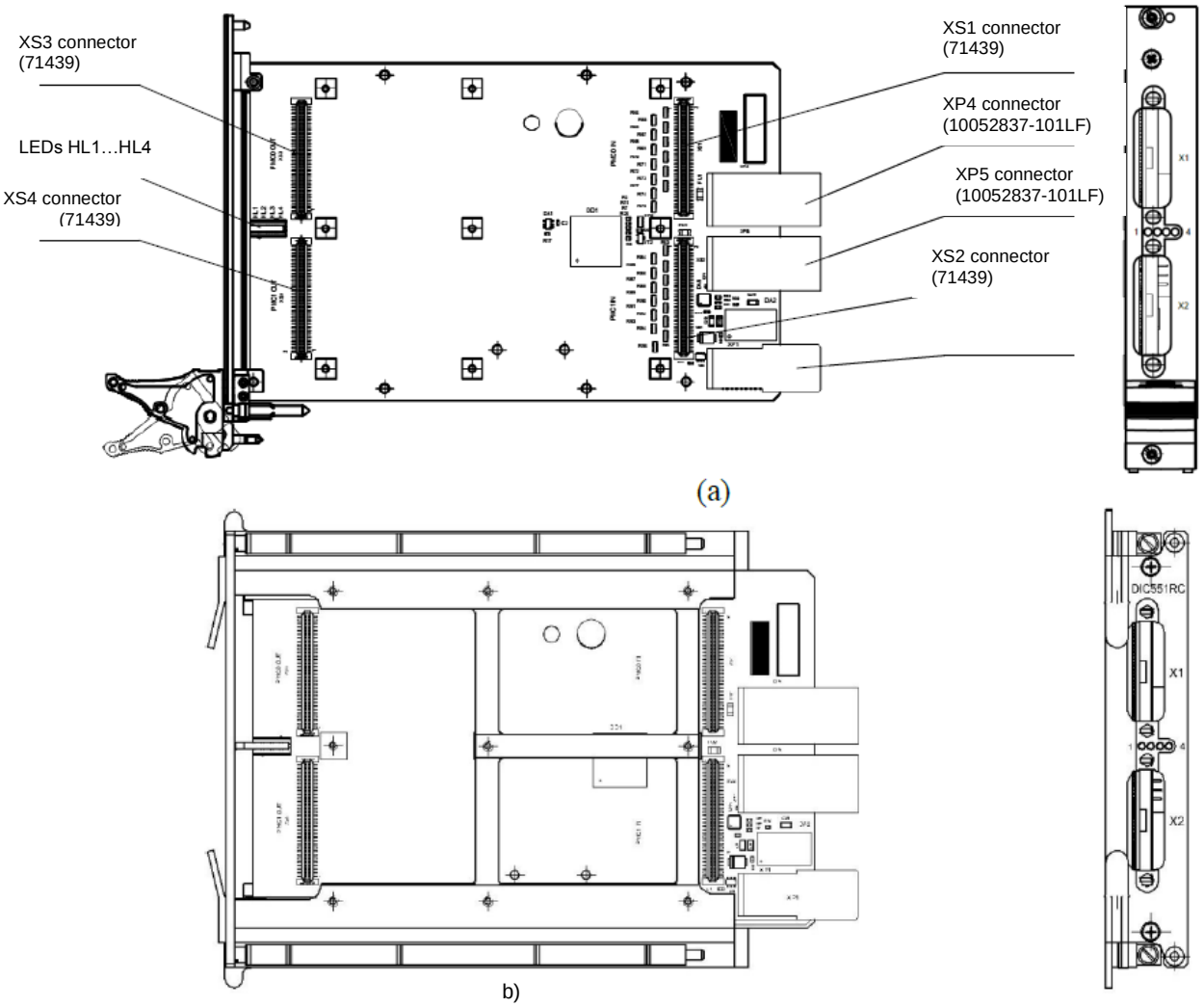


Figure 1.1 – Major components and connectors of the module; (a) – DIC551; (b) – DIC551RC (there are no XS3 and XS4 connectors for the versions with front output)

Mezzanine is installed at a height of 10.5 mm from the carrier-board. One carrier-board can have up to 2 mezzanine boards with 50 (power boards - with 26) contact outputs or a single double-size mezzanine installed on it.

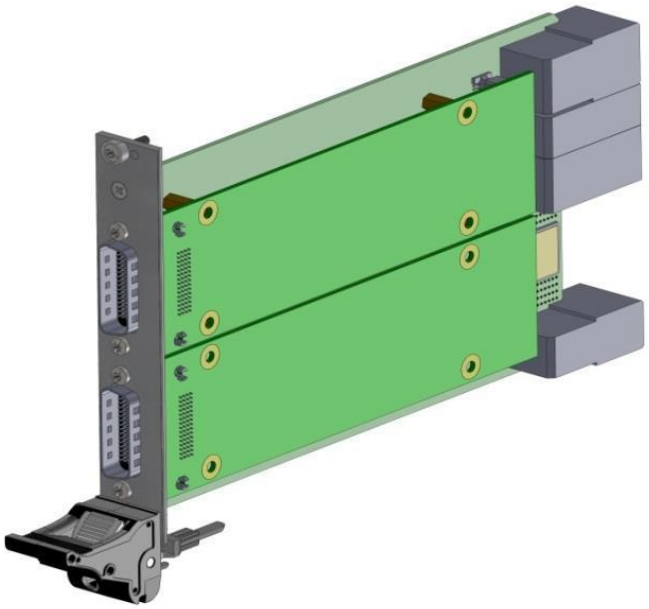


Figure 1.2 – External view of the module, ready-assembled

There are two versions of mezzanines manufactured – front output of signals and rear output of signals, via DIC551xx carrier-board to the system backplane.

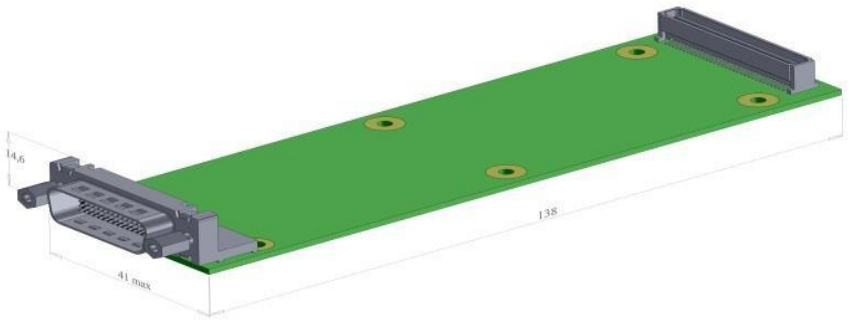


Figure 1.3 – Mezzanine with the front output of signal

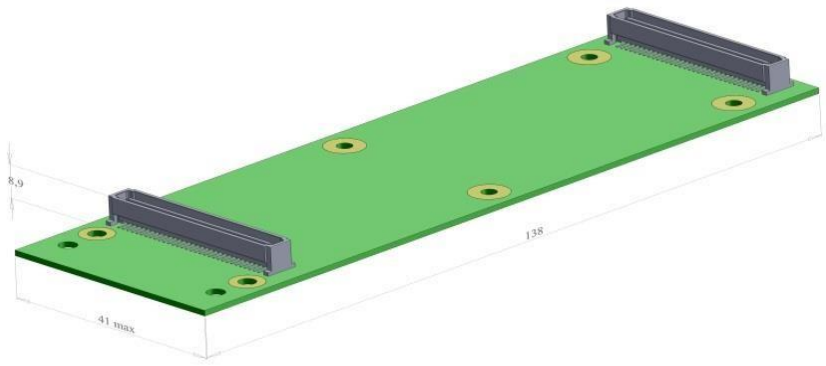


Figure 1.4 – Mezzanine with rear output of signal

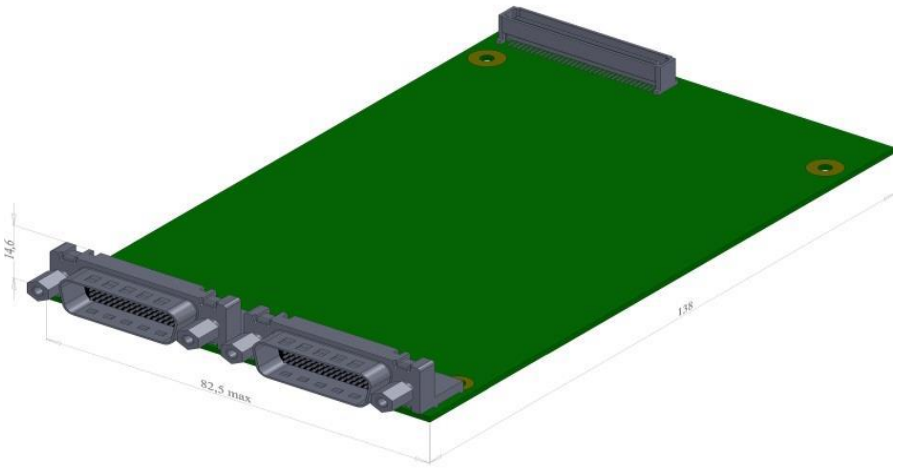


Figure 1.5 – Double-size mezzanine with the front signal output

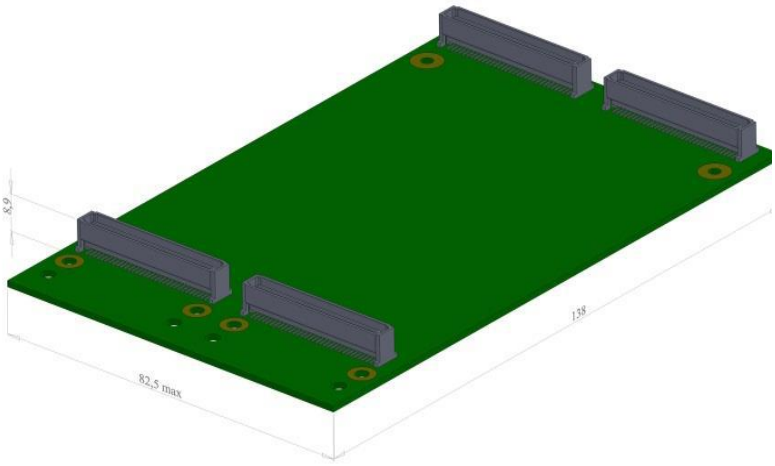


Figure 1.6 – Double-size mezzanine with rear signal output.

Various versions of the front panels of the I/O module are shown in the figures below.

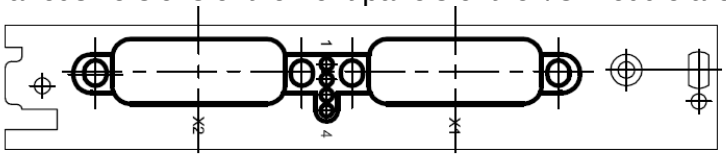


Figure 1.7 – Panel IMES.741555.011 (installation of two connectors of DB-15* type)

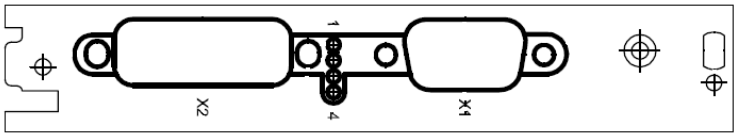


Figure 1.8 – Panel IMES.741555.011-01 (installation of the connectors of DB-9 and DB-15* types)

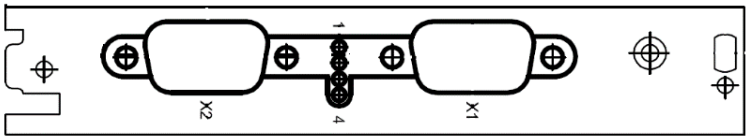


Figure 1.9 – Panel IMES.741555.011-02 (installation of two connectors of DB-9* type)

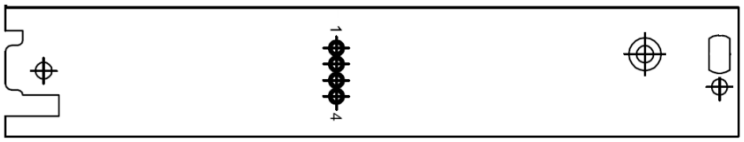


Figure 1.10 – Panel IMES.741555.011-03 (solid panel is used in case of rear output)
* - or similar, but coinciding in coupling sizes.

1.2.2 Block diagram of the carrier-board

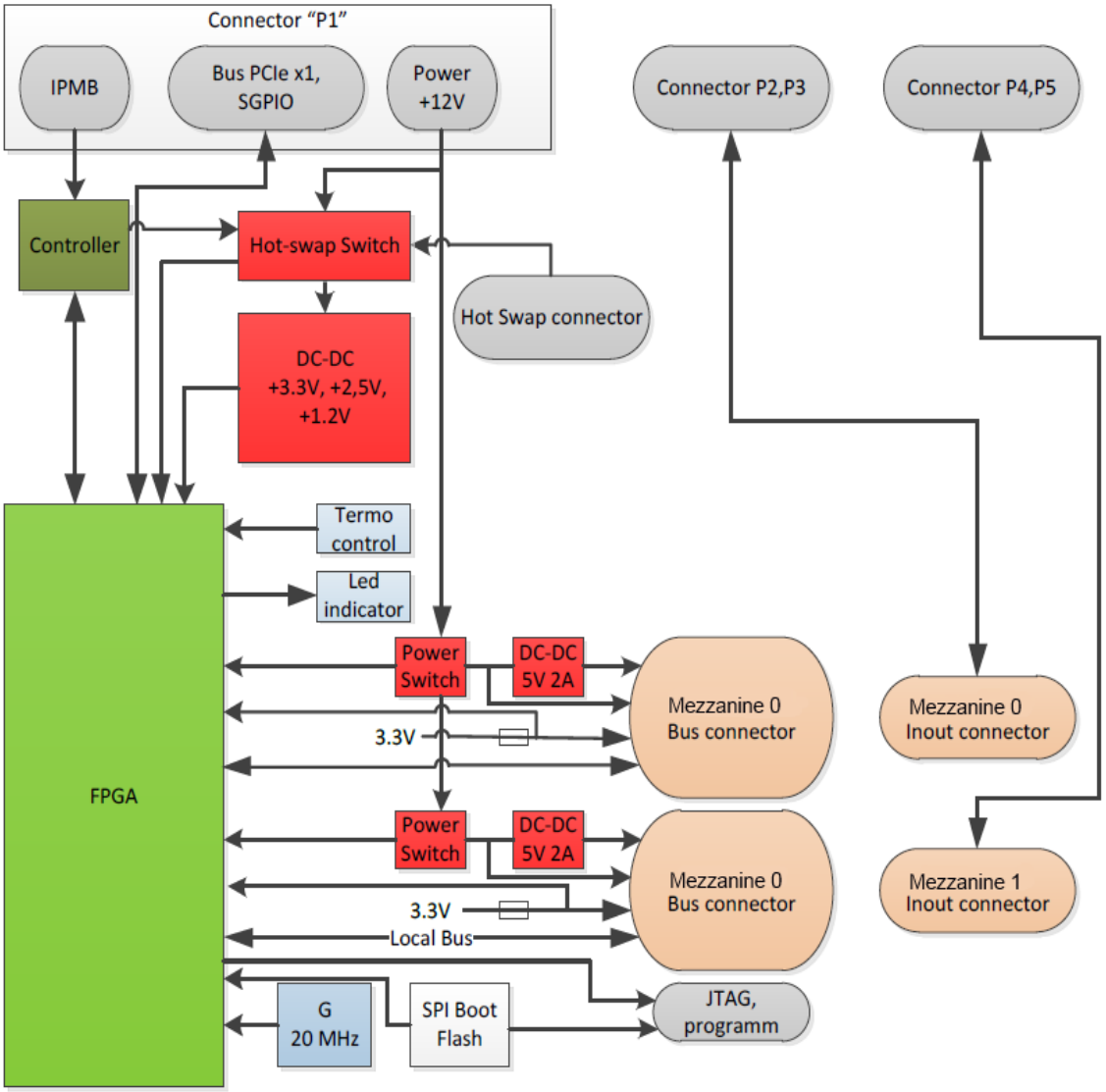


Figure 1.11 – Block diagram of the carrier-board

The carrier-board is based on the Spartan-6 FPGA with integrated PCIe x1 transmitter-receiver unit. FPGA implements interface of exchange over PCIe bus and functionality of controlling mezzanine boards, FPGA also controls and manages mezzanine power supply. Additional microcontroller unit installed on the carrier-board and having its own power supply, controls performance capability of the FPGA, power supply parameters of mezzanines and carrier-board. Communication between CPU and microcontroller unit is carried out via IPMB bus. Power supply of mezzanines is carried out by voltage of 12 V; in order to control power supply of each mezzanine there are intelligent keys with current protection capability. Each mezzanine receives additional low power supply of 3.3 V, used for power supply of mezzanine identification memory and level converters. For connection of mezzanines, 64 contact board-to-board connectors are used.

Each mezzanine is connected with FPGA multiplexed bus that has the following interfaces: SPORT 2 x channels, SPI 4x channels, UART 16550A 4x channels, parallel port 16 bits 3x channels, 32x bit Wishbone bus.

1.2.3 Distinctive features of carrier-board

Distinctive features of the carrier-board are the following:

- interface with CompactPCI Serial x1 system bus.
- interfaces available on the multiplexed bus for each mezzanine:
- 4x UART interfaces (1 Mbaud)
- 2x SPORT – serial interfaces with maximum word length of 32 bit and frequency up to 32 MHz, as well as support of TDMA and I2S modes.
- 4x SPI interfaces with the maximum word length of 32 bit and and clock frequency up to 32 MHz.
- 16 bit parallel port with a possibility of generation of signal output pulses (access time is determined by the cPCI Serial bus cycle).
- 16 bit parallel port with a possibility of generation of interrupts when changing the state of port outputs (access time is determined by the cPCI Serial bus cycle).
- 16 bit parallel port (access time is determined by the cPCI Serial bus cycle).
- 32 bit bus compatible with Wishbone bus with the clock frequency of 32 MHz.
- interface for mezzanine identification (SPI)
- 2x timer-counters compatible with 8254, with the clock frequency of 20 MHz.

1.2.4 Connection of mezzanines to the carrier-board

All the interfaces on the carrier-board are available simultaneously, but due to the limitation of the number of contacts on mezzanine connectors, each (from 9 to 56) connector output for mezzanine connection can be connection to one of the 4 interfaces, according to the table 20. Function of each output is configured individually and is determined by the "Device Switching Register" of the relevant parallel port.

1.2.5 Description of mezzanines

Mezzanine general structure. Mezzanine (Fig.1.12) represents a board, which is installed on the carrier-board. Operations with mezzanine on the part of computer are carried out via combination of interfaces, provided by the carrier-board. On the board, in addition to mezzanine functionality, there are such identification tools as:

hard key – hardware key, designed for identification of mezzanine availability.

flash key – a memory chip with serial interface. Contains information on the board, type of protocols used, mezzanine configurations etc., which is required for automatic configuration of module's driver.

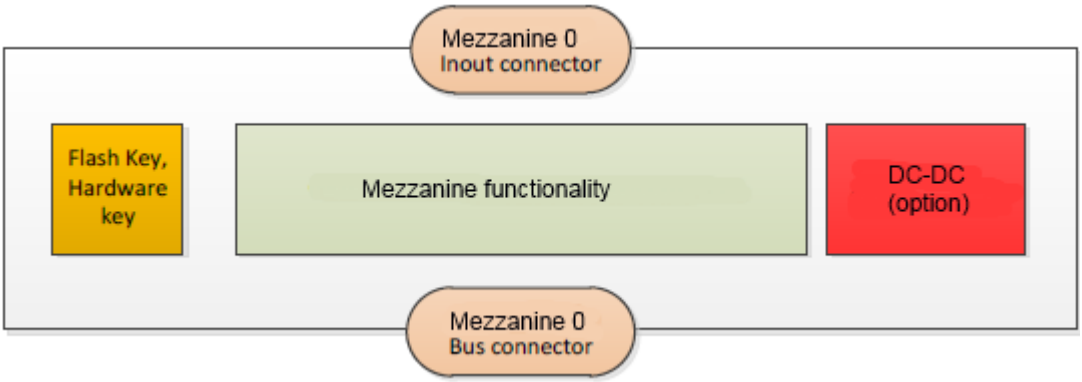


Figure 1.12 – General block diagram of the mezzanine

1.2.5.1 MIC1002 mezzanine of RS485/422/232 interfaces

The mezzanine is designed for I/O operations via 4 individual galvanic isolated serial ports of RS232\RS485\RS422 type and represents the board for conversion of signal levels from UART, located on the carrier-board, into signal levels of the relevant standards. Switching of port types is carried out using micro-switches.

Main features:

- 4 x channels of RS232\RS485\RS422 ports;
- galvanic isolation of channels, 750V;
- protection of output signals against ESD;
- full support of RS232 port (9 pin);
- connection of load resistance of 120 Ohm for RS485;
- 2 x input and 2 x output lines for RS422;
- possibility to individually turn off power supply of each port;
- program switching of transfer direction for RS485

Module power supply: from carrier-board; Power: no more than 4 W;

When working with the driver in RS-485 mode in the reception port, in control register. "MCR" (modem control register) bit "RTS" is required to be installed as equal to 0, deactivating the transmitter by doing so. The more details on the programming principle of operation with the mezzanine is described in the document "User Manual for DIC551 system programmers" IMES.467444.068I12.

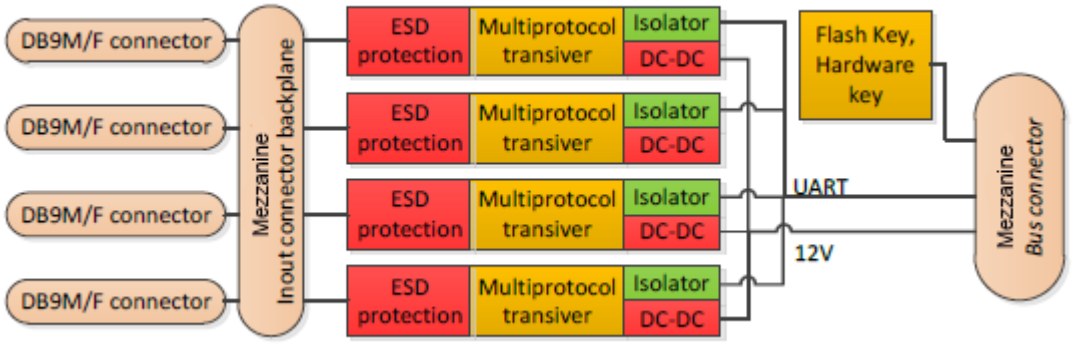


Figure 1.13 – Block diagram of MIC1002 mezzanine

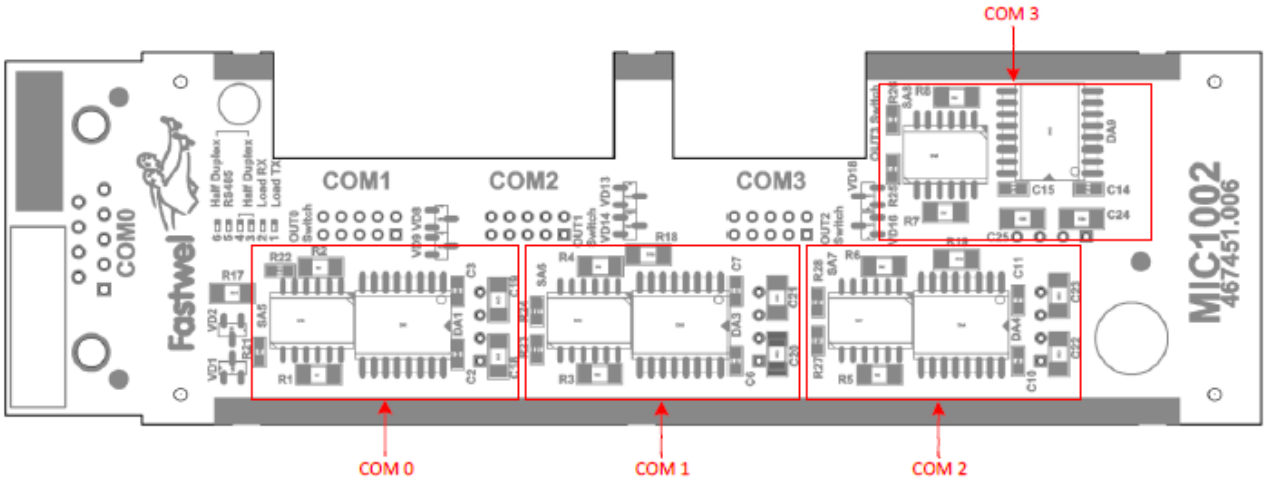


Figure 1.14 – External view of MIC1002 module from the TOP side and location of switching points

Table 1 Installation of micro-switches

No	Position	Value	Note
1	On	Connection of the terminating resistor for 120 Ohm from the transmitter's side	In RS-485/422 mode
2	On	Connection of the terminating resistor for 120 Ohm from the receiver's side	
3	On	Closure of Tx+ and Rx+	In RS-485/422 mode
4	On	Closure of Tx- and Rx-	
5	On	RS-485/422 mode	
	Off	RS-232 mode	In this case, 1-4 micro-switches are placed in "OFF" position
6	On	Reception prohibition	
	Off	Reception permission	

Note – micro-switch "ON" position corresponds to switched-on state

For connection over RS-232/485/422 interfaces, connectors DSUB9/M – XP6 (COM0) and IDC2-10R – XP3-XP5(COM1-COM3) are installed. COM1 – COM3 interfaces are routed to the additional 4HP strip, installed into the crate via IMES.685622.016 connectors. Strips and cables are included into the installation kit IMES.468911.003, supplied with MIC1002 mezzanine. Information on the relevant assignment of contacts is given in the table 2. The next figure shows a strip with the installed connectors.

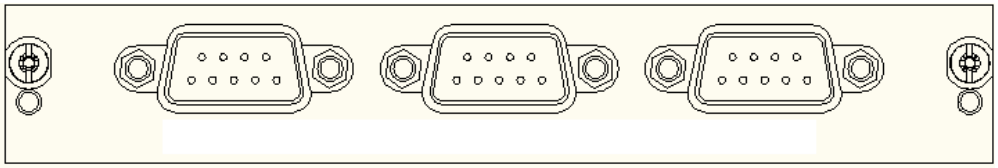


Table 2 Assignment of contacts of XP6, XP3 – XP5, COM1 – COM3 connector

Contact	Purpose		
	RS-232	RS-422	RS-485
1	DCD		
2	RX	RX–	
3	TX	TX+	D+
4	DTR	TX–	D-
5	GND		
6	DSR		
7	RTS		
8	CTS	RX+	
9	RI		
10	GND		

MIC1002 mezzanine is connected with the carrier-board via XP1. Tables 3 and 4 contain assignments of contacts. XP1 connector is used for data exchange between the carrier-board and mezzanine via UART interface. Additional XP2 connector is installed into MIC1002-02 mezzanine and is designed for the rear output of signals from mezzanine, it is used for duplicating signals from XP3-XP6 connectors, in this case XP6 connector "COM0" is not installed.

Table 3 Assignment of XP1 connector contacts

Contact	Value	Contact	Value	Contact	Value	Contact	Value
1	GND	17	RX(1)	33	RX(3)	49	NC
2	GND	18	TX(1)	34	TX(3)	50	NC
3	+3.3	19	nRTS(1)	35	nRTS(3)	51	NC
4	+3.3	20	nCTS(1)	36	nCTS(3)	52	NC
5	CS_ID	21	nDTR(1)	37	nDTR(3)	53	NC
6	CLK_ID	22	nDSR(1)	38	nDSR(3)	54	NC
7	MOSI_ID	23	nDCD(1)	39	nDCD(3)	55	NC
8	MISO_ID	24	nRI(1)	40	nRI(3)	56	NC
9	RX(0)	25	RX(2)	41	NC	57	NC
10	TX(0)	26	TX(2)	42	NC	58	NC
11	nRTS(0)	27	nRTS(2)	43	NC	59	NC
12	nCTS(0)	28	nCTS(2)	44	NC	60	NC
13	nDTR(0)	29	nDTR(2)	45	NC	61	+12
14	nDSR(0)	30	nDSR(2)	46	NC	62	+12
15	nDCD(0)	31	nDCD(2)	47	NC	63	GND
16	nRI(0)	32	nRI(2)	48	NC	64	GND

Table 4 Assignment of XP2 connector contacts

Contact	Value	Contact	Value	Contact	Value	Contact	Value
1	GND0	17	NC	33	NC	49	NC
2	RX/RX0-	18	NC	34	NC	50	NC
3	CTS/RX0+	19	GND1	35	GND2	51	GND3
4	GND0	20	RX/RX1-	36	RX/RX2-	52	RX/RX3-
5	TX/TX0+	21	CTS/RX1+	37	CTS/RX2+	53	CTS/RX3+
6	DTR/TX0-	22	GND1	38	GND2	54	GND3
7	GND0	23	TX/TX1+	39	TX/TX2+	55	TX/TX3+
8	DSR0	24	DTR/TX1-	40	DTR/TX2-	56	DTR/TX3-
9	RTS0	25	GND1	41	GND2	57	GND3
10	DCD0	26	DSR1	42	DSR2	58	DSR3
11	RI0	27	RTS1	43	RTS2	59	RTS3
12	NC	28	DCD1	44	DCD2	60	DCD3
13	NC	29	RI1	45	RI2	61	RI3
14	NC	30	NC	46	NC	62	NC
15	NC	31	NC	47	NC	63	NC
16	NC	32	NC	48	NC	64	NC

1.2.5.2 MIC1003 digital I/O mezzanine

The mezzanine is designed for input/output of 48 signals with logic levels CMOS 5V, contains protection against electrostatic discharge. Output data on contacts in the group is changing simultaneously, the latency time amounts to no more than 2.1 μS. Can be used for measuring signal frequency, receipt and delivery of serial code, conversion of codes, control of alphanumeric indicators, generation of control time diagrams.

The basic version of the module uses CPLD matrix and In-System Programmable (hereinafter referred to as the ISP) technology, which enable to change operation algorithm of the module directly within the system, without power shut-down, using special additional means. Connection with the carrier-board is carried out via a high-speed galvanic isolated serial port.

Mezzanine MIC1003-01 has a frontal output of signals via XP4 connector of Molex 0015922250 type. MIC1003-02 mezzanine has a rear output of signals via XP2 connector and carrier-board to the system block backplane. Position of SA1 switches determines connection with the pull-down or pull-up for 6 and 8 contact groups, see table 5.

Main features:

- 48 x channels of digital I/O with individual direction configuration;
- group galvanic isolation of channels 750V;
- protection of output signals against ESD;
- delivering and receipt of serial code (compatible with RS232 via protocol) over any channel;
- generation of interrupts when changing data at inputs;
- measurement of signal frequency (up to 2000 kHz) via any channel;
- programmable time interval for de-bouncing at inputs (de-bouncing).

Module power supply: from carrier-board; Power: no more than 4W;

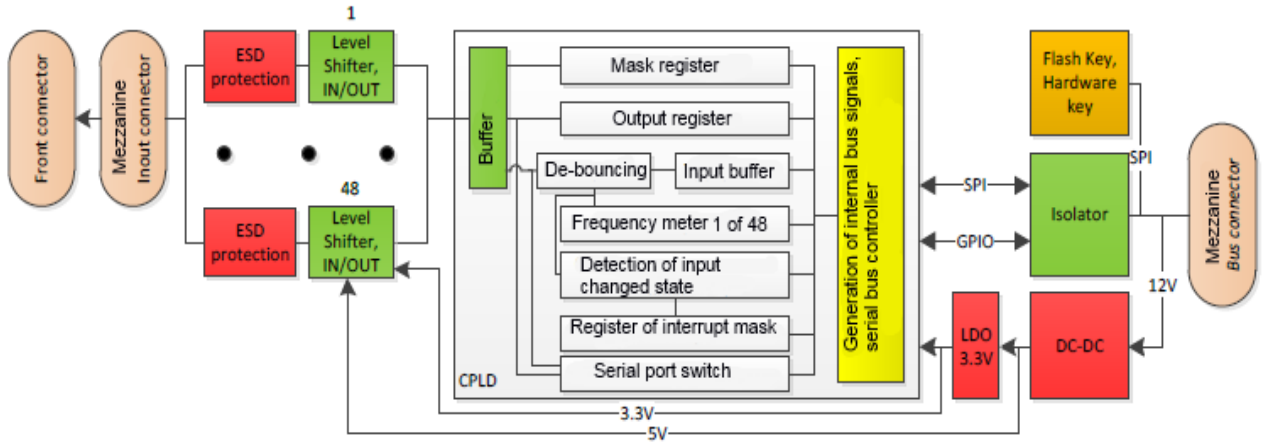


Figure 1.15 – Block diagram of MIC1003 mezzanine

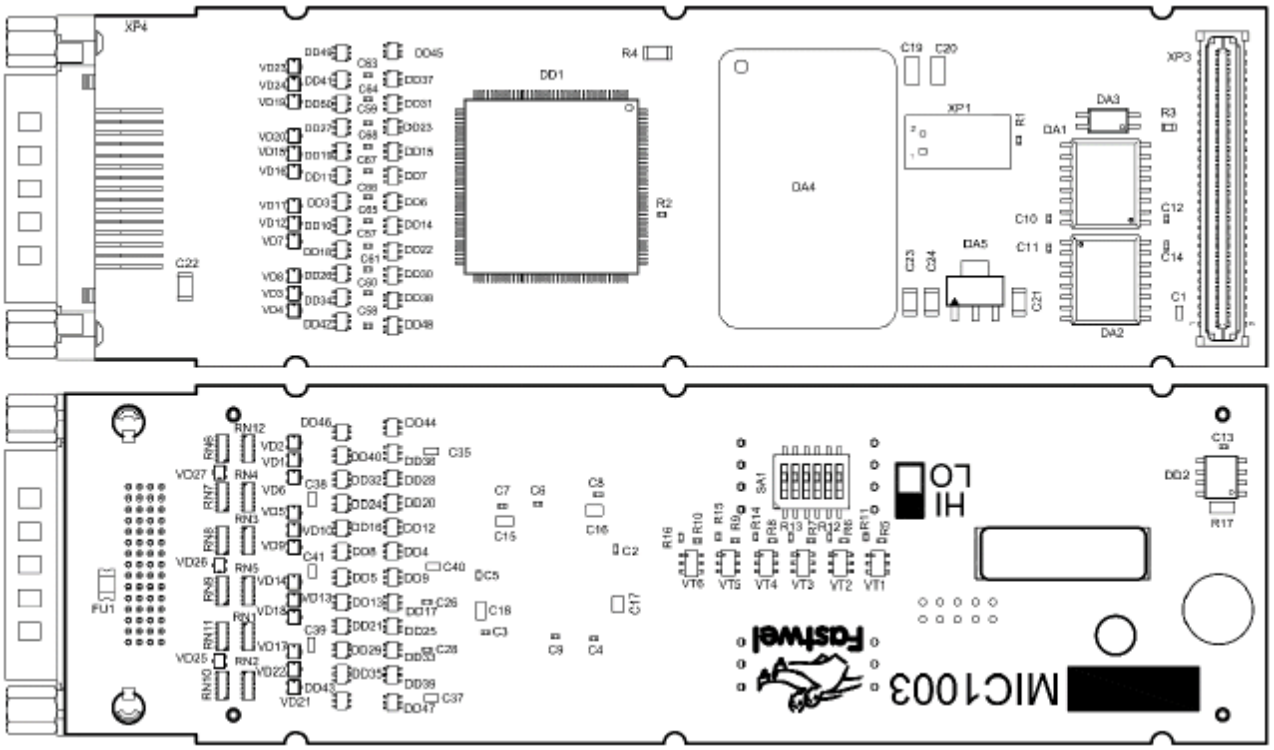


Figure 1.16 – External view of MIC1003 module

Table 5 Position of SA1 switches

SA1	Group of contacts	Pull-up	Pull-down
SA1.6	0 – 7	Hi	Lo
SA1.5	8 – 15	Hi	Lo
SA1.4	16 – 23	Hi	Lo
SA1.3	24 – 31	Hi	Lo
SA1.2	32 – 39	Hi	Lo
SA1.1	40 - 47	Hi	Lo

The module of providing mezzanine for use is described by two levels:

1. HAL module level of engagement (via board's driver) with devices on the carrier-board for provision of the communication channel with mezzanine and fulfillment of some additional functions.
2. Level of interaction of HAL module directly with mezzanine. Via "transparent" communications channels. This level enables full control of mezzanine functionalities. The more detailed information on the programming principle of operation is described in the "User Manual for DIC551 system programmers" document IMES.467444.068I12

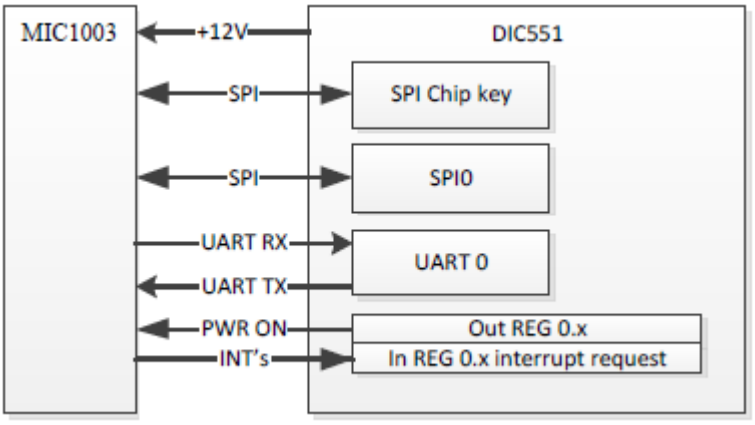


Figure 1.17 – Model of connection between mezzanine and carrier-board.

The carrier-board has the following mezzanine interaction capabilities:

1. Using SPI Chip Key interface to receive identification information from Chip Key memory chip, installed in the mezzanine.
2. Exchange data with the registers located on the mezzanine, via 32-bit SPI interface. Interface settings are fixed: 32 bit. In the 32-bit word: 24 bit data [23:0], 4 bit register address [31:28], bit [27] operation pointer: 1 - write, 0 – read, bits [26:24] unassigned (non-significant).
3. Connect receiver and UART transmitter to the mezzanine.
4. Fulfill a function of mezzanine activation (power reset) using one of register's I/O outputs of the carrier-board.
5. Receive interrupts from the mezzanine using one of the outputs of carrier-board's I/O register.

Mezzanine register model. Since mezzanine has 48 digital inputs and outputs and only 24 information bits can be sent simultaneously, all the mezzanine registers consist of the lower and upper parts. In this case the lower part is positioned at even addresses and the upper part - at odd addresses.

Table 6

+0	W\R	Output register (outputs 23 - 0)
+1	W\R	Output register (outputs 47 - 24)
The data are recorded to the output register, in case of reading operations the register contents will be deducted.		

Table 7

+2	W\R	Direction register (outputs 23 - 0)
+3	W\R	Direction register (outputs 47 - 24)
The value, recorded into the relevant bit: 0 – corresponds to the input, 1 – corresponds to the output of		

Table 8

+4	W	Interrupt enabling register (outputs 23 - 0)
+5	W	Interrupt enabling register (outputs 47 - 24)
The value recorded to the relevant bit, will be as follows: 0 – corresponds to the prohibition of interrupt generation when changing the state of this output, 1 – to the permission.		

Table 9

+4	R	Interrupt register (outputs 23 - 0)
+5	R	Interrupt register (outputs 47 - 24)
Value 1 during register reading means activation of the interrupt flag for this output, i.e. fulfills condition for interrupt to appear at this output. Register reading resets the interrupt flag.		

Table 10

+6	W\R	Interrupts control register (outputs 23 - 0)
+7	W\R	Interrupts control register (outputs 47 - 24)
The value recorded to the relevant bit, will be as follows: 0 – corresponds to interrupt generation along the positive edge at output, 1 – along the negative edge.		

Table 11

+8	W\R	Register for connection to UART
Value recorded to 5:0 bits (from 1 to 48) indicates the output number to which UART output is connected, value in bits 11:6 points at the output number to which UART input is connected. Value 0 in both cases disconnects UART from all the outputs.		

Table 12

+9	W\R	Register of control and state of the frequency meter and de-bouncing unit
Value recorded to 5:0 bits (from 1 to 48) indicates the output number to which the frequency meter is connected, 0 indicates that the frequency meter is disconnected from the inputs. Bit 6 in 1 permits counting to the frequency meter, 0 - resets the frequency meter. Bit 7 in 1 permits interrupt generation from the frequency meter. Reading of bit 8,1 indicates the readiness of the frequency meter to read the data, 0 - that it is not ready to read the data (counting is running or there is no signal) Bits 11:9 enable to choose the clock frequency for the frequency meter. Bits 15:12 set the number of measured periods of averaging input frequency, from which an arithmetic mean value will be derived. Bits 18:16 set the length of operation, temporary sensitivity of the de-bouncing unit.		

Table 13

+a	W\R	De-bouncing control register (outputs 23 - 0)
+b	W\R	De-bouncing control register (outputs 47 - 24)
Recording 1 to the relevant bit activates the de-bouncing suppression unit into the input circuit of the output.		

Table 14

+c	R	Input data register (outputs 23 - 0)
+d	R	Input data register (outputs 47 - 24)
Reading these registers shows the state of mezzanine outputs.		

Connection of mezzanine to the carrier-board.

For mezzanine and carrier-board connection, the following interfaces will be used:

1. Mezzanine is controlled via SPI0 interface with CS0. Settings SPI sending 32 bit, DIV = 3, CS0, Rx_neg = 1, Tx_neg = 1, Lsb = 0, ASS = 1, Enbl_clk= 1, Properties selection register = 1.

2. Data transfer via the 2-wire RS232-TTL interface is carried out via UART0. Only data receipt and transmission lines are used.
3. Mezzanine sends data from the frequency meter input to the CLK input and GATE of the counter 2, located on the carrier, this makes it possible to measure the frequency, as well as length and period of signal passing. Switching between measurement types is performed by software.
4. Configuration data are coming from non-volatile memory, located on the mezzanine, using SPI interface.

Interfaces 1 - 3 have galvanic isolation, with isolation voltage 750V.

With the use of SA1 it is possible to switch the pull-down of output pins, in groups by 8 contacts, between the earth and power supply voltage, the value of the pull-down resistance amounts to 10 kOhm. SA1.6 switch is responsible for outputs from 7 to 0, and SA1.1 is responsible for outputs from 47 to 40 correspondingly, according to the table 5.

All the external outputs of the mezzanine are equipped with ESD protection and by software can individually change the input-output direction, after reset all the outputs will be operating at input.

The combined interrupt from all the sources is transferred to the output 2 of port #2 (port2.2), for determination of the interrupt source it is required to deduct registers +4 and +5, as well as +9, if operation of the frequency meter is permitted.

When installing the logic value 1 at the output port2.0 on the board, CPLD mezzanine will be placed in the programming mode and loading of the software code in CPLD will be possible, by default this port **should be compulsory installed into 0**.

Activation/deactivation of mezzanine is carried out by way of supplying 12V from the relevant channel of the carrier-board.

1.2.5.3 MIC1004 mezzanine of current loop interfaces

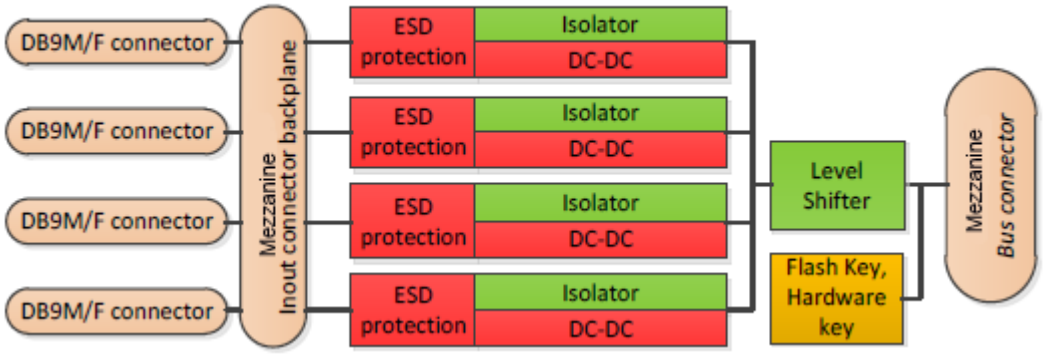


Figure 1.18 – Block diagram of MIC1004 mezzanine

The mezzanine is designed for I/O operations via 4 individual galvanic isolated serial ports of "current loop" type and represents the board for conversion of signal levels from UART, located on the carrier-board, into signal levels corresponding to the "current loop" standard.. Switching ports of Master-Slave type and 2-4 wire communications line is carried out with the use of micro-switches.

Main features:

- 4 x channels of current loop ports;
- galvanic isolation of channels, 750V;
- protection of output signals against ESD;
- possibility to individually turn off power supply of each port;
- operation on 2 - and 4 - wire lines;

operation in the master - slave mode;
Power to the module is supplied from the carrier-board;
Power: no more than 5W;

Figure 1.19 shows external view of the MIC1004 module from the TOP side and location of switching points

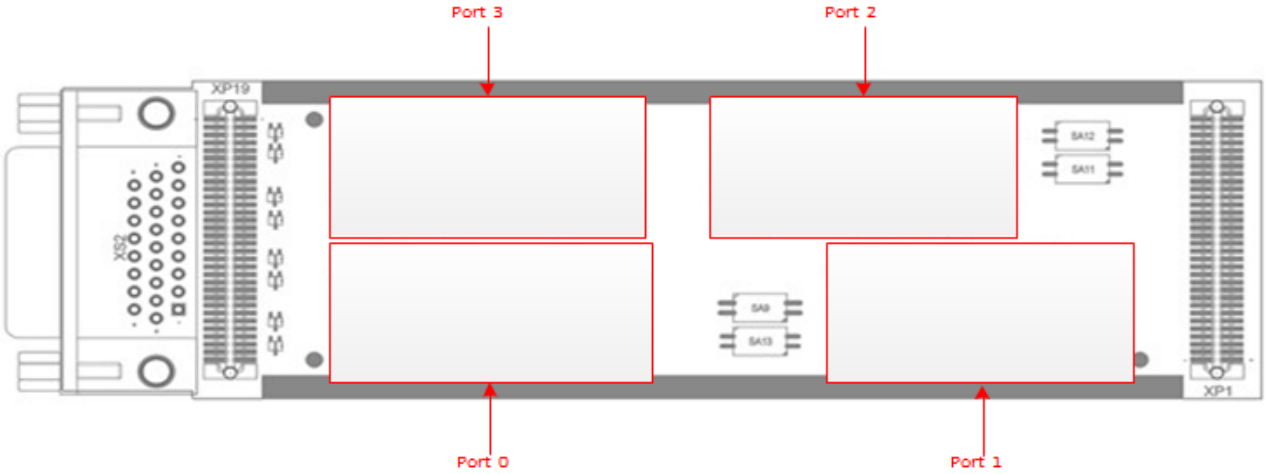


Figure 1.19 – External view of the MIC1004 module from the TOP side

The mezzanine is designed for I/O operations via 4 individual galvanic isolated serial ports of "current loop" type and represents the board for conversion of signal levels from UART, located on the carrier-board, into signal levels corresponding to the "current loop" standard. The more detailed information on the programming principle of operation is described in the "User Manual for DIC551 system programmers" document IMES.467444.068I12. Switching of "master-slave" ports and 2- or 4-wire communications line can be performed via jumpers and micro-switches.

Jumpers at XP7-XP14 connectors set transmitter's and receiver's type, depending on the availability of the current source in the circuit: active or passive. Table 15 demonstrates possible options. If active type was chosen, the relevant micro-switches SA9,11,12,13 should be set to "ON" position. Table 16 has possible "ON" position values.

Using jumpers on XP15-XP18 connectors it is possible to close Tx- and Rx+ signal lines corresponding to the port, for full-duplex mode.

Table 15 Options for transmitter and receiver connection

Connector	Contacts	Value
XP7, XP9, XP11, XP13	1-2	Passive transmitter
	2-3	Active transmitter
XP8, XP10, XP12, XP14	1-2	Passive receiver
	2-3	Active receiver

Table 16 Position of micro-switches SA9, SA11, SA12, SA13

Switch	Contacts	Port number	Value
SA9	1	0	Active transmitter
	2		Active receiver
SA11	1	1	Active transmitter
	2		Active receiver
SA12	1	2	Active transmitter
	2		Active receiver
SA13	1	3	Active transmitter

	2		Active receiver

For external (front) connection of the current loop interfaces, the MIC1004-01 board is equipped with XS2 connector (DSUB26S). If the rear signal output is used (via XP19 connector, then to the carrier-board and to the backplane of the system unit) of current loop interface, the board MIC1004-02 should be used.

Table 17 demonstrates contact values.

Contact	Value	Contact	Value
1	Tx0+	14	
2		15	Rx2+
3	Tx1+	16	
4		17	Tx3-
5	Tx2+	18	Rx3+
6	Tx2-	19	Rx0-
7		20	
8	Tx3+	21	Rx1+
9		22	Rx1-
10	Tx0-	23	
11	RX0+	24	Rx2-
12		25	
13	Tx1-	26	Rx3-

With MIC1004 mezzanine carrier-board it is connected via XP1 (or XP1, XP19 for MIC1004-02). Tables 18 and 19 contain assignments of contacts. XP1 connector is used for data exchange between the carrier-board and mezzanine via UART interface. XP19 connector is used for duplicating signals from XS2.

Data can be transferred between devices with 3 possible port configurations: unidirectional, half-duplex or full-duplex transmission/receipt in active or passive modes. Figures 1.20, 1.21 and 1.22 demonstrate connection options.

Table 18 Assignment of XP1 connector contacts

Contact	Value	Contact	Value	Contact	Value	Contact	Value
1	GND	17	RX1	33	RX3	49	NC
2	GND	18	TX1	34	TX3	50	NC
3	+3.3	19	NC	35	NC	51	NC
4	+3.3	20	NC	36	NC	52	NC
5	CS_ID	21	NC	37	NC	53	NC
6	CLK_ID	22	NC	38	NC	54	NC
7	MOSI_ID	23	NC	39	NC	55	NC
8	MISO_ID	24	NC	40	NC	56	NC
9	RX0	25	RX2	41	NC	57	NC
10	TX0	26	TX2	42	NC	58	NC
11	NC	27	NC	43	NC	59	+3.3

12	NC	28	NC	44	NC	60	+3.3
13	NC	29	NC	45	NC	61	+12
14	NC	30	NC	46	NC	62	+12
15	NC	31	NC	47	NC	63	GND
16	NC	32	NC	48	NC	64	GND

Table 19 Assignment of XP19 connector contacts

Contact	Value	Contact	Value	Contact	Value	Contact	Value
1	NC	17	NC	33	NC	49	NC
2	NC	18	NC	34	NC	50	NC
3	RV+(3)	19	NC	35	NC	51	NC
4	NC	20	NC	36	NC	52	NC
5	Rv-(3)	21	Rv+(2)	37	Rv+(1)	53	Rv+(0)
6	NC	22	NC	38	NC	54	NC
7	Tv+(3)	23	Rv-(2)	39	Rv-(1)	55	Rv-(0)
8	NC	24	NC	40	NC	56	NC
9	Tv-(3)	25	Tv+(2)	41	Tv+(1)	57	Tv+(0)
10	NC	26	NC	42	NC	58	NC
11	NC	27	Tv-(2)	43	Tv-(1)	59	Tv-(0)
12	NC	28	NC	44	NC	60	NC
13	NC	29	NC	45	NC	61	NC
14	NC	30	NC	46	NC	62	NC
15	NC	31	NC	47	NC	63	NC
16	NC	32	NC	48	NC	64	NC

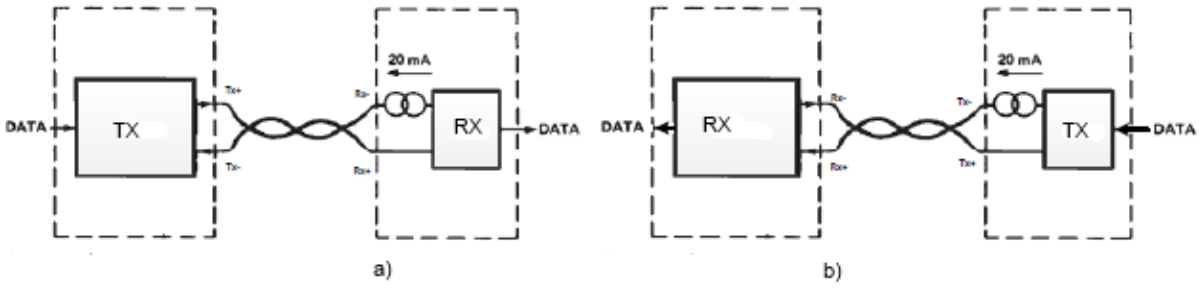


Figure 1.20 – Unidirectional connection: a) active receiver; b) active transmitter

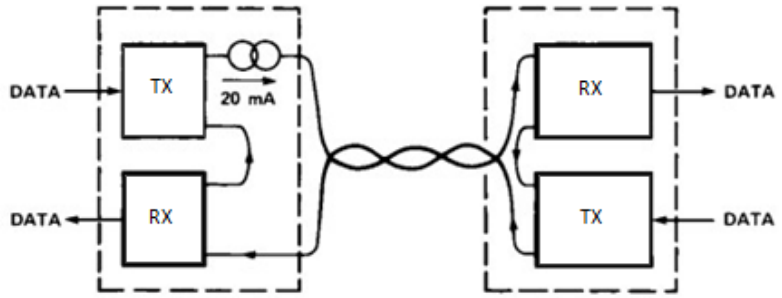


Figure 1.21 – Full-duplex connection

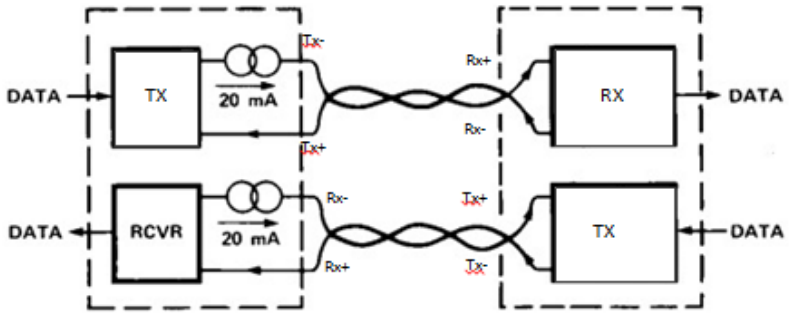


Figure 1.22 – Full-duplex connection

1.2.6 Delivery checklist

Standard delivery checklist of the carrier-board:

- DIC551 carrier-board or DIC551RC carrier-board;
- Packaging;

Standard delivery checklist for mezzanine MIC1002:

- Mezzanine MIC1002;
- Installation kit;
- Packaging;

Standard delivery checklist fir mezzanine MIC1003, MIC1004:

- Mezzanine MIC1003;
- Packaging;

Evaluation KIT for mezzanine developers (DIC551-03):

- Carrier-board DIC551-01;
- Mezzanine M551T;
- Packaging;

Note – If any of the components from the delivery checklist is not present or has external mechanical damages, please contact the official distributor that sold you this module. Retain the original antistatic and consumer packages of the module till the end of the guarantee service life period.

1.3 DESCRIPTION OF MEZZANINE CONNECTORS AND PORTS OF CARRIER-BOARD

1.3.1 Connector for mezzanines

1. High-density connector for the use in low-current mezzanines. Contains 50 contacts with maximum load current of 1A and voltage of 40V per contact. Isolation voltage 500V AC Molex 0015922250.

Figure 1.23 - High-density connector for the use in low-current mezzanines.

2. Low-density connector for the connection of power channels of DHR 26F mezzanine.

Contains 26 contacts with maximum load current of 2A (current limit 5A) and voltage of 100V per contact. Isolation voltage 1000V AC.

1.3.2 Inter-board connections of mezzanine and carrier-board

Inter-board connections of the carrier-board and mezzanines are fulfilled by connectors of 71436 and 71439 (Molex) type.

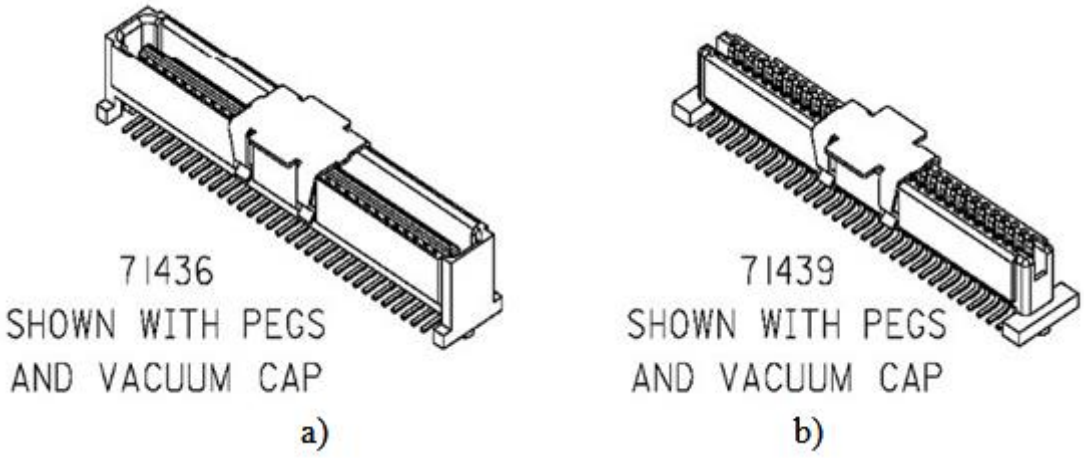


Figure 1.24 – Connectors MOLEX 71436 (a) and 71439 (b)

Contains 64 contacts with maximum load current of 0.5A (limit current 1A) and isolation voltage of 250V AC per contact.

Inter-board connections of the carrier-board and mezzanines are fulfilled by 4 XS1… XS4 connectors (Figure 1.24, a, b). XS3 and XS4 have direct connection with XP5 and XP4 of the module. XS1 and XS2 connectors are identical and are designed for input and output of signals of the supported interfaces and power supply of the mezzanines.

Table20 Assignment of XS1, XS2 (MOLEX 71439) connectors' contacts

No	Name pin	Parallel port	UART 16550	SPI	32 bit Wishbone bus
1	GND	Signal ground			
2	GND				
3	+3V3	Power supply of interfaces via the fuse for 300 mA. Is used ONLY for power supply of identification memory and level converters.			
4	+3V3				
5	CS_ID	Outputs for the connection of mezzanine identification memory, operating via SPI interface. Identification of module presence is carried out during module start by determining a high level at SO_ID output with the connected mezzanine, and low level - when there is no mezzanine.			
6	CLK_ID				
7	SI_ID				
8	SO_ID				
9	Port 0.0	IO Reg0.0↔	RX0←	SPORT 0 CLK_TX↔	D0↔
10	Port 0.1	IO Reg0.1↔	TX0→	SPORT 0 FRAME_TX↔	D1↔
11	Port 0.2	IO Reg0.2↔	nRTS0→	SPORT 0 TX →	D2↔
12	Port 0.3	IO Reg0.3↔	nCTS0←	SPORT 0 CLK_RX↔	D3↔
13	Port 0.4	IO Reg0.4↔	nDTR0→	SPORT 0 FRAME_RX↔	D4↔
14	Port 0.5	IO Reg0.5↔	nDSR0←	SPORT 0 RX←	D5↔
15	Port 0.6	IO Reg0.6↔	nDCD0←	SPORT 0 Limp→	D6↔
16	Port 0.7	IO Reg0.7↔	nRI0←		D7↔
17	Port 0.8	IO Reg0.8↔	RX1←	SPORT 1 CLK_TX↔	D8↔
18	Port 0.9	IO Reg0.9↔	TX1→	SPORT 1 FRAME_TX↔	D9↔
19	Port 0.10	IO Reg0.10↔	nRTS1→	SPORT 1 TX →	D10↔
20	Port 0.11	IO Reg0.11↔	nCTS1←	SPORT 1 CLK_RX↔	D11↔
21	Port 0.12	IO Reg0.12↔	nDTR1→	SPORT 1 FRAME_RX↔	D12↔
22	Port 0.13	IO Reg0.13↔	nDSR1←	SPORT 1 RX←	D13↔
23	Port 0.14	IO Reg0.14↔	nDCD1←	SPORT 1 Limp→	D14↔
24	Port 0.15	IO Reg1.15↔	nRI1←		D15↔
25	Port 1.0	IO Reg1.0↔	RX2←	SPI 0 MOSI→	D16↔
26	Port 1.1	IO Reg1.1↔	TX2→	SPI 0 MISO←	D17↔
27	Port 1.2	IO Reg1.2↔	nRTS2→	SPI 0 CLK →	D18↔
28	Port 1.3	IO Reg1.3↔	nCTS2←	SPI 0 CS0→	D19↔
29	Port 1.4	IO Reg1.4↔	nDTR2→	SPI 0 CS1→	D20↔
30	Port 1.5	IO Reg1.5↔	nDSR2←	SPI 0 CS2→	D21↔
31	Port 1.6	IO Reg1.6↔	nDCD2←	SPI 0 CS3→	D22↔
32	Port 1.7	IO Reg1.7↔	nRI2←	SPI 0 CS4→	D23↔
33	Port 1.8	IO Reg1.8↔	RX3←	SPI 1 MOSI→	D24↔
34	Port 1.9	IO Reg1.9↔	TX3→	SPI 1 MISO←	D25↔
35	Port 1.10	IO Reg1.10↔	nRTS3→	SPI 1 CLK →	D26↔
36	Port 1.11	IO Reg1.11↔	nCTS3	SPI 1 CS0→	D27↔
37	Port 1.12	IO Reg1.12↔	nDTR3→	SPI 1 CS1→	D28↔
38	Port 1.13	IO Reg1.13↔	nDSR3←	SPI 1 CS2→	D29↔
39	Port 1.14	IO Reg1.14↔	nDCD3←	SPI 1 CS3→	D30↔
40	Port 1.15	IO Reg1.15↔	nRI3←	SPI 1 CS4→	D31↔
41	Port 2.0	IO Reg2.0↔		SPI 2 MOSI→	A0→
42	Port 2.1	IO Reg2.1↔		SPI 2 MISO←	A1→
43	Port 2.2	IO Reg2.2↔		SPI 2 CLK →	A2→

44	Port 2.3	IO Reg2.3↔		SPI 2 CS0→	A3→
45	Port 2.4	IO Reg2.4↔		SPI 2 CS1→	A4→
46	Port 2.5	IO Reg2.5↔		SPI 2 CS2→	A5→
47	Port 2.6	IO Reg2.6↔		SPI 2 CS3→	A6→
48	Port 2.7	IO Reg2.7↔	Timer0 OUT→	SPI 2 CS4→	A7→
49	Port 2.8	IO Reg2.8↔	Timer0 CLK←	SPI 3 MOSI→	SEL→
50	Port 2.9	IO Reg2.9↔	Timer0 GATE←	SPI 3 MISO←	WE→
51	Port 2.10	IO Reg2.10↔	Timer2 OUT→	SPI 3 CLK →	CLK→
52	Port 2.11	IO Reg2.11↔	Timer2 CLK←	SPI 3 CS0→	STB→
53	Port 2.12	IO Reg2.12↔	Timer2 GATE←	SPI 3 CS1→	ACK←
54	Port 2.13	IO Reg2.13↔	Timer1 OUT→	SPI 3 CS2→	CYC→
55	Port 2.14	IO Reg2.14↔	Timer1 CLK←	SPI 3 CS3→	INT0←
56	Port 2.15	IO Reg2.15↔	Timer1 GATE←	SPI 3 CS4→	
57	Strb0	Strb0 OUT – output of clock counter 0 of the carrier-board →			
58	Strb1	Strb1 OUT – output of clock counter 1 of the carrier-board →			
59	+3V3	Mezzanine power supply			
60	+3V3				
61	+12V	Power supply of power converters for galvanic isolated interfaces			
62	+12V				
63	GND	Power converter's ground			
64	GND				

Table21 Assignment of XS3, XS4 (MOLEX 71439) connectors' contacts

XS3		XS4	
Name pin	**Contact number**	**Name pin**	**Contact number**
IO1	P1_1	IO1	P1_1
IO2	P1_2	IO2	P1_2
IO3	P1_3	IO3	P1_3
IO4	P1_4	IO4	P1_4
IO5	P1_5	IO5	P1_5
IO6	P1_6	IO6	P1_6
IO7	P1_7	IO7	P1_7
IO8	P1_8	IO8	P1_8
IO9	P1_9	IO9	P1_9
IO10	P1_10	IO10	P1_10
IO11	P1_11	IO11	P1_11
IO12	P1_12	IO12	P1_12
IO13	P1_13	IO13	P1_13
IO14	P1_14	IO14	P1_14

NC	P1_15	NC	P1_15
NC	P1_16	NC	P1_16
NC	P1_17	NC	P1_17
NC	P1_18	NC	P1_18
IO15	P1_19	IO15	P1_19
IO16	P1_20	IO16	P1_20
IO17	P1_21	IO17	P1_21
IO18	P1_22	IO18	P1_22
IO19	P1_23	IO19	P1_23
IO20	P1_24	IO20	P1_24
IO21	P1_25	IO21	P1_25
IO22	P1_26	IO22	P1_26
IO23	P1_27	IO23	P1_27
IO24	P1_28	IO24	P1_28
IO25	P1_29	IO25	P1_29
IO26	P1_30	IO26	P1_30
NC	P1_31	NC	P1_31
NC	P1_32	NC	P1_32
NC	P1_33	NC	P1_33
NC	P1_34	NC	P1_34
IO27	P1_35	IO27	P1_35
IO28	P1_36	IO28	P1_36
IO29	P1_37	IO29	P1_37
IO30	P1_38	IO30	P1_38
IO31	P1_39	IO31	P1_39
IO32	P1_40	IO32	P1_40
IO33	P1_41	IO33	P1_41
IO34	P1_42	IO34	P1_42
IO35	P1_43	IO35	P1_43
IO36	P1_44	IO36	P1_44
IO37	P1_45	IO37	P1_45
IO38	P1_46	IO38	P1_46
NC	P1_47	NC	P1_47
NC	P1_48	NC	P1_48
NC	P1_49	NC	P1_49
NC	P1_50	NC	P1_50
IO39	P1_51	IO39	P1_51
IO40	P1_52	IO40	P1_52
IO41	P1_53	IO41	P1_53
IO42	P1_54	IO42	P1_54
IO43	P1_55	IO43	P1_55
IO44	P1_56	IO44	P1_56
IO45	P1_57	IO45	P1_57
IO46	P1_58	IO46	P1_58
IO47	P1_59	IO47	P1_59
IO48	P1_60	IO48	P1_60
IO49	P1_61	IO49	P1_61

IO50	P1_62	IO50	P1_62
IO51	P1_63	IO51	P1_63
IO52	P1_64	IO52	P1_64

Table 22 Assignment of XP1 (10052825-101LF) connector contacts

Name pin	Contact number	Name pin	Contact number
IPMB_PWR	A1	GND	A4
STNDBY	B1	1_USB2+	B4
GND	C1	1_USB2-	C4
+12V	D1	GND	D4
+12V	E1	PE_CLKIN+	E4
GND	F1	PE_CLKIN-	F4
+12V	G1	GND	G4
+12V	H1	1_SATA_Tx+	H4
GND	I1	1_SATA_Tx-	I4
+12V	J1	GND	J4
+12V	K1	1_SATA_Rx+	K4
GND	L1	1_SATA_Rx-	L4
GND	A2	1_PE_Tx00+	A5
IPMB_SCL	B2	1_PE_Tx00-	B5
IPMB_SDA	C2	GND	C5
GND	D2	1_PE_Rx00+	D5
RSRV	E2	1_PE_Rx00-	E5
RSRV	F2	GND	F5
GND	G2	1_PE_Tx01+	G5
RST_IN#	H2	1_PE_Tx01-	H5
WAKE_OUT#	I2	GND	I5
GND	J2	1_PE_Rx01+	J5
PCIE_EN#	K2	1_PE_Rx01-	K5
SYSEN#	L2	GND	L5
1_USB3_Tx+	A3	GND	A6
1_USB3_Tx-	B3	1_PE_Tx02+	B6
GA0	C3	1_PE_Tx02-	C6
1_USB3_Rx+	D3	GND	D6
1_USB3_Rx-	E3	1_PE_Rx02+	E6
GA1	F3	1_PE_Rx02-	F6
SATA_SDI	G3	GND	G6
SATA_SDO	H3	1_PE_Tx03+	H6
GA2	I3	1_PE_Tx03-	I6
SATA_SCL	J3	GND	J6
SATA_SL	K3	1_PE_Rx03+	K6
GA3	L3	1_PE_Rx03-	L6

Table 23 Assignment of XP4 (10052837-101LF) connector contacts

Name pin	Contact number	Name pin	Contact number
IO1	A1	IO33	A5
IO2	B1	IO34	B5
GND	C1	GND	C5
IO3	D1	IO35	D5
IO4	E1	IO36	E5
GND	F1	GND	F5
IO5	G1	IO37	G5
IO6	H1	IO38	H5
GND	I1	GND	I5
IO7	J1	IO39	J5
IO8	K1	IO40	K5
GND	L1	GND	L5
GND	A2	GND	A6
IO9	B2	IO41	B6
IO10	C2	IO42	C6
GND	D2	GND	D6
IO11	E2	IO43	E6
IO12	F2	IO44	F6
GND	G2	GND	G6
IO13	H2	IO45	H6
IO14	I2	IO46	I6
GND	J2	GND	J6
IO15	K2	IO47	K6
IO16	L2	IO48	L6
IO17	A3	IO49	A7
IO18	B3	IO50	B7
GND	C3	GND	C7
IO19	D3	IO51	D7
IO20	E3	IO52	E7
GND	F3	GND	F7
IO21	G3	IO53	G7
IO22	H3	IO54	H7
GND	I3	GND	I7
IO23	J3	IO55	J7
IO24	K3	IO56	K7
GND	L3	GND	L7
GND	A4	GND	A8
IO25	B4	IO57	B8
IO26	C4	IO58	C8
GND	D4	GND	D8
IO27	E4	IO59	E8
IO28	F4	IO60	F8
GND	G4	GND	G8

IO29	H4	IO61	H8
IO30	I4	IO62	I8
GND	J4	GND	J8
IO31	K4	IO63	K8
IO32	L4	IO64	L8

Table 24 Assignment of XP5 (10052837-101LF) connector contacts

Name pin	Contact number	Name pin	Contact number
IO1	A1	IO33	A5
IO2	B1	IO34	B5
GND	C1	GND	C5
IO3	D1	IO35	D5
IO4	E1	IO36	E5
GND	F1	GND	F5
IO5	G1	IO37	G5
IO6	H1	IO38	H5
GND	I1	GND	I5
IO7	J1	IO39	J5
IO8	K1	IO40	K5
GND	L1	GND	L5
GND	A2	GND	A6
IO9	B2	IO41	B6
IO10	C2	IO42	C6
GND	D2	GND	D6
IO11	E2	IO43	E6
IO12	F2	IO44	F6
GND	G2	GND	G6
IO13	H2	IO45	H6
IO14	I2	IO46	I6
GND	J2	GND	J6
IO15	K2	IO47	K6
IO16	L2	IO48	L6
IO17	A3	IO49	A7
IO18	B3	IO50	B7
GND	C3	GND	C7
IO19	D3	IO51	D7
IO20	E3	IO52	E7
GND	F3	GND	F7
IO21	G3	IO53	G7
IO22	H3	IO54	H7
GND	I3	GND	I7
IO23	J3	IO55	J7
IO24	K3	IO56	K7
GND	L3	GND	L7

GND	A4	GND	A8
IO25	B4	IO57	B8
IO26	C4	IO58	C8
GND	D4	GND	D8
IO27	E4	IO59	E8
IO28	F4	IO60	F8
GND	G4	GND	G8
IO29	H4	IO61	H8
IO30	I4	IO62	I8
GND	J4	GND	J8
IO31	K4	IO63	K8
IO32	L4	IO64	L8

1.3.3 SPORT serial port of the carrier-board

SPORT serial port Represents 32 bit configurable multi-speed serial port with support of DMA, TDM and I2S.

The port ensures I/O interface with various peripheral devices. Each serial port (Read, Write) has its own control registers and data buffers. Possibility of using various options of clock and frame synchronization makes it possible to support a range of data exchange protocols via serial port and ensures hardware interface with many data converters and industrial standard codecs.

The port can be operating on the clock frequency up to 32 MHz, supporting a data exchange rate of
32 Mb/sec. Possibility of independent receipt and transmission of data ensures significant flexibility when arranging communications lines. Data from serial port can be automatically transferred to the internal memory and from the internal memory using the DMA – Direct Memory Access mode. Each serial port supports multichannel mode with TDM – Time Division Multiplexing.

Signals of clock and frame synchronization of serial port can be generated inside the port or can be received from an external source. Serial port can operate with the word length from 3 to 32 bits and with various data transfer formats: data transfer starts from the most significant bit or least significant bit.

The serial port has the following features:

- independent receipt and transmission functions;
- transmission of data words with a length up to 32 bits, starting with most significant bits or least significant bits;
- double data buffering – each part of the serial port (both receiving and transmitting parts) has data register and shift register; double buffering reduces the time required for serial port servicing;
- signals of clock and frame synchronization can be generated inside the port in the wide frequency range or received from an external source;
- transmissions of single data words to the internal memory or from it, controlled by interrupts _;
- transmission over DMA to the internal memory and from it – each SPORT can automatically receive and/or transmit an entire data unit;
- chain of DMA operations for transmitting several data units;
- multichannel mode with time division of channels – each SPORT
can selectively receive data from the flow of serially forwarded bits with the use of time division of channels; this mode is good for T1 interfaces.

1.3.4 Serial port SPI of the carrier-board

SPI serial port Represents 32 bit configurable multi-speed serial port with support of SPI 0 and SPI 3 protocol. The serial port has the following features:

- Full-duplex data transfer;
- length of the transferred word is from 3 to 32 bit;
- transmission can start from the most significant or the least significant bits;
- 4 x device select lines;
- possibility of using interrupt during transmission/receipt of data;
- transmission/receipt of data by drop/rise of the clock signal;
- clock frequency up to 32M.

1.3.5 Parallel port of the carrier-board

Represents 16-bit parallel port with a random register access to input-output, without the use of FIFO. The serial port has the following features:

- Port bit capacity: 16 bits;
- separate configuration of the port bits to I/O;
- hardware pulse shaper, connected to each bit of the port;
- generation of interrupts when changing the state of the port's input data;

1.3.6 Timer of carrier-board

Represents a modified timer of 8254 type. The timer has the following features:

- Clock frequency – 20 MHz;
- maximum external clock frequency: 32 MHz;
- Timer bit capacity: 32 bits;
- operating modes 0 – 5 are similar to the modes of 8254 timer;
- access to registers: 32-bit;
- possibility of timer's external triggering;
- timer cascading possibility;
- availability of two 32-bit frequency dividers for generating pulses

1.3.7 UART 16550A of the carrier-board

Software and hardware simulation of 16550A chip functionalities. Additional information is available at: https://en.wikipedia.org/wiki/16550_UART

1.3.8 Carrier-board mezzanine identification interface

Represents a microprogram automation for automatic readout of configuration information on the installed mezzanine over SPI protocol, when feeding power to mezzanine. For reading purposes the information is available in the relevant memory bank of the carrier-board and is used for configuring 3.3.3 – 3.3.6 interfaces for operation with a particular mezzanine. There is also an interface of random access to identification memory chip, designed for memory programming under manufacturing cycle conditions, as well as possibility of access to specific data of a particular mezzanine, e.g. calibration constants.

1.3.9 Register card of the carrier-board

1.3.9.1 General structure of DIC551 (DIC551RC) mezzanine carrier-board

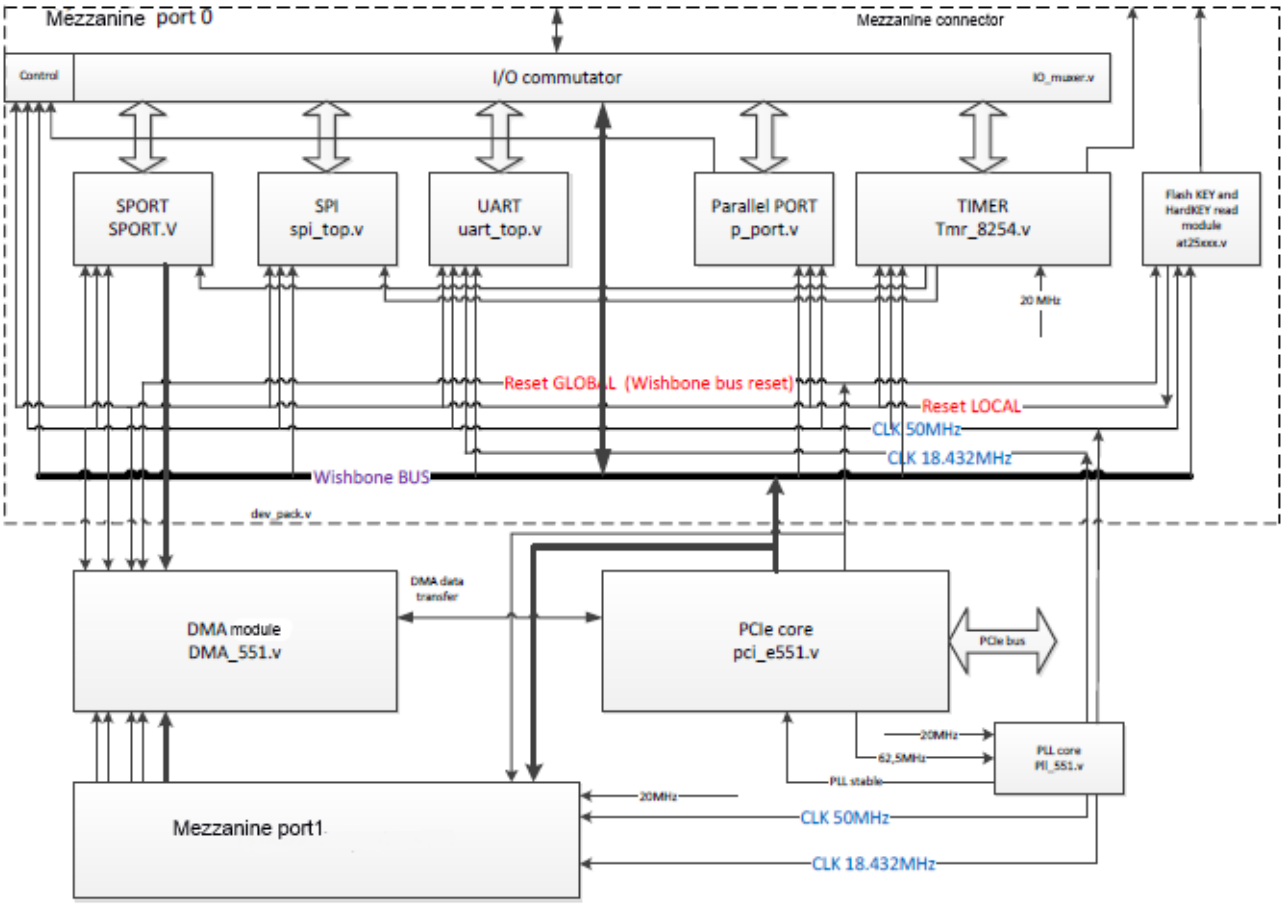


Figure 1.25 General structure of DIC551 (DIC551RC) mezzanine carrier-board

Module I/O space is shaped by 4x register banks: 2x register banks of mezzanine control ports (mezzanine port 0 & 1) – bank 0 and 1, port of state and control of memory direct access unit (DMA module) – bank 2, registers of service bus information PCIe (pci_e551.v) - hidden to the user. Parallel Wishbone bus was used as the internal inter-modular FPGA bus of the device. Since PCI supports only one interrupt to the device (on the bus), interrupts from all I/O devices are combined by logical "AND". Interrupt source is detected using software tools by sequential reading of state registers of I/O devices located in FPGA.

Device clocking is carried out by PCIe system bus (62.5 MHz) and highly-stable generator with low jitter, with a frequency of 20 MHz.

Table 25

Name	Parallel port	UART and	SPI and SPORT	32 bit Wishbone bus
	Device 0	*Device 1*	*Device 2*	*Device 3*
Port 0.0	IO Reg0.0↔	RX0←	SPORT 0 CLK_TX↔	D0↔
Port 0.1	IO Reg0.1↔	TX0→	SPORT 0 FRAME_TX	D1↔
Port 0.2	IO Reg0.2↔	nRTS0→	SPORT 0 TX →	D2↔

Name pin	Parallel port	UART and Timer	SPI and SPORT	32 bit Wishbone bus
Port 0.3	IO Reg0.3↔	nCTS0←	SPORT 0 CLK_RX↔	D3↔
Port 0.4	IO Reg0.4↔	nDTR0→	SPORT 0 FRAME_RX↔	D4↔
Port 0.5	IO Reg0.5↔	nDSR0←	SPORT 0 RX←	D5↔
Port 0.6	IO Reg0.6↔	nDCD0←	SPORT 0 Limp→	D6↔
Port 0.7	IO Reg0.7↔	nRI0←		D7↔
Port 0.8	IO Reg0.8↔	RX1←	SPORT 1 CLK_TX↔	D8↔
Port 0.9	IO Reg0.9↔	TX1→	SPORT 1 FRAME_TX↔	D9↔
Port 0.10	IO Reg0.10↔	nRTS1→	SPORT 1 TX →	D10↔
Port 0.11	IO Reg0.11↔	nCTS1←	SPORT 1 CLK_RX↔	D11↔
Port 0.12	IO Reg0.12↔	nDTR1→	SPORT 1 FRAME_RX↔	D12↔
Port 0.13	IO Reg0.13↔	nDSR1←	SPORT 1 RX←	D13↔
Port 0.14	IO Reg0.14↔	nDCD1←	SPORT 1 Limp→	D14↔
Port 0.15	IO Reg0.15↔	nRI1←		D15↔
Port 1.0	IO Reg1.0↔	RX2←	SPI 0 MOSI→	D16↔
Port 1.1	IO Reg1.1↔	TX2→	SPI 0 MISO←	D17↔
Port 1.2	IO Reg1.2↔	nRTS2→	SPI 0 CLK →	D18↔
Port 1.3	IO Reg1.3↔	nCTS2←	SPI 0 CS0→	D19↔
Port 1.4	IO Reg1.4↔	nDTR2→	SPI 0 CS1→	D20↔
Port 1.5	IO Reg1.5↔	nDSR2←	SPI 0 CS2→	D21↔
Port 1.6	IO Reg1.6↔	nDCD2←	SPI 0 CS3→	D22↔
Port 1.7	IO Reg1.7↔	nRI2←	SPI 0 CS4→	D23↔
Port 1.8	IO Reg1.8↔	RX3←	SPI 1 MOSI→	D24↔
Port 1.9	IO Reg1.9↔	TX3→	SPI 1 MISO←	D25↔
Port 1.10	IO Reg1.10↔	nRTS3→	SPI 1 CLK →	D26↔
Port 1.11	IO Reg1.11↔	nCTS3	SPI 1 CS0→	D27↔
Port 1.12	IO Reg1.12↔	nDTR3→	SPI 1 CS1→	D28↔
Port 1.13	IO Reg1.13↔	nDSR3←	SPI 1 CS2→	D29↔
Port 1.14	IO Reg1.14↔	nDCD3←	SPI 1 CS3→	D30↔
Port 1.15	IO Reg1.15↔	nRI3←	SPI 1 CS4→	D31↔
Port 2.0	IO Reg2.0↔		SPI 2 MOSI→	A0→
Port 2.1	IO Reg2.1↔		SPI 2 MISO←	A1→
Port 2.2	IO Reg2.2↔		SPI 2 CLK →	A2→
Port 2.3	IO Reg2.3↔		SPI 2 CS0→	A3→
Port 2.4	IO Reg2.4↔		SPI 2 CS1→	A4→
Port 2.5	IO Reg2.5↔		SPI 2 CS2→	A5→
Port 2.6	IO Reg2.6↔		SPI 2 CS3→	A6→
Port 2.7	IO Reg2.7↔	Timer0 OUT→	SPI 2 CS4→	A7→
Port 2.8	IO Reg2.8↔	Timer0 CLK←	SPI 3 MOSI→	SEL→
Port 2.9	IO Reg2.9↔	Timer0 GATE←	SPI 3 MISO←	WE→
Port 2.10	IO Reg2.10↔	Timer2 OUT→	SPI 3 CLK →	CLK→
Port 2.11	IO Reg2.11↔	Timer2	SPI 3 CS0→	STB→

Name	Parallel port	UART and	SPI and SPORT	32 bit Wishbone bus
		CLK←		
Port 2.12	IO Reg2.12↔	Timer2 GATE←	SPI 3 CS1→	ACK←
Port 2.13	IO Reg2.13↔	Timer1 OUT	SPI 3 CS2→	CYC→
Port 2.14	IO Reg2.14↔	Timer1 CLK	SPI 3 CS3→	INT0←
Port 2.15	IO Reg2.15↔	Timer1 GATE←	SPI 3 CS4→	
Strb0	Strb0 OUT – output of clock counter 0 of the carrier-board →			
Strb1	Strb1 OUT – output of clock counter 1 of the carrier-board →			

**** an arrow-head towards the carrier-board (→ output, ← input, ↔ bidirectional line) .***

1.3.9.2 Register module of mezzanine I/O space

Each mezzanine occupies a separate memory bank equal to 1024 32-bit words (0x3ff) or 4KB.

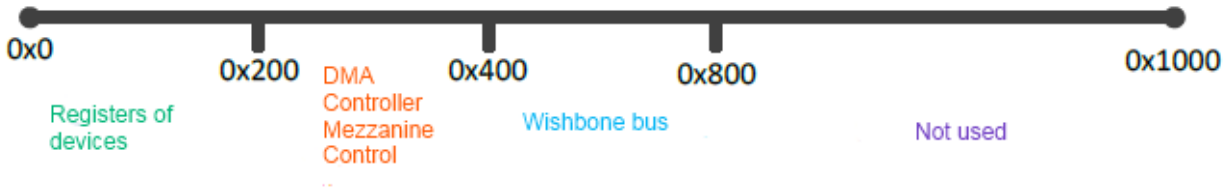


Figure 1.26 – Model of mezzanine I/O space

Register card Table 26

Name and modules	Interrupt number	Addresses on bus	Device number
Parallel port, type 1		0x000 – 0x00C 0x020 – 0x03C	0 1
Parallel port, type 2	0	0x040 – 0x05C	
Module for serial memory operation		0x010	
Indication of interrupts and geographical address		0x014	
Control of LEDs		0x01C	
Serial port, type 1 (SPI).	1 2 3 4	0x080 – 0x09C 0x0A0 – 0x0BC 0x0C0 – 0x0DC 0x0E0 – 0x0FC	0 1 2 3
Serial port, type 2 (SPORT). Transmitting module	5 7	0x100 – 0x11C 0x140 – 0x15C	0 1

Serial port, type 2 (SPORT). Receiving module.	6 8	0x120 – 0x13C 0x160 – 0x17C	0 1
Serial port type 3 (UART)	9 10 11 12	0x180 – 0x19C 0x1A0 – 0x1BC 0x1C0 – 0x1DC 0x1E0 – 0x1FC	0 1 2 3
Timers module	13	0x060 – 0x07C	
DMA controller	14	0x200 – 0x3FF	
Wishbone bus.	15	0x400 – 0x7FC	
Firmware version		0x800	

1.3.9.3 Register model of I/O ports of the carrier-board

a. Parallel port, type 1

Represents register digital input-output with a possibility to set direction. In addition, the port supports possibility of control an output switching unit, which performs connection of various ports to the FPGS output pins.

Table 27 Parallel port memory card, type 1

Addres	Operation	Name	Description
+0h	R	IN	Input register
+0h	W	OUT	Output register
+4h	R/W	DIR	Direction register
+8h	R/W	MODE	Register of device switching

Table 28 Input register

Bit	Operation	Description
15-0	R	State of inputs of the 15-0 port
31-16		Not used

Table 29 Output register

Bit	Operation	Description
15-0	W	State of outputs of the 15-0 port
31-16		Not used

Table 30 Direction register

Bit	Operation	Description
15-0	R/W	1 in the relevant bit moves the port to output data
31-16		Not used

Table 31 Register of device switching

Bit		Description
1-0	00	Output 0 is connected with *device 0*
	01	Output 0 is connected with *device 1*
	10	Output 0 is connected with *device 2*
	11	Output 0 is connected with *device 3*
….	……	
31-30	00	Output 15 is connected with *device 0*
	01	Output 15 is connected with *device 1*
	10	Output 15 is connected with *device 2*
	11	Output 15 is connected with *device 3*

b. Parallel port, type 2

Represents register digital input-output with a possibility to set direction. The port can generate interrupts when changing the state of port input lines, as well as generate single pulses of positive and negative polarity of the specified duration at output lines of the port, at the time of recording the logical 1 to the relevant bit of the port. In addition, the port supports possibility of control an output switching unit, which performs connection of various ports to the FPGS output pins.

Table 32 Parallel port memory card, type 1

Address	Operation	Name	Description
+0h	R	IN	Input register
+0h	W	OUT	Output register
+4h	R/W	DIR	Direction register
+8h	R/W	MODE	Register of device switching
+ ch	R/W	GEN_MODE	Register for control of port's pulse outputs.
+10h	R/W	GEN	Register of pulse generation.
+14h	R/W	INT_EN	Register for control of interrupts.
+18h	R/W	INT_R	Register for reset of interrupts.
+1ch	R/W	WIDTH	Register for setting a pulse duration time.

Table 33 Input register

Bit	Operation	Description
15-0	R	State of inputs of the 15-0 port
31-16		Not used

Table 34 Output register

Bit	Operation	Description
15-0	W	State of outputs of the 15-0 port
31-16		Not used

Table 35 Direction register

Bit	Operation	Description
15-0	R/W	1 in the relevant bit moves the port to output data
31-16		Not used

Table 36 Register of device switching

Bit		Description
1-0	00	Output 0 is connected with device 0
	01	Output 0 is connected with device 1
	10	Output 0 is connected with device 2
	11	Output 0 is connected with device 3
….	…….	
31-30	00	Output 15 is connected with device 0
	01	Output 15 is connected with device 1
	10	Output 15 is connected with device 2
	11	Output 15 is connected with device 3

Table 37 Register for control of port's pulse outputs.

Bit	Operation	Description
15-0	R/W	Switching of the port's output between output register generator output. 0 – output register is connected, 1 – generator output to the relevant port output
31-16	R/W	Polarity of output pulses: 0 – positive, 1 – negative, for the relevant output.

Table 38 Register of pulse generation

Bit	Operation	Description
15-0	R/W	Recording 1 in the relevant bit leads to pulse generation at the port output.
31-16		Not used

Table 39 Register of interrupts control

Bit	Operation	Description	
1-0	R/W	00	Interrupt at output 0 is prohibited
		01	Interrupt at output 0 is generated at the positive edge.
		10	Interrupt at output 0 is generated at negative edge.
		11	Interrupt at output 0 is generated at any edge
….	R/W	…….	
31-30	R/W	The same is for output 15	

Table 40 Register of interrupts reset

Bit	Operation	Description
15-0	W	Recording 1 to the bit corresponding to the port's output leads to interrupt reset at the relevant output.
15-0	R	Register for interrupts state. 1 in the relevant bit means that there is an interrupt at the relevant port output.
31-16		Not used

Table 41 Register for setting pulse duration time

Bit	Operation	Descriptio
7-0	R/W	Sets the pulse length in periods of the bus clock frequency (20ns) for outputs of the 3-0 port.
15-8	R/W	Sets the pulse length in periods of the bus clock frequency (20ns) for outputs of the 7-4 port.
23-16	R/W	Sets the pulse length in periods of the bus clock frequency (20ns) for outputs of the 11-8 port.
31-24	R/W	Sets the pulse length in periods of the bus clock frequency (20ns) for outputs of the 15-12 port.

c. Module for serial memory operation

Module (flash_key) performs all operations to access the flash-memory chip installed on the mezzanine (soft key). In addition to flash-memory operation the module also determines mezzanine presence based on the behavior of miso line of flash-memory during device reset. Conditions – miso line on the mezzanine should be pulled up to 3.3V and the carried-board should have a pull-down of 100kOhm to the ground. In case of th installed mezzanine, the 30th bit of the flash-memory state and control register would have 1, in the lack of flash-memory - 0. Mezzanine installation is checked once during power supply, within 128 cycles of the reference clock of the bus, after bus reset. During the testing time, module generates an additional reset signal rst_o in order to prevent improper connection of I/O modules to mezzanine devices.

Table 42 Register of flash-memory state and control (Base Address + 0)

<table>
<tr><th>Bit</th><th>Operation</th><th>Description</th></tr>
<tr><td>0-7</td><td>W</td><td>Data to be recorded to memory (1 Byte)</td></tr>
<tr><td>0-7</td><td>R</td><td>Data read from memory (1 Byte)</td></tr>
<tr><td>23-8</td><td>R/W</td><td>Address at which read/write operation is performed (16 bits).
<table>
<tr><th>Type of memory chip</th><th>Maximum address</th></tr>
<tr><td>25080</td><td>0x3ff</td></tr>
<tr><td>25160</td><td>0x7ff</td></tr>
<tr><td>25320</td><td>0xfff</td></tr>
<tr><td>25640</td><td>0x1fff</td></tr>
<tr><td>25128</td><td>0x3fff</td></tr>
<tr><td>25256</td><td>0x7fff</td></tr>
</table></td></tr>
<tr><td>26-24</td><td>R/W</td><td>Command executed by memory chip
<table>
<tr><th>Commands</th><th>Code</th></tr>
<tr><td>Write enable</td><td>0b110</td></tr>
<tr><td>Write disable</td><td>0b100</td></tr>
<tr><td>State register read</td><td>0b101</td></tr>
<tr><td>State register write</td><td>0b001</td></tr>
<tr><td>Data read</td><td>0b011</td></tr>
<tr><td>Data write</td><td>0b010</td></tr>
</table></td></tr>
<tr><td>27</td><td>R/W</td><td>Read/write operation direction This bit should be installed during reading operations from memory chip.</td></tr>
<tr><td>28</td><td>W</td><td>Start of command execution.</td></tr>
<tr><td>28</td><td>R</td><td>Indication of memory chip busy for access state. Communications cycle is running.</td></tr>
<tr><td>29</td><td>W</td><td>Activation of power supply 12V (static parameter - 1 power supply is activated)</td></tr>
<tr><td>29</td><td>R</td><td>Fault12V – Power supply overload+12V</td></tr>
<tr><td>30</td><td>R</td><td>Fault_3V3 – absence of +3V3 power supply on mezzanine (resettable fuse was activated)</td></tr>
<tr><td>31</td><td>R</td><td>Indication of mezzanine availability in the slot.</td></tr>
</table>

Interrupt control register (Base Address + 4):

1 installed in 0-15 bits demonstrates interrupts of the relevant interface (in accordance with the Table 26), where bit number corresponds to the number of interrupt.

d. Control of LEDs

It is possible to control the LEDs installed on the carrier-board.

Table 43

Bit	Operation	Value
0	W	LED1, value = 1 activated, = 0 - deactivated
1	W	LED2, value = 1 activated, = 0 - deactivated.
2-31		Reserve

e. Serial port, type 1 (SPI)

Represents 4x independent SPI ports having the following features:

- Full-duplex data transfer;
- modifiable length of the word is ranging from 3 to 128 bits;
- selection of a falling or rising edge during receipt and transmission;
- 5 x device select lines;
- modifiable clock frequency;
- use of only internal clock frequency of FPGA for port operation purposes;
- port operation only in master mode;

Table 44 Memory card of SPI port

Addres	Description
+0h	Data 0 – bits from 0 to 32 (R\W)
+4h	Data 1 – bits from 33 to 63 (R\W)
+8h	Data 2 – bits from 64 to 95 (R\W)
+ch	Data 3 – bits from 96 to 127 (R\W)
+10h	Control and status word
+14h	Control word of frequency divider
+18h	Device selection register

Table 45 Control and status word

Bit	Operation	Name	Description
0-6	R/W	Char_len	Length of the receivable/transmittable word: 1 – 1 bit, 127 – 127 bit, 0 – 128 bit.
7	R		Reserved
8	R/W	Go_bsy	Writing of 1 starts data transmission Upon completion of the transmission cycle, the bit will automatically return to 0.
9	R/W	Rx_neg	If the bit is installed, data will be latched along the falling edge of the clocking signal.
10	R/W	Tx_neg	If the bit is installed, data will be changed along the falling edge of the clocking signal.
11	R/W	LSB	If the bit is installed as the first, the least-significant bit will be forwarded
12	R/W	I E	Enabling interrupt generation after data transmission cycle.

13	R/W	ASS	If the bit is installed, a device selection signal will be shaped automatically during the time of data transfer.
14	R/W	Enbl_clk	Continuous frequency generation to the output
31:15	R		Reserved

Table 46 Control word of frequency divider

Bit	Operation	Name	Description
15-0	R/W	Div	Reference frequency division ratio for obtaining of port's clock frequency. $f_{sclk} = \frac{f_{wb\_clk}}{(DIVIDER+1)\cdot 2}$. Reference frequency – 62.5 MHz;
31-16	R		Reserved

In the device select register, the least-significant 5 bits correspond to the lines Chip Select (CS) at port output

Example of device connection:

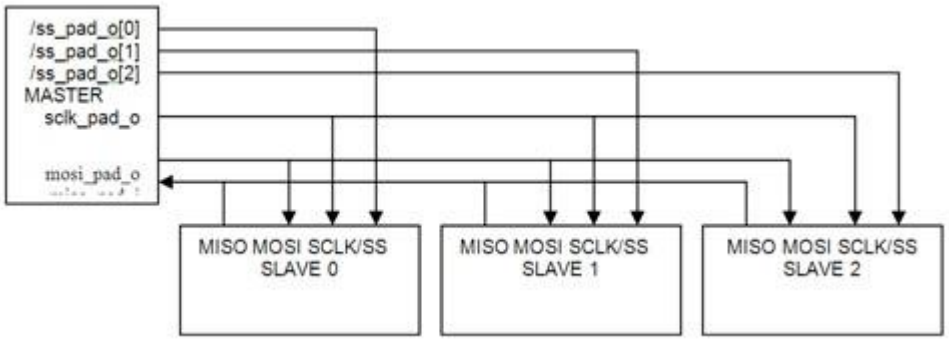


Figure 1.27 – Example of device connection

Timing diagrams of port operation with various configurations of Tx_neg and Rx_neg bits:

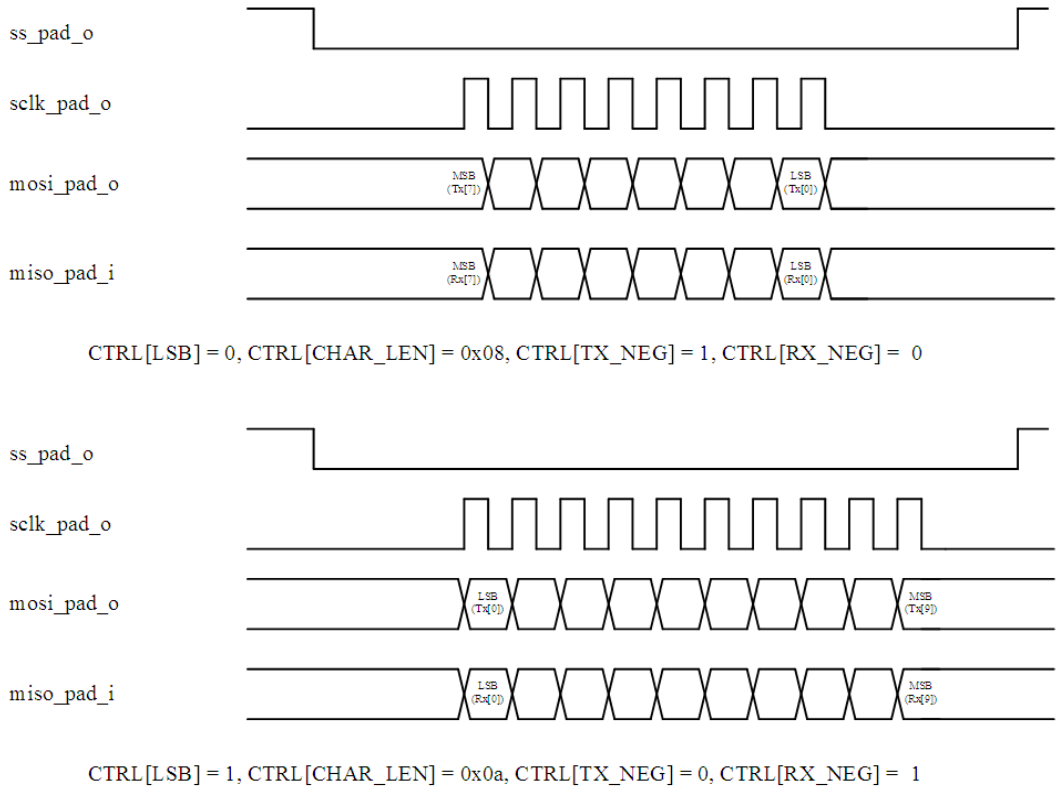


Figure 1.28 – Timing diagrams of port operation

f. Serial port, type 2 (SPORT)

Represents two pairs of independent modules of receiver and transmitter with FIFO. The both ports can operate in master/slave modes by flexible change of synchronization configurations. Lines of clock frequency and frame can operate both as input and output. Each port has FIFO for 2048 readouts and implements data collection capabilities with the use of DMA channels. Configuration of DMA channels is carried out in a separate block.

- **Transmitter**

Table 47 Memory card SPORT TX

Addres	Operation	Description
+0h	W	Data for transmission
+4h	R/W	Control word 0
+8h	R/W	Control word 1
+ch	R/W	Control word 2
+10h	R	Port status

Table 48 Control word of 0 SPORT TX

Bit	Operation	Name	Description
0	R/W	Clk_pol_tx	Polarity of clock signal 0 – data shift along the positive edge, 1 – along the negative edge.
1	R/W	Clk_out_tx	Enabling clock frequency output to operate as the output, if 1.
2	R/W	Clk_inv_tx	Inversion of input frequency, if = 1
3	R/W	Clk_sel_tx	Switching serial port's clocking source, = 0 – internal clocking source, = 1 – clocking from CLK_TX pin.
4	R/W	Frame_sel_tx	Selection of Frame signal type. = 0 – frame for the entire data sending, = 1 – only for the first bit
5	R/W	Frame_pol_tx	Frame polarity selection, = 0 – positive polarity, = 1 – negative polarity.
6	R/W	Frame_out_tx	Enabling the Frame output to operate as the output, if 1.
7	R/W	Frame_inv_tx	Inversion of input Frame signal.
8	R/W	LSB	= 1 – the first to transfer will be the most-significant bit,
9	R/W	Mode	= 0 – single transmission, = 1 – repeated transmission.
10	R/W	I2S	= 1 – port in I2S mode of transmission (for odd sendings of frame = 1, for even = 0)
11	R/W	Star	Start of the transmission
13:12	R/W	Start_sel_tx[0]	= 0 – continuous Frame rate for start, = 1 – single launch for start.
		Start_sel_tx[1]	= 0 – internal transmission start, = 1 – start of transmission from the pin Frame.
14	R	reserved	
19:15	R/W	word_len	Length of single word sending (5 bits) 2^N-1
30:20	R/W	TRESH_in_tx	Value of sender buffer's threshold
31	R/W	Rst_data	Reset of serial port's FIFO

Table 49 Control word of 1 SPORT TX

Bit	Operation	Name	Description
11:0	R/W	Divider	Divider of internal frequency for generation of the port's clock frequency
11:12 PM	R/W	frame_rate	Generation of pulses for starting transmission in the continuous mode (Start_sel_tx[0] = 0). Frequency of port' clocking is divided by a ratio ranging from 3 to 4096, code is changing from 2 to 4095.
28:24	R/W	Frame_count	Number of sendings during one start in TDMI mode (5 bits) 2^N-1
29	R/W	Frame_type	0 – early frame synchronization (start per 1 clock cycle prior to data), 1 – late
31	R/W	rst	Transmitter reset

Table 50 Control word 2 SPORT TX

Bit		Operation	Name	Description
0		R/W	SPORT_enbl	= 1 enable operation SPORT_tx, or else = 0
1		R/W	DMA_enbl	= 1 enable DMA, or else = 0
31:3		R	reserved	

Table 51 Status interrupt control word SPORT TX

Bit	Operation	Name	Description
0	R	Busy	Port is busy with transmission
1	R	FF_data	Buffer is full
2	R	OVF_data	Sender buffer overflow
3	R	EMP_data	Receive buffer is empty
4	R	TH_data	Value of sender buffer's threshold
5	R/W	FF_en	Enabling interrupt in case of the "Buffer is full"
6	R/W	OVF_en	Enabling interrupt in case of the "Buffer is overflown"
7	R/W	EMP_en	Enabling interrupt in case of the "Buffer is
8	R/W	TH_en	Enabling interrupt in case of the "Buffer threshold triggering"

- Receiver

Table 52 Memory card SPORT TX

Addres	Operation	Description
+0h	R	Reading data from FIFO
+4h	R/W	Control word 0
+8h	R/W	Control word 1
+ch	R/W	Control word 2
+10h	R	Port status
+14h	R	Reading of the receiving data register

Table 53 Control word of 0 SPORT TX

Bit	Operation	Name	Description
0	R/W	Clk_pol_rx	Polarity of clock signal 0 – data shift along the positive edge, 1 – along the negative edge.
1	R/W	Clk_out_rx	Enabling clock frequency output to operate as the output, if 1.
2	R/W	Clk_inv_rx	Inversion of input frequency, if = 1
3	R/W	Clk_sel_rx	Switching serial port's clocking source, = 0 – internal clocking source, = 1 - clocking from CLK_TX pin.
4	R/W	Frame_sel_rx	Selection of Frame signal type. = 0 – frame for the entire data sending, = 1 – only for the first bit

5	R/W	Frame_pol_rx	Frame polarity selection, = 0 – positive polarity, = 1 – negative polarity.
6	R/W	Frame_out_rx	Enabling the frame output to operate as the output, if 1.
7	R/W	Frame_inv_rx	Inversion of input frame signal.
8	R/W	LSB	= 1 – the first to receive will be the most significant bit, = 0 – the least significant bit.
9	R/W	Mod e	= 0 – receipt at frame edge, = 1 – receipt at frame level (delay for 1 clock cycle).
10	R/W	I2S	= 1 – port in I2S mode of receipt (for odd sendings of frame = 1, for even = 0)
11	R/W	Start	Forced receipt start with simultaneous frame generation.
12	R/W	DMA_enbl	= 1 DMA enabled, = 0 – disabled
13	R	Reserved	
14	R	Reserved	
19:15	R/W	Frame_len	Length of single word sending (5 bits) 2^N-1
30:20	R/W	tresh_in_rx	FIFO triggering threshold.
31	R/W	Rst_data	Reset of serial port's FIFO

Table 54 Control word of 1 SPORT TX

Bit	Operation	Name	Description
11:0	R/W	Divider	Divider of internal frequency for generation of the port's clock frequency
11:12 PM	R/W	Frame_rate	Generation of pulses for starting receipt in the continuous mode (int_frame_continue= 0). Frequency of port' clocking is divided by a ratio ranging from 3 to 4096, code is changing from 2 to 4095.
28:24	R/W	Frame_count	Number of the words received during one frame in TDMI mode (5 bits) 2^N-1
29	R/W	int_frame_continue	1 – continuous generation of framerate, 0 – one-time generation per start bit.
31	R/W	rst	Receiver reset

Table 55 Control word of 2 SPORT RX

Bit	Operation	Name	Description
31:0	R/W	tdmi_en	Bit field, setting 1 in the bit field enables receipt of this word in case of the TDMI mode of port's receipt. Maximum number of slots in TDMI mode: 32.

Table 56 Status word of SPORT RX

Bit	Operation	Name	Description
0	R	Busy	The port is busy with data receipt
1	R	FF_data	Buffer is full
2	R	OVF_data	Receipt buffer overflow
3	R	EMP_data	Receive buffer is not empty
4	R	TH_data	Triggering of receipt buffer's threshold
5	R/W	FF_en	Enabling interrupt in case of the "Buffer is full"
6	R/W	OVF_en	Enabling interrupt in case of the "Buffer is overflown"
7	R/W	EMP_en	Enabling interrupt in case of the "Buffer is not empty"
8	R/W	TH_en	Enabling interrupt in case of the "Buffer threshold triggering"
19:9	R	data_count	Amount of data in FIFO.

g. Serial port, type 3 (UART)

Represents 4x ports software compatible with the standard transmitter-receiver unit 16550A.

Table 57 Memory card UART

Address	Operation	Description
+0h	R	Receipt buffer
+0h	W	Sender buffer
+4h	R/W	Enabling/Informing interrupts
+8h	R	Information of interrupt
+8h	W	FIFO control
+ch	R/W	Communication control
+10h	W	Modem control
+14h	R	Port status
+18h	R	Modem status

More details on counter operating modes can be found at:
http://en.wikipedia.org/wiki/16550_UART

h. Timers module

Represents tow sets of counters: counters (type 1) whose functionality is compatible with 8254 (3 pcs), but with the increased counter bits up to 32x, and "simple" counters (type 2) for generating strobe pulses (2 pcs.).

Type 1 counters enable operation in 5 modes functionally compatible with 8254, have 32 bits and make it possible to use several signal sources as clocking. The counters have individual data latching inputs and a common data latching input that enables reading data from three counters simultaneously. It is possible to build a diagram of cascade connection of counters for generation pulse complex sequences. Mechanism of access and control of each counter is represented by pair of registers: control and status word and data word. When writing data word, the data are uploaded to the counter. When reading, counter's instantaneous state is read. When reading data word with the use of data latching bits, the latched counter states will be read. After reading the data of the relevant counter (in the latched state), the latching bit will be reset and counter data latching mechanism will be unblocked. More details on counter operating modes can be found at: http://www.digchip.com/datasheets/parts/datasheet/227/8254.php

Type 2 counters are 32x bit subtracting counters with data loading and generation of the carry pulse, which occurs in case of counter overflow. The counters are designed for generation of short (50 ns) strobe pulses. Clocking of the counters is carried out from the temperature-compensated with a frequency of 20MHz, installed in the carrier-board. Simultaneous control of counters is possible in order to receive synchronous pulse sequences. Mechanism of access and control of the counters is represented by the following registers: control and status word and data word. When writing data word, the data are uploaded to the counter. There is one control and status word for the both counters and it enables simultaneously and separately upload data to the counters, invert output signal from the counters, as well as stop or start the counters simultaneously or separately. Reading data from counters is not provided.

Table 58 Memory card of timers module

Address	Description
+0h	Data for counter 0, type 1 (R\W)
+4h	Control and status word of counter 0, type 8254 (R\W)
+8h	Data for counter 1, type 1 (R\W)
+ch	Control and status word of counter 1, type 8254 (R\W)
+10h	Data for counter 2, type 1 (R\W)
+14h	Control and status word of counter 2, type 8254 (R\W)
+18h	Data for clock counters 0 and 1, type 2, (W)
+1ch	Control word of clock counters 0 and 1, type 2 (R\W)

Table 59 Control and status word of counter, type 1

Bit	Operation	Description
4:2	R/W	Counter operation mode: 0 interrupt of terminal counting 1 single-trip multivibrator 2 pulse generator 3 cascade generator 4 single software-controlled strobe 5 single hardware-triggered strobe.
6:5	R/W	Selection of counter clocking input: 0 Internal clocking signal (20 MHz) 1 Internal clocking signal (50 MHz) 2 external clocking signal 3 0
8:7	R/W	Selection of GATE input connection:

		0	GATE = 1
		1	GATE = OUT1(for counter 0) or OUT0(for counter 1 and 2) *
		2	GATE = OUT2(for counter 0 and 1) or OUT1(for counter 2) *
		3	GATE external
9	R/W	Latching the selected counter	
10	R/W	Latching data in all counters	
11	R/W	Inversion of counter output	
12	R/W	Enabling interrupt of this counter	
13	R	Interrupt flag is reset after register reading	
14	R/W	Enabling operation of this counter	
15	W	Counter reset (bit is reset automatically)	
16	R/W	Conditions for interrupt to appear: 0 – positive, 1 – negative edge of counter output.	
30	W	Reset of all counters	
31	R	Status of counter output	

* OUT0..1 –counter output

Table 60 Control and status word of the counters, type 2

Bit	Description
0	Enabling counting to counter 0
1	Forced data upload to counter 0*
2	Output signal polarity of counter 0. 0 - positive pulse, 1 – negative pulse
3	Setting this bit to 1 enables writing data for booting the counter 0. I.e. in order to upload data to the counter it is required to set the bit to 1 and write data to the data register for clock counters. If data need to be written to the both counters simultaneously, bits 3 and 7 need to be set, after that data will be written to register +18h.
4	Enabling counting to counter 1
5	Forced data upload to counter 1*
6	Output signal polarity of counter 1. 0 - positive pulse, 1 – negative pulse
7	Setting this bit to 1 enables writing data for booting the counter 1.

* When counter starts, data forced loading bit should be set simultaneously with the counting enable bit. The bit will be reset automatically.

i. Wishbone bus

Represents 32x bit parallel bus. More details on bus operation can be found at https://ru.wikipedia.org/wiki/Wishbone

j. DMA controller

General structure of DMA controller.

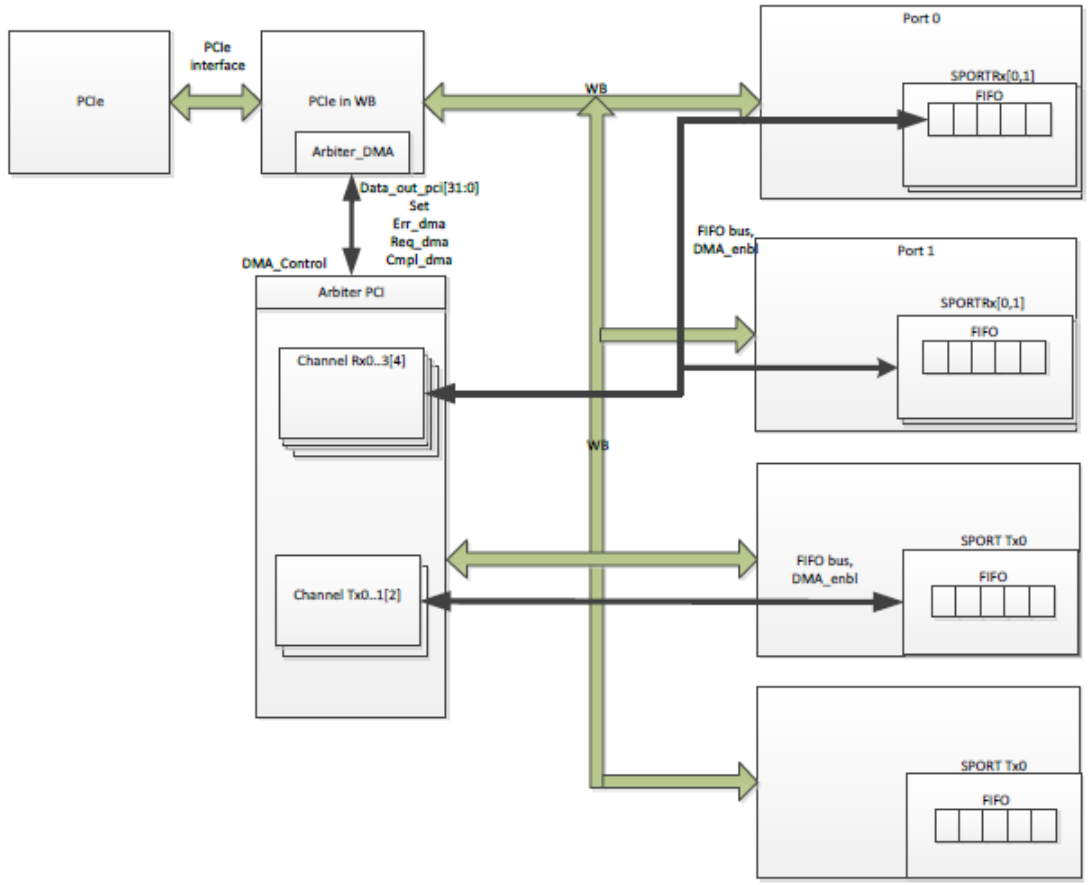


Figure 1.29 – General structure of DMA controller

DMA has 6 channels: 4x "dma_rx" – for each receiving port SPORT Rx from each mezzanine and 2x "dma_tx" - one transmitting SPORT Tx for each mezzanine. Each channel is independent and enables to transmit data from the FIFO receiving buffer of SPORT Rx port to PCIe channel and from PCIe channel to the output buffer SPORT Tx. Since there is a single PCIe channel, arbitration of requests from all the channels is carried out.

For activation (deactivation) of "dma_rx" channels it is required set 1(0) in bit 12 of the register SPORT Rx (control word 0, address +4h). For activation (deactivation) of "dma_tx" channels it is required to set 1 - deactivation (0 - activation) in bit 1 in the register SPORT Tx (control word 2, address +ch).

For proper operation, the entries in addressing of DMA channels should be done when the channels are off (the relevant bits have 0).

Table 61 Address space

Bit	Operation	Name	Description
dma_rx0			
+0x0	R/W	dma_addr_lo_rx0	[31:0] lower 32 bit of host physical memory
+0x4	R/W	dma_addr_hi_rx0	[31:0] upper 32 bit of host physical memory
+0x8	R/W	dma_dwcount_rx0	[10:0] length of 32x bit word transaction

+0xc	R/ W	dma_cntrl_ rx0	[3:0] control word
+0x10	R/ W	dmad_addr_lo_ rx0	[31:0] lower 32 bits of physical memory address of initial
+0x14	R/ W	dmad_addr_hi_ rx0	[31:0] upper 32 bits of physical memory address of initial
+0x18	R/ W	dmad_count_ rx0	[7:0] number of descriptors
+0x1c	R/ W	cur_dmad_count_rx0	[7:0] current descrirptor
dma_rx1 channel			
+0x20	R/ W	dma_addr_lo_ rx1	
+0x24	R/ W	dma_addr_hi_ rx1	
+0x28	R/ W	dma_dwcount_ rx1	
+0x2c	R/ W	dma_cntrl_ rx1	
+0x30	R/ W	dmad_addr_lo_ rx1	
+0x34	R/ W	dmad_addr_hi_ rx1	
+0x38	R/ W	dmad_count_ rx1	
+0x3c	R/ W	cur_dmad_count_rx1	
dma_tx channel			
+0x40	R/ W	dma_addr_lo_ tx0	
+0x44	R/ W	dma_addr_hi_ tx0	
+0x48	R/ W	dma_dwcount_ tx0	
+0x4c	R/ W	dma_cntrl_ tx0	
+0x50	R/ W	dmad_addr_lo_ tx0	
+0x54	R/ W	dmad_addr_hi_ tx0	
+0x58	R/ W	dmad_count_ tx0	
+0x5c	R/ W	cur_dmad_count_tx0	

Table 62 Structure of dma_cntrl control word

Bit	Operation	Name	Description
0	R/W	run	Start
1	R/W	inten	Interrupt enabling
2	R	interrupt	Interrupt flag is reset after reading
3	R/W	chain	Enabling to upload data from RAM

As a first step, we will need to configure the initial descriptor address, for which purpose values dmad_addr_lo, dmad_addr_hi need to be filled out and a total amount of descriptors (N-1) dmad_count should be specified. After performing of this transaction, if dmad_count>0, the next descriptor will be addressed (Next value address = Current value +16). If the end of descriptors list is detected (dmad_count = cur_dmad_count), return to the initial will be performed.

In order to start DMA transaction, value 1 should be written in "dma_cntrl" word in the "run" bit. In this case, if "chain" bit = 0, then the values dma_addr_lo, dma_addr_hi, dma_dwcount and dma_cntrl are taken from those written in registers of DMA channels. If "chain" bit = 1, then these values are read from the address, specified in the current descriptor.

After this transaction, if the value in "chain" bit = 0, the "run" bit is reset. In order to build a chain of DMA transactions you will have to set value 1 in the "chain" bit. In this case, upon completion of this transaction, the next descriptor will be read from RAM and value of the "run" bit be taken from the newly read word. In order to perform a single transaction, in the word "dma_cntrl" set the "run" bit to 1, bit
"chain" to 0.

All the transactions are carried out by 32x bit words.

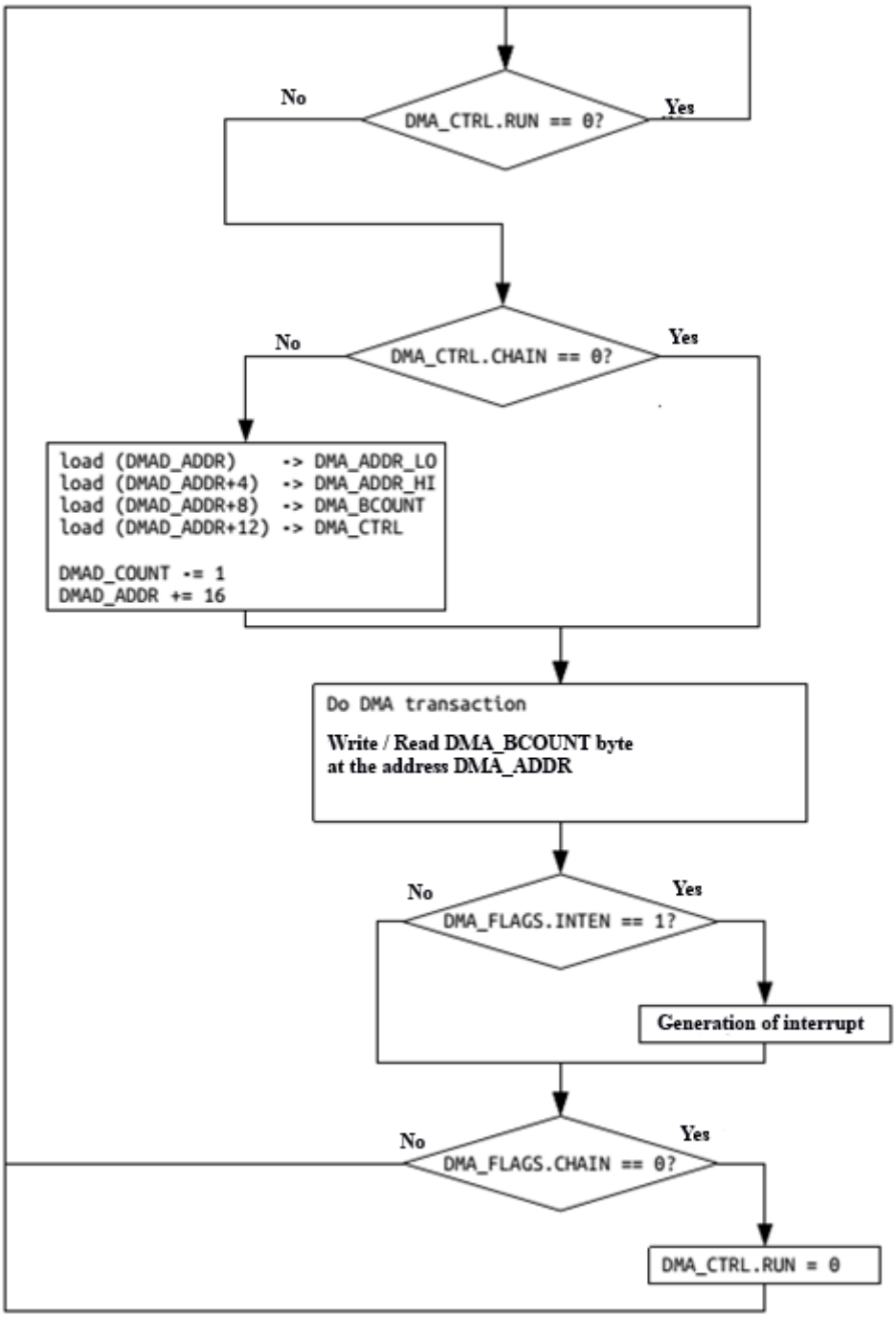


Figure 1.30 – Simplified algorithm of DMA operation

1.4 LABELING

In accordance with the design documentation requirements, module and mezzanine labeling should be made to the printed board and contains the following notations:

- code name (code name) of the module;
- manufacturer's name;
- serial number of the board;
- year of batch manufacturing start;
- decimal number of the printed board;
- reference designators of elements.

Labeling of consumer packages is made by sticking an individual identification number (sticker) of module's version type.

Package sticker contains the following notations:

- name of module's version type;
- notation of the module's version type in the Fastwel® product catalog.

1.5 PACKAGING

In accordance with the requirements of manufacturing specification, module and/or mezzanine are going to be packed in an individual antistatic package (bag) and placed in a separate consumer package (carton box).

Internal carton insert inside the consumer package ensures additional durability, prevents deformation and module's shifts during transportation.

2 INTENDED USE

2.1 PREPARATION FOR USE

2.1.1 Installation of drivers

This section describes the procedure of drivers installation for DIC551 module and mezzanines MIC1002/MIC1004 in Linux OS**,** In order to install the drivers, you can use instructions for assembly and installation of Linux kernel modules, which can be found over the Internet at: https://www.kernel.org/doc/Documentation/kbuild/modules.txt **,** or by installing linux-doc package:

$ sudo apt-get install linux-doc

$ less /usr/share/doc/linux-doc/kbuild/modules.txt.gz

- Install header files of Linux kernel and development tools:

$ sudo apt-get install build-essential linux-headers-`uname -r`

- Unpack archives and move to the directory with driver's source code:

$ tar -zxf dic551-linux-<VER>.tar.gz

$ cd dic551-linux

where <VER> is a number of the driver's version.

- Perform compilation:

$ make -C /lib/modules/`uname -r`/build M=$PWD

- Check modules operation:

$ modprobe libcrc32c

$ insmod ./fastwel.ko

$ insmod ./mic100x.ko

$ insmod ./dic551/dic551.ko

$ dmesg | tail -n50

Commands should be finished without errors and output of the last command should contain the line:

fastwel: Fastwel universal driver <VER> major 240

where <VER> is a number of the driver's version.

- Install the kernel modules to system directory:

$ sudo make -C /lib/modules/`uname -r`/build M=$PWD modules_install

$ sudo depmod

- Add the modules to the automatic loading list:

$ echo dic551 | sudo tee -a /etc/modules

$ echo mic100x | sudo tee -a /etc/modules

More details on the contents, operation principles and access to mezzanines is described in the "Use Manual for programmers of DIC551 mezzanines" IMES.467444.068I12.

2.1.2 Information on the types of dangerous effects

The module is structurally safe for life and health during its use under the specified operating conditions and contains no adverse effect sources.

2.1.3 General requirements

All installation and preparation works with the module and devices connected to it should be carried out only when the power supply of such devices is off and module's connectors have no voltages.

ATTENTION: IN ORDER TO PREVENT MODULE BREAKDOWNS IT IS REQUIRED TO STRICTLY COMPLY WITH THE GENERAL REQUIREMENTS WHEN PREPARING THE MODULE FOR USE!

2.1.4 Electrostatic safety requirements

In accordance with the GOST R IEC 60950-2002 (for the equipment to be connected to electricity mains with a voltage up to 600V). All installation and preparation works, replacement of elements and module maintenance should be carried out only with the use of special tools and technical accessories (e.g. electrostatic discharge straps etc.), free of electrostatic discharge and magnetization properties.

ATTENTION: THE MODULE CONTAINS ESD COMPONENTS!

2.2 MODULE USE

While in operation, the module will be automatically configured and requires no configurations and software settings.

3 MAINTENANCE

No maintenance is required for the module during its entire useful life.

4 REPAIRS

Module repairs should be performed only in the Service centers of manufacturer or in authorized PROSOFT® service centers.

General provisions and grounds for repairs are outlined in Section 8 of the User Manual.

ATTENTION: PERFORMING MODULE'S REPAIRS ON YOUR OWN IS PROHIBITED!

5 STORAGE

5.1 STORAGE CONDITIONS

Module storage conditions for group 1 are defined in the GOST standard 15150-69 (IEC 721-2-1 standard).

6 TRANSPORTATION

6.1 GENERAL REQUIREMENTS AND CONDITIONS

6.1.1 Shipping package

The module should be transported in the manufacturer's separate package (container), which contains individual antistatic bag and carton box.

It is possible to transport modules, packaged in individual antistatic packages, in multiple packaging (transport container) of the manufacturer.

Package should ensure integrity and operating capability of the module after transportation.

ATTENTION: DURING TRANSPORTATION, PROTECTION OF MODULE'S TRANSPORT PACKAGE AGAINST INGRESS OF ATMOSPHERIC PRECIPITATION SHOULD BE ENSURED!

6.1.2 Means of transportation

Transportation of the modules is allowed by highway and railway transport types, without limitations for movement speeds over any distances.

Transportation of the modules by air transport is allowed in th

6.1.3 Climatic conditions

Transportation of the modules with the above transportation types is allowed under the following climatic conditions:

- ambient air temperature: from - 50 to +60 °C;
- - relative air humidity: no more than 95 % at the temperature up to +30 °C.
- atmospheric pressure from 84 to 107 kPa (from 630 to 800 mm of mercury).

6.2 TRANSPORTATION CHARACTERISTICS

Overall dimensions:

Overall dimensions of the shipping container:

- DIC551: no more than: 230 mm × 155 mm x 45 mm.

- DIC551RC, DIC551-03 (Evaluation KIT): no more than 350 mm x 260 mm 70 mm
- MIC1002, MIC1003, MIC1004: no more than 230 mm × 155 mm x 45 mm.

Weight**:**

- DIC551: no more than 0.2 kg.
- DIC551RC: no more than 0.7 kg.
- MIC1002, MIC1003, MIC1004: no more than 0.1 kg.

Weight of the shipping container (gross weight):

- DIC551: no more than 0.4 kg.
- DIC551RC: no more than 0.9 kg.
- DIC551-03 (Evaluation KIT): no more than 0.8 kg;
- MIC1002: no more than 0.3 kg.
- MIC1003: no more than 0.25 kg.
- MIC1004: no more than 0.25 kg.

6.3 PLACEMENT AND FIXING OF SHIPMENT CONTAINER

Placement and fixing of the shipment container should be carried out in such a way that will ensure stability of its position, excluding any shifts and shocks during transportation.

ATTENTION: ANY BLOWS, DROPS AND SHOCKS DURING TRANSPORTATION THAT COULD HAVE AN IMPACT ON MODULE'S SAFETY AND WORKING CAPACITY, SHOULD BE AVOIDED!

7 UNPACKING

7.1 GENERAL REQUIREMENTS AND CONDITIONS

7.1.1 Climatic requirements

Module's unpacking should be carried out only in a facility with an ambient temperature of not lower than + 15° C and relative humidity of not more than 70 %.

7.1.2 Additional requirements

Unpacking of the module that was exposed to ambient temperatures under 0° C should be carried out only in a heated facility; in this case, the module should be previously kept under normal conditions within 6 hours.

ATTENTION: It is prohibited to place the packaged module close to the heat source!

7.1.3 Safety precautions

During unpacking of the module, it is required to observe safety precautions, ensuring its safety.

7.1.4 External view assessment

At the time of unpacking it is required to check the module that it has no external mechanical damages after transportation.

Note – If any of the components from the delivery checklist lacks or has external mechanical damages, please contact the official distributor that sold you this module.
Retain the original antistatic and consumer packages of the module till the end of the guarantee service life period.

8 WARRANTIES

8.1 Warranty liabilities

Manufacturer guarantees that product's quality meets all requirements of the design documentation and technical specifications (DIC551: IMES.469555.001TR; DIC551RC, MIC1002, MIC1003, MIC1004: IMES469555.002TR)
in case the Consumer complies with operation, transportation, storage, installation and mounting conditions.

The Manufacturer hereby guarantees that the products supplied thereby are free from defects in workmanship and materials, provided operation and maintenance norms were observed during the currently established warranty period. The Manufacturer's obligation under this warranty is to repair or replace free of charge any defective electronic component being a part of a returned product.

Products that broke down through the Manufacturer's fault during the warranty period will be repaired free of charge. Otherwise the Consumer will be invoiced as per the current labor remuneration rates and expendable materials cost.

8.2 Liability limitation right

The Manufacturer shall not be liable for any damages, caused to any property due to the failure of the devices at the time of its operation during the whole service period of the device.

8.3 Warranty period

The warranty period for the products made by Fastwel LLC is 36 months since the sale date (unless otherwise provided by the supply contract). The warranty period for the custom-made products is 60 months from the date the Product was fist purchased (unless otherwise provided by the supply contract).

8.4 Limitation of warranty obligations

The above warranty obligations shall not be applied:

- To the products (including software), which were repaired or were amended by the employees, that do not represent the manufacturer. Exceptions are the cases where the customer has made repairs or made modifications to the devices in the strict compliance with instructions, preliminary agreed and approved by the manufacturer in writing;
- To the products, broken down due to unacceptable polarity reversal (to the opposite sign) of the power supply, improper operation, transportation, storage, installation, mounting or accident.

8.5 Procedure of equipment return and repairs

Sequence of activities when returning the products for repairs:

- Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization;
- Attach a failure inspection report with a product to be returned in the form, accepted by the Manufacturer, with a description of the failure circumstances and symptoms;
- Carefully package the product in the antistatic bag and carton box, in which the product had been supplied. Failure to package in antistatic material will VOID all warranties.

The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer.

ANNEX A

(for reference purposes)

List of abbreviations and notations used

- Module – depending on the version is either 3U I/O Module cPCI®Serial DIC551, or 4U I/O Module cPCI®Serial DIC551RC;
- PROSOFT® - PROSOFT ® company, official distributor;
- Manual – User Manual;

ANNEX B
Options of the installable mezzanines and correspondence of the front panels

Version DIC551	Mezzanine version MIC1001	Mezzanine version MIC1002	Mezzanine version MIC1003	Mezzanine version MIC1004	Panel, to be installed to DIC551	Additional 4HP panel for output of three COM-ports (301412.098), pcs
DIC551-01	-	-	-	-	301412.086	
DIC551-01	-	MIC1002-01	-	-	301412.086-02	1
DIC551-01	MIC1001-01	MIC1002-01	-	-	301412.086	1
DIC551-01	-	MIC1002-01	MIC1003-01	-	301412.086	1
DIC551-01	-	MIC1002-01		MIC1004-01	301412.086	1
DIC551-01		MIC1002-01 (2 pcs.)	-	-	301412.086-02	2
DIC551-01	MIC1001-01	-	MIC1003-01	MIC1004-01	301412.086	
DIC551-02	MIC1001-02	MIC1002-02	MIC1003-02	MIC1004-02	301412.086-03	
DIC551-02	-	-	-	-	301412.086-03	

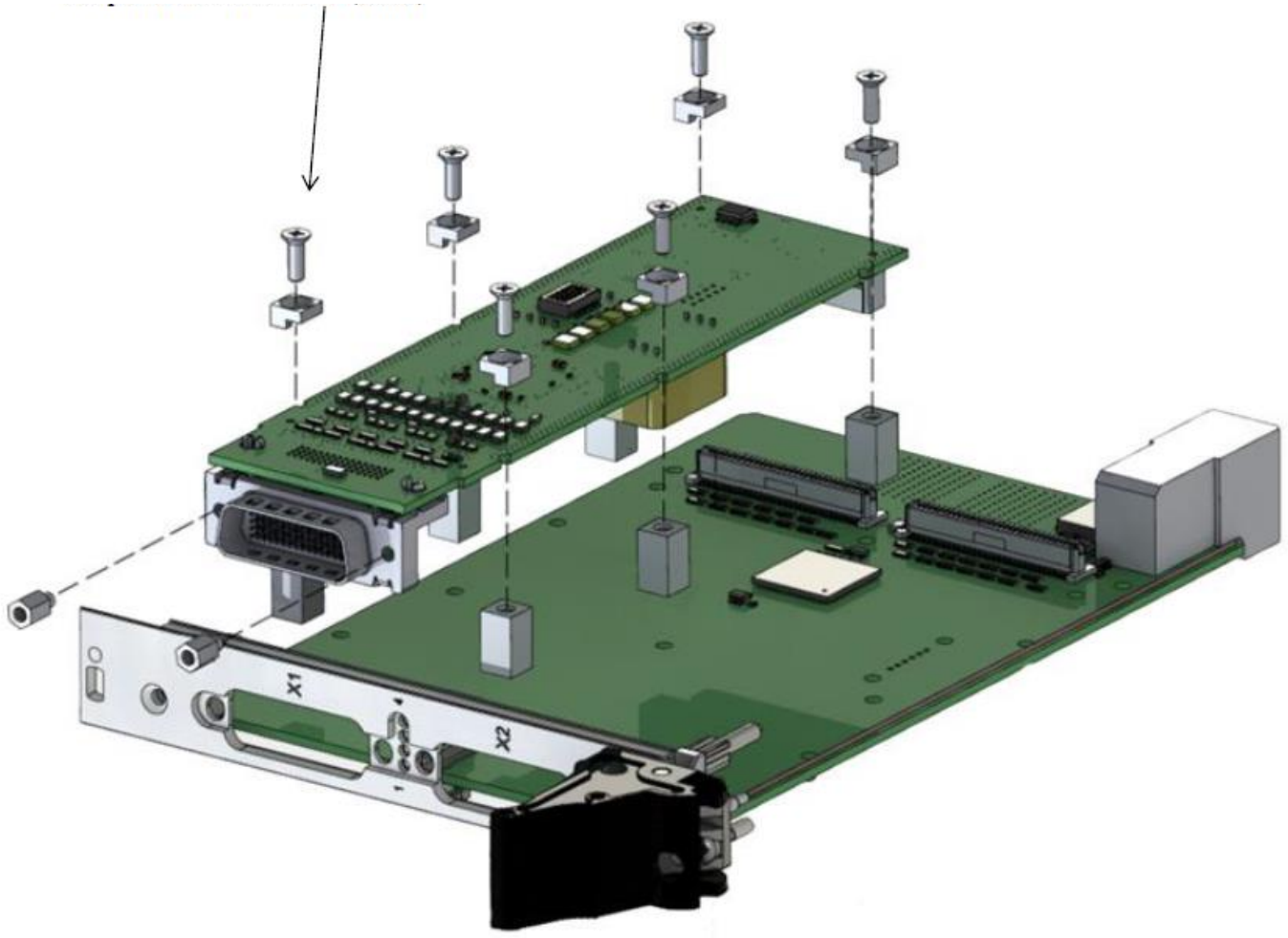
Warning! When ordering the /Coated option, the DIC551 module obtains conformal coating and the installed mezzanines should have conformal coating (/Coated option).

Version DIC551RC	Mezzanine version MIC1001	Mezzanine version MIC1002	Mezzanine version MIC1003	Mezzanine version MIC1004	Panel installed to DIC551RC	Additional panel for output of 3 COM-ports (741424.025) pcs
DIC551RC-01	-	-	-	-	741238.001	
DIC551RC-01	-	MIC1002-01	-	-	741238.001-02	1
DIC551RC-01	MIC1001-01	MIC1002-01	-	-	741238.001	1
DIC551RC-01	-	MIC1002-01	MIC1003-01	-	741238.001	1
DIC551RC-01	-	MIC1002-01		MIC1004-01	741238.001	1
DIC551RC-01	-	MIC1002-01 (2 pcs.)	-	-	741238.001-02	2
DIC551RC-01	MIC1001-01	-	MIC1003-01	MIC1004-01	741238.001	
DIC551RC-02	MIC1001-02	MIC1002-02	MIC1002-02	MIC1002-02	741238.001-03	
DIC551RC-02	-	-	-	-	741238.001-03	

Warning! When ordering the /Coated option, the DIC551RC module obtains conformal coating and the installed mezzanines should have conformal coating (/Coated option).

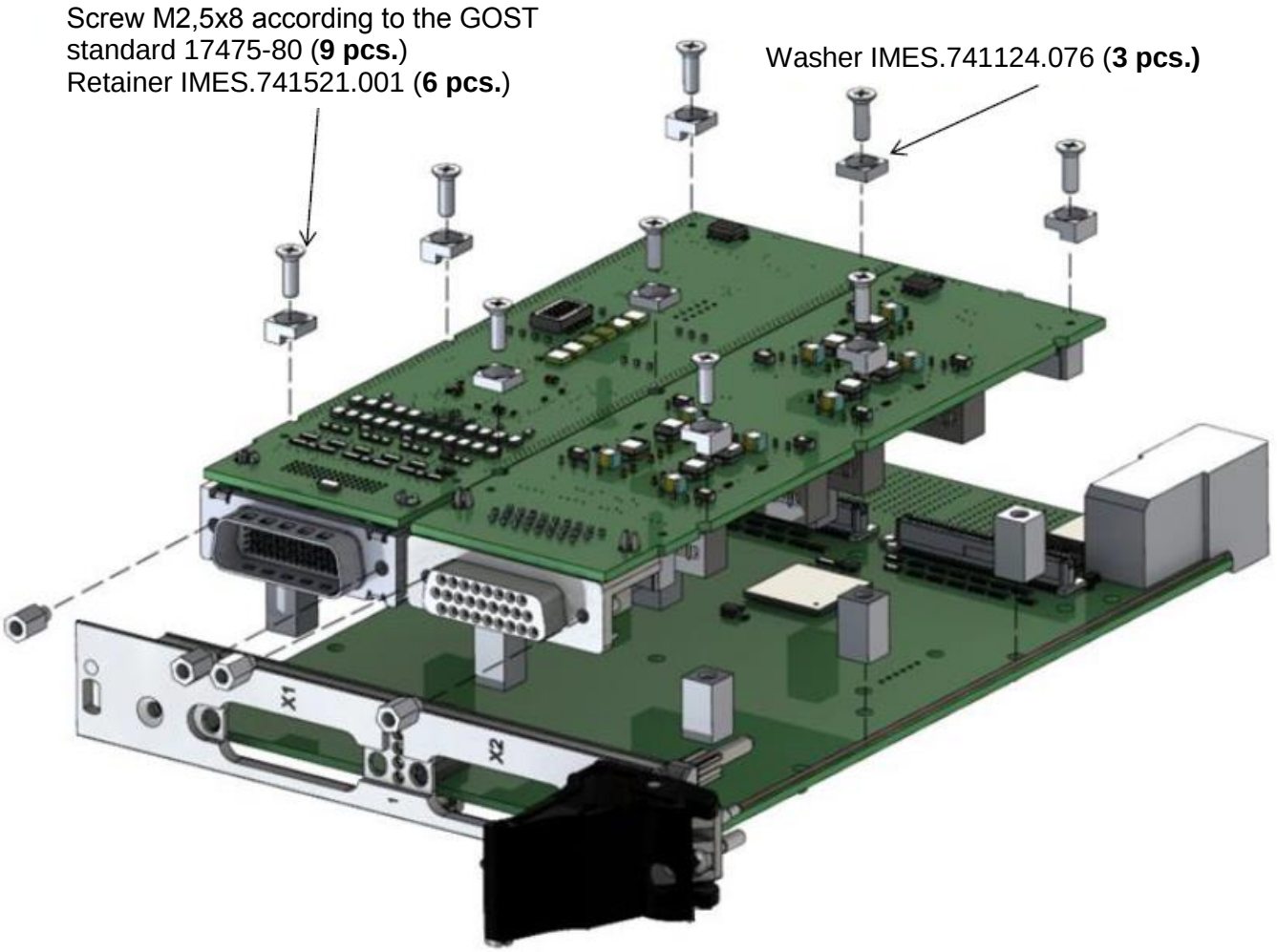
ANNEX C
Assembling diagram of DIC551 Module with one mezzanine

Screw M2,5x8 according to the GOST standard 17475-80 (**6 pcs.**)
Retainer IMES.741521.001 (**6 pcs.**)



Mezzanine module and front panel are shown schematically.
ATTENTION! When ordering the /Coated option, the DIC551 module receives conformal coating and the installed mezzanine should have conformal coating (/Coated option).
The fasteners should be fixed in accordance with the industry-specific standard 107.460091.014-2004 type 23A.

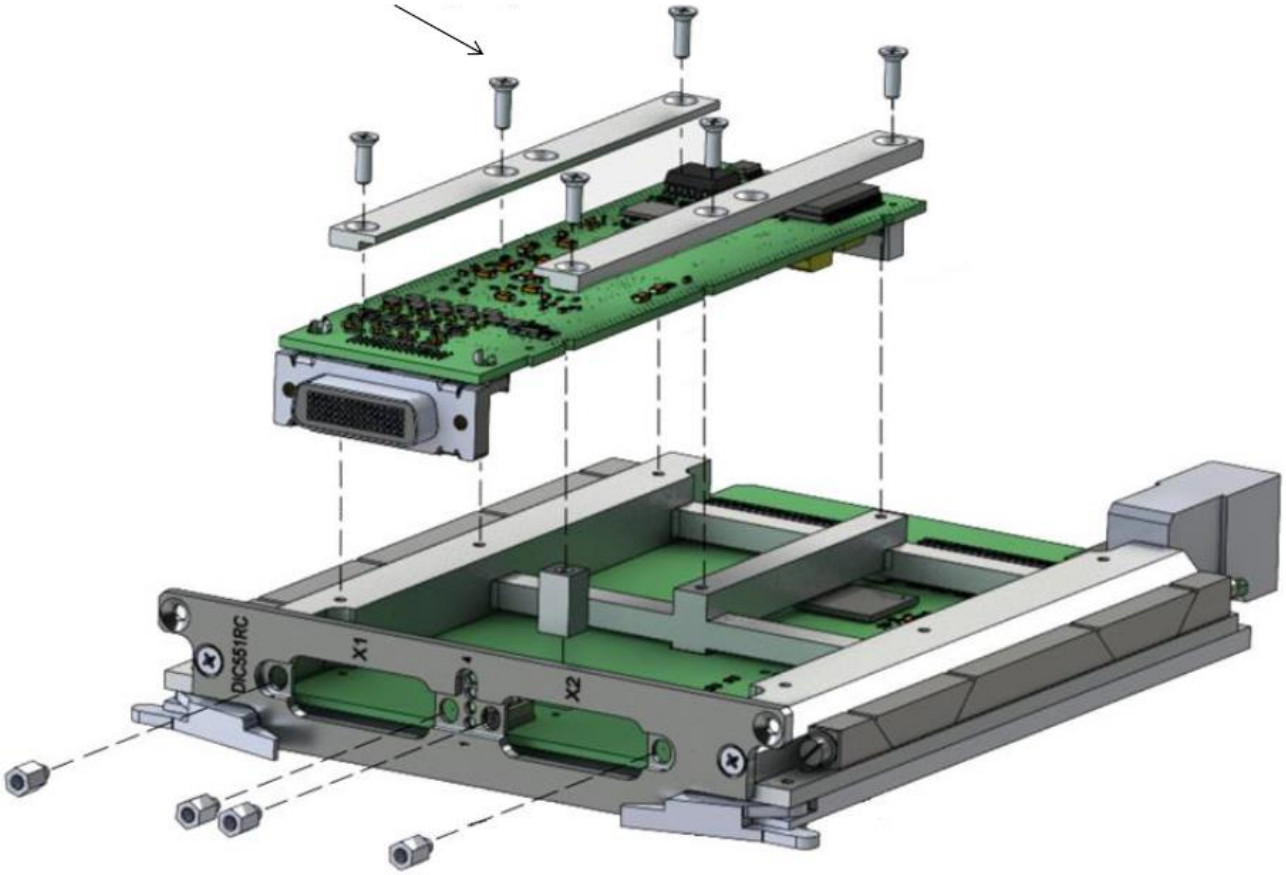
ANNEX D
Assembling diagram of DIC551 Module with two mezzanines



Mezzanine module and front panel are shown schematically.
ATTENTION! When ordering the /Coated option, the DIC551 module receives conformal coating and the installed mezzanine should have conformal coating (/Coated option).
The fasteners should be fixed in accordance with the industry-specific standard 107.460091.014-2004 type 23A.

ANNEX E
Assembling diagram of DIC551RC with one mezzanine

Screw M2,5x8 according to the GOST standard 17475-80 (**6 pcs.**)
Plate IMES. 741522.004 (**2 pcs.**)

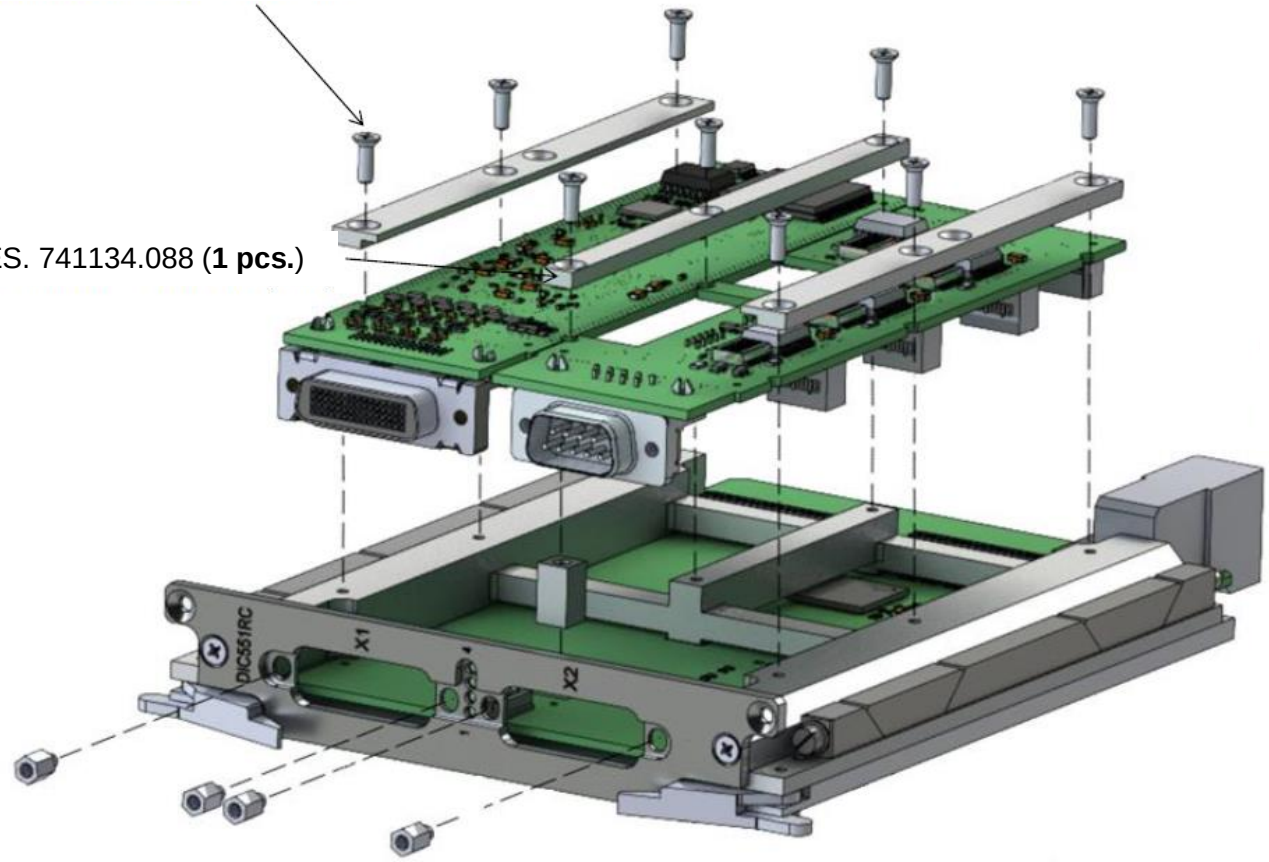


Mezzanine module and front panel are shown schematically.
ATTENTION! When ordering the /Coated option, the DIC551RC module receives conformal coating and the installed mezzanine should have conformal coating (/Coated option).
The fasteners should be fixed in accordance with the industry-specific standard 107.460091.014-2004 type 23A.

ANNEX F
Assembling diagram of DIC551RC with two mezzanines

Screw M2,5x8 according to the GOST standard 17475-80 (**6 pcs.**)
Plate IMES. 741522.004 (**2 pcs.**)

Plate IMES. 741134.088 (**1 pcs.**)



Mezzanine module and front panel are shown schematically.
ATTENTION! When ordering the /Coated option, the DIC551RC module receives conformal coating and the installed mezzanine should have conformal coating (/Coated option).
The fasteners should be fixed in accordance with the industry-specific standard 107.460091.014-2004 type 23A.

REVISION RECORD LIST

Revision record list

Rev.	Numbers of sheets (pages)				Total amount of sheets (pages) in the document	Document #	Reference number of the supporting document and date	Signed	Date
	Changed	Replaced	New	Canceled					
-			66		66	IC151391			October 12, 2015
1.1	-	all	1	-	67	NC150486			February 10, 2016
1.2		all			70	NC160680			June 01, 2016

ANNEX G
DISCLAIMER

This Disclaimer contains special operating conditions of Fastwel in the following areas: intellectual property, warranty policy, conditions of the order and delivery.

1 INTELLECTUAL PRORETY

1.1 If any infraction, interference, improper use, illegitimate exploitation and/or violation of the industrial and/or intellectual property rights of any third party and/or property, exploitation during the use of Fastwel Embedded Module will take place – Fastwel does not guarantee to replace the materials, computer programs, procedures or equipment affected by the complaint and under no circumstances doesn't bear responsibility in any form for possible refusal in case of such a replacement.
1.2 Use of the Fastwel products as well as the objects of intellectual property containing in them, in the ways and for the purposes, not provided by the present user manual and datasheet isn't allowed without preliminary written approval of Fastwel.
1.3 Fastwel is not responsible for possible incidents and losses, related to the operation of end devices, in which the original Fastwel equipment is used.

2 WARRANTY POLICY

2.1 When the detected flaws in an element can be corrected without decreasing the foreseen technical features and functionality for it, User may demand Fastwel the urgent correction of the failures in additionally agreed period and an increasing of the period of the guarantee of the element equal as the time elapsed from the formal request to repair the failures, until the receipt of the repaired element. All costs associated to the correction of failures, included those of assembly, dismantle, transport, tests, etc, if they exist, shall be prosecuted according the Warranty Policy of Fastwel.

3 ORDER AND DELIVERY CONDITIONS

3.1 The general rule is that all Fastwel equipment prices are determined with due consideration of delivery under the EXW terms and conditions (Incoterms 2010). Delivery of the products under other terms and conditions should be preliminary agreed and stated in writing between the parties.
3.2 Unless otherwise expressly agreed with Fastwel, all the deliveries of Fastwel equipment will be carried out only after the official purchase order is obtained and provided that the ordered products have been prepaid in full. Other terms and conditions of cooperation should be made in writing.
3.3 Any delivery of Fastwel electronics is submitted with the right package in accordance with the current rules and standards in the Member States of the European Economic Area. The purchaser independently bears all risks regarding the compliance of package and marking of Fastwel products with legislation requirements being in effect at the place of purchased products destination (in the buyer's country). The specified condition excludes unequivocally any liability of Fastwel for possible non-compliance of package and marking of products with the requirements of legislation of the country of products destination.
3.4 In general, all components of the supply are properly protected with respect to freight, in order to avoid any damage to the supply, third parties, environmental damages or unrelated goods, as consequence of wrong packaging.
3.5 Each package unit is labeled on the exterior area with the indications of product's Part Number and Serial Number.
3.6 The support documents for the order should be made either in English or in Russian unless otherwise agreed between parties in writing.
3.7 Fastwel does not pay penalties and does not cover costs associated with delay in the delivery of the products caused by actions of the third parties, force-majeure etc. - Fastwel doesn't bear any responsibility for non-execution or inadequate execution of the obligations in a case when it is caused by actions of the third parties (for example producers or suppliers of accessories), force majeure etc.
3.8 Fastwel declares that independently and at any time without damage, it has an exclusive right to define and change functionality architecture, bill of materials of its products without any preliminary coordination and approvals of the third parties.

4 OTHER CONDITIONS

4.1 Fastwel has the obligation to respect the current Russian legislation (including, but not limited to environmental, labor, social laws) in each moment and to apply it to its embedded electronics considering all and each execution phase, that is to say, from the design until the commissioning and subsequent maintenance. In this regard Fastwel is not liable to the user or other persons in connection with possible changes of the company's rules (including, but not limited to warranty, ordering policy) caused by changes of the Russian legislation.
4.2 Unless otherwise expressly agreed in writing, Fastwel provides no training for assembly\installation\adjustment\operation of its equipment.