KIC551

Interface Module

in 3U CompactPCI Serial format

User Manual

Rev. 003

September 2021

The product described in this manual is compliant with all related CE standards.

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Revision Record

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This User Manual (hereinafter referred to as the “User Manual” or “Manual”) is applicable to the KIC551 interface module with forced cooling and KIC551RC interface module with conduction cooling (hereinafter referred to as the device or KIC551/KIC551RC) and contains description, principle of operation, technical specs of KIC551/KIC551RC, as well as establishes rules of its operation.

You should read this User Manual before using the product.

The manufacturer shall not be liable for any potential loss or damages, caused by non-compliance of recommendations and requirements given in this User Manual.

Attention!

All the operations with this device should be performed by trained engineers and technicians in strict adherence to the instruction manuals.

Ownership rights

Safety requirements

This Fastwel Group's product is developed and tested for the purpose of ensuring compliance to the electric safety requirements. Its design provides long-term trouble-free operation. The service life of the product can be significantly reduced due to the improper handling during unpacking and installation. Therefore, in the interests of your safety and in order to ensure proper operation of the product, you should follow the recommendations below.

Conventions

Caution, High Voltage!

This sign and text warn of the dangers associated with electrical discharges (> 60 V) when touching the device or any part of it. Failure to follow the precautions mentioned or prescribed in the regulations may endanger your life or health, and may result in damages to the equipment. Please also read the below subparagraph dedicated to the rules for working with high voltage.

Attention! Static-Sensitive Device!

This sign and text indicate that the electronic boards and their components are sensitive to static electricity, so proper care should be taken when handling this device and performing inspections to ensure integrity and functionality of the device.

Attention! Hot surface!

This sign and text warn of the danger associated with touching hot surfaces of the device.

Attention!

This sign is aimed at drawing your attention to aspects of this User Manual that, if not fully understood or ignored, may endanger your health or cause damages to the equipment.

Note

This sign is used to specify text fragments that should be read carefully.

Safety requirements

This Fastwel Group product has been developed and tested to ensure compliance with electrical safety requirements. Its design provides long-term fail-safe operation. The product's life cycle may be significantly shortened due to mishandling during unpacking and installation. Therefore, for your own safety and for ensuring proper operation of the device, you should follow the recommendations given below.

Rules for safe handling with high voltage

Attention!

All the operations with this device should only be performed by personnel with sufficient qualifications.

Caution, High Voltage!

Before installing the board in the system, make sure that the mains power supply is off. The same also applies to the installation of expansion boards.

There is a serious risk of electric shock during installation, repairs, and maintenance of the device, so always unplug the power supply cord while carrying out of works. The same also applies to the other power supply cables.

Board Handling Instructions

Static-sensitive device!

Electronic boards and their components are sensitive to static electricity. Therefore, special attention should be given when handling these devices to ensure their safety and operability.

✓ Do not leave the board in the non-operating position without protective packaging.

✓ If possible, always work with the board in workplaces protected against static electricity. Should this not be possible, the user should remove the static charge before touching the product with their hands or tools. The best way to do so is by touching any metal part of the system enclosure.

✓ Since the product is equipped with batteries to power the memory and real-time clock, avoid placing the board on conducting surfaces such as anti-static mats or sponges. They can cause short circuits and damage the battery and the board's conducting circuits.

General rules of usage

✓ In order to keep the warranty, the product must not be altered or changed in any way. Any changes and improvements unauthorized by Fastwel Group other than those contained in this User Manual or received from the technical support service of Fastwel Group in the form of a set of instructions for their implementation will void the warranty.

✓ This device should be installed and connected only to systems that meet all necessary technical and climatic requirements. This also applies to the operating temperature range of a particular version of the board. You should also consider the temperature limits of the batteries installed on the board.

✓ This device should be installed and connected only to the systems that meet all the necessary technical and climatic requirements. This also applies to the operating temperature range of a specific version of the module. Temperature limits of the batteries installed on the module should also be considered.

✓ Follow the instructions in this User Manual only when performing all necessary installation and configuration operations.

✓ Retain the original packaging for storing products in the future or to transport in case of a warranty claim. If it is necessary to transport or store the board, pack it the same way as it was packed at the time of receipt.

✓ Proceed with extra caution when handling and unpacking the device. Follow the instructions in the Chapter **Transportation, Unpacking and Storage** below.

MANUFACTURER'S WARRANTIES

Warranty liabilities

Fastwel Co. Ltd. (Fastwel), warrants that its standard hardware products will be free from defects in materials and workmanship under normal use and service for the currently established warranty period. Fastwel's only responsibility under this warranty is, at its option, to replace or repair any defective component part of such products free of charge.

Fastwel neither assumes nor authorizes any other liability in connection with the sale, installation or use of its products. Fastwel shall have no liability for direct or consequential damages of any kind arising out of sale, delay in delivery, installation, or use of its products.

If a product should fail through Fastwel's fault during the warranty period, it will be repaired free of charge. For out of warranty repairs, the customer will be invoiced for repair charges at current standard labor and materials rates.

Warranty period

The warranty period for the manufacturer's products is 36 months from the date of sale (unless otherwise provided by the delivery agreement).
For customized products, the warranty period is 60 months from the date of sale (unless otherwise provided by the delivery agreement).

Limitation of warranty obligations

The above warranty does not apply to:

- the products (including software) that have been repaired or modified by the employees who do not represent the Manufacturer. The exception is when the Consumer has made repairs or made changes to the product strictly in accordance with the instructions previously agreed and approved by the Manufacturer in writing;

- the products which have failed because of an inappropriate change of a polarity sign (to the opposite one) of the power supply source, incorrect operation, transportation, storage, installation, mounting or accident.

Procedure for returning products for repairs

Sequence of actions when returning products for repairs:

- contact the Product Manufacturer or Supplier for return material authorization for the product;
- attach to the returned product the fault identification report made in the form adopted by the Consumer, indicating the list of circumstances and signs of malfunction;
- place the product in the consumer packaging of the Manufacturer (antistatic packaging) and cardboard packaging (box)), in which the product was delivered to the Consumer. If there is no antistatic packaging, the Consumer loses the right to warranty service unilaterally;
− the Consumer pays all the expenses related to the delivery of the product to the Supplier.

Transportation, Unpacking and Storage

Transportation

The modules should be transported in the separate manufacturer's packaging (container), consisting of an individual antistatic packaging and a cardboard box, in closed transport (road, rail, air in heated and sealed compartments) under storage conditions 5 according to the GOST standard 15150-69 or under storage conditions 3 for sea transportation.

Transportation of packaged modules should be carried out in accordance with the rules of transportation of goods currently valid for this type of transport.

During handling operations and transportation, the packaged modules should not be subjected to sudden shocks, drops, impacts and precipitation. The packaged modules should be placed on the vehicle in such a way as to preclude their further movements.

Unpacking

Before unpacking, after transportation at negative ambient temperatures, the modules must be kept for 6 hours under storage conditions 1, in accordance with the GOST standard 15150-69.

Do not place the packed modules near any heat sources before unpacking.

When unpacking the modules, it is necessary to observe all precautions to ensure their safety, as well as marketable condition of manufacturer's consumer packaging.

When unpacking, it is necessary to check the modules for any external mechanical damages after transportation.

Storage

Storage conditions of the modules 1 in accordance with the GOST standard 15150-69.

1 Description and operation of KIC551/KIC551RC

1.1 Purpose of KIC551/KIC551RC

Names of the products described in this User Manual: KIC551 interface module (product designation: IMES.421459.551) and KIC551RC interface module (product designation: IMES.467449.003).

The KIC551 interface module is a high-speed programmable switch for PCI Express and Gigabit Ethernet interfaces and is designed to transfer packets between peripheral slots and an external device (see subparagraph 1.4).

The KIC551 is designed so as to provide consumers with an integrated 3U CPCI Serial solution for the use in real-time systems, manufacture control, high-speed data acquisition and data processing. KIC551 serves as an extension to the lineup of 3U CPCI modules manufactured by Fastwel Group.

The KIC551RC interface module with a conduction-type cooler is based on KIC551 and is used for building powerful special purpose ultra-reliable systems.

To remove heat from the KIC551RC, there is a specially designed heat removal cassette in accordance with the CompactPCI Serial Mesh Backplane specification, PICMG 2.20 R 1.0.

Thereafter, the modules are named either as KIC551/KIC551RC or “the module”. In the text, where it is necessary to indicate individual characteristics of the modules, it will be noted that we are referring to the specific module version, and not to the module in general.

1.2 Technical specs of KIC551/KIC551RC

■ PCIe Gen 3 interface:

▪ Support of Peer-to-Peer and Multicast operation modes;

▪ Possibility of slexible port configuration in x1, x4 and x8 modes;

▪ Possibility of Upstream port switching;

▪ Support of 54 x channel /12 ports PCIe Gen 2/3 switching;

▪ Switching of up to eight PCIe ports, routed to the backplane with PCIe optical port, routed to the front panel.

■ Fiber Optic (KIC551-01 and KIC551RC-01):

▪ bus width: 8 x PCIe;

▪ Support of GEN3 bandwidth (8 Gb/sec);

▪ MPO 12 Fiber 50um MMF cable connection (2 x cables);

▪ Maximum connection length: 50 m;

▪ Maximum Fiber Optic PCI Express connection rate: 64 GT/s*.

■ 1 Gbit Ethernet interface:

▪ Switching of 8 x 1000BASE-T channels, routed to the backplane with the 1000BASE-T port on the front panel;

▪ Insulation strength: min. 100 V for channels, routed to the backplane;

▪ Insulation strength: min. 500 V for the channel, routed to the front panel.

■ SFI 10 Gbit interface:

▪ Connection of SFP+ modules;

▪ Providing a high-speed data transmission channel.

* Abbreviation that stands for “gigatransfers per second”

■ **STM32F207 integrated advanced ARM-based MCU (hereinafter referred to as the microcontroller of MCU):**

▪ Control of the supplied power;

▪ Support of the real-time clock;

▪ Managing the settings of optical modules;

▪ Acquisition and processing data from Hardware Monitor;

▪ Monitoring FPGA performance;

▪ Function of updating firmware for all integrated equipment, both in manual (via the Fast Ethernet channel) and in automatic modes (according to a previously started algorithm).

■ **Configuration FPGA:**

▪ Control of the supplied power;

▪ Control of the managing MCU performance;

▪ Support of botting from the backup ROM in the event of WD-timer actuation;

▪ PCIe switch configuration and booting;

▪ Support of firmware update via the Ethernet channels;

▪ Indication of KIC551/KIC551RC performance.

■ **Supported standards:**

▪ PICMG® CPCI-S.0 R1.0 March 2, 2011;

▪ PCI Express® 3.0 specification;

▪ PCI Express® External Cabling Specification Revision 1.0 January 4, 2007;

▪ PCI Express® Base Specification Revision 2.0 December 20, 2006;

▪ SFF-8431 Specifications for Enhanced Small Form Factor Pluggable Module SFP+.

■ **Power supply:**

▪ Supply voltage: + 12 V, + 5 V_standby.

■ **Operating temperature range of KIC551:**

▪ Industrial version: from - 40 to +85 °C;

▪ Commercial version: from 0 to +70 °C.

■ **Operating temperature range of KIC551RC:**

▪ from -50 to +85 °C.

■ **Humidity:**

▪ up to 80%, non-condensing;

▪ up to 98%, non-condensing for \Coated option.

■ **Resistance to vibration/single shocks/multiple shocks:**

▪ 5 g/50 g/25 g (KIC551);

▪ 6 g/75 g/15 g (KIC551RC).

■ **MTBF:**

▪ Min. 100,000 hours (KIC551);

▪ Min. 120,000 hours (KIC551RC).

■ **Weight:**

▪ Max. 0.65 kg (KIC551);

▪ Max. 1.0 kg (KIC551RC).

1.3 Structural features of KIC551RC

The technical specifications for both KIC551 and KIC551RC are listed in subparagraph 1.2; Features of the KIC551RC module are as follows:

▪ conduction heat removal cassette is used instead of the finned heatsink;

▪ KIC551RC correposnds to the IMES.469555.002 TU specifications.

For more details on KIC551RC, please see subparagraphs 1.6 and 1.8.

1.4 Structure and functioning of KIC551/KIC551RC

KIC551/KIC551RC is installed into a system slot of the backplane and performs switching of PCIe packets between peripheral slots and and an external device over the PCIe optical interface. The module is additionally equipped with a 10 Gbit Ethernet controller included in the list of PCIe devices and makes it possible to transfer data via the channel displayed on the front panel. Separately from the PCIe packet switching subsystem, a 1 Gbit Ethernet switch is installed on the KIC551 / KIC551RC module, which makes it possible to control individual system modules, as well as data exchange within the single-star topology. KIC551/KIC551RC can also be used to increase the bandwidth of peripheral slots over the PCIe lines if the processor module does not support x4 and x8 buses on peripheral slots.

1.5 Ordering information for KIC551

KIC551 is manufactured in accordance with Table 1.1:

Table 1.1 – Versions of KIC551

Name	Number	Ordering name	Note
KIC551 Interface Module	IMES.421459.551	KIC551-01-C	PCIe and Ethernet switch with PCIe optical interface, 4HP; from 0 to +70 °C.
	IMES.421459.551-01	KIC551-01-I	PCIe and Ethernet switch with PCIe optical interface, 4HP; from -40 to +85 °C.
	IMES.421459.551-02	KIC551-02-C	PCIe and Ethernet switch without PCIe optical interface, 4HP; from 0 to +70 °C.
	IMES.421459.551-03	KIC551-02-I	PCIe and Ethernet switch without PCIe optical interface, 4HP; from -40 to +85 °C.

For ordering KIC551 with a conformal coating, you will need to add \ Coated option to the above. E.g. KIC551-01 \ Coated.
Photo of KIC551 is shown in Fig. 1.1.

1.6 Ordering information for KIC551RC

KIC551RC is manufactured in accordance with Table 1.2:

Table 1.2 – Versions of KIC551RC

Name	Number	Ordering name	Note
KIC551RC Interface Module	IMES.467449.003	KIC551RC-01	PCIe and Ethernet switch with PCIe optical interface, equipped with a conduction-type cooling unit, 5HP.
	IMES.467449.003-01	KIC551RC-02	PCIe and Ethernet switch without PCIe optical interface, equipped with conduction-type cooling unit, 5HP.

For ordering KIC551RC with conformal coating you need to add a \Coated option to the above (e.g., KIC551RC-01\Coated).
Photo of KIC551RC is shown in Fig. 1.6.

1.7 Location of components and overall dimensions of KIC551

The following figures will help identify the components and understand their relationships and functions. The KIC551 versions may have slight differences, which are not reflected in the diagrams and photographs.

1.7.1 Overall view of KIC551

Fig. 1.1 show the external view of KIC551-01 with the installed finned heatsink (4HP). The front panel of KIC551-02 has no connectors of PCIe optical interface (the differences between the versions of the KIC551 module are shown in Table 1.1 – Versions of KIC551), specified on KIC551-01 as RX and TX (see Fig. 1.3 and Fig. 1.4).

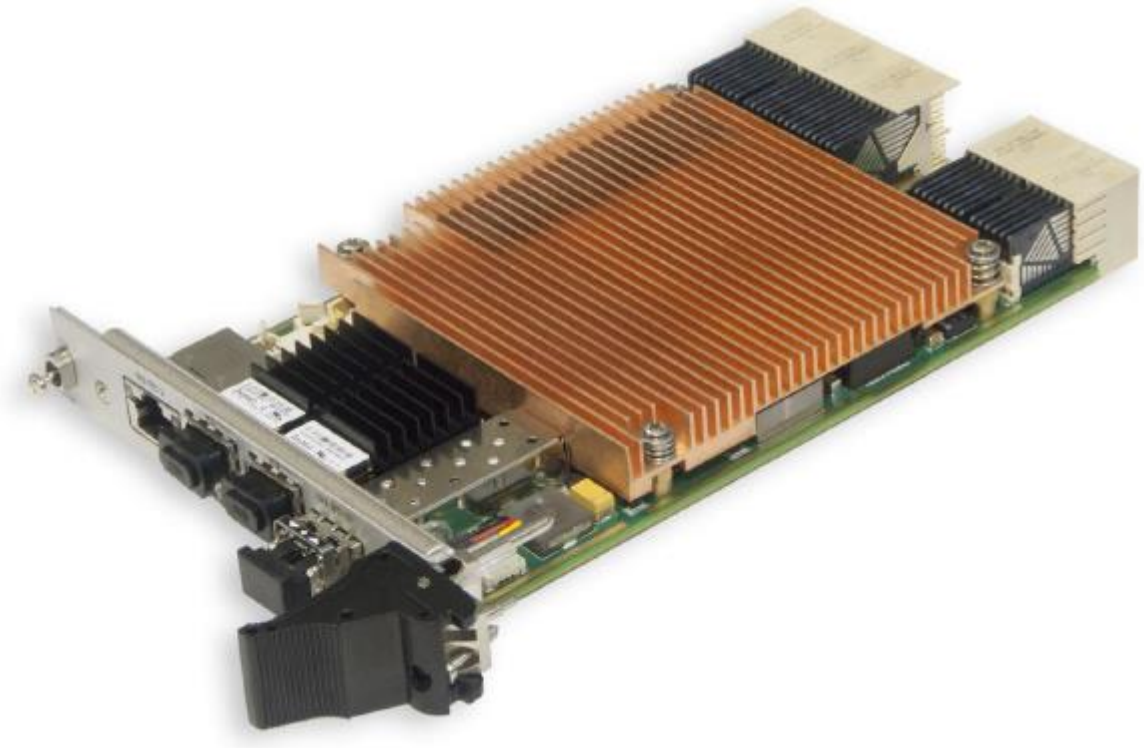


Fig. 1.1 – KIC551-01

The appearance of the module versions may slightly differ from the one shown in figure.

1.7.2 Location of main components of KIC551

Fig. 1.2 shows the top side of the KIC551-01 module (heatsink is not shown).

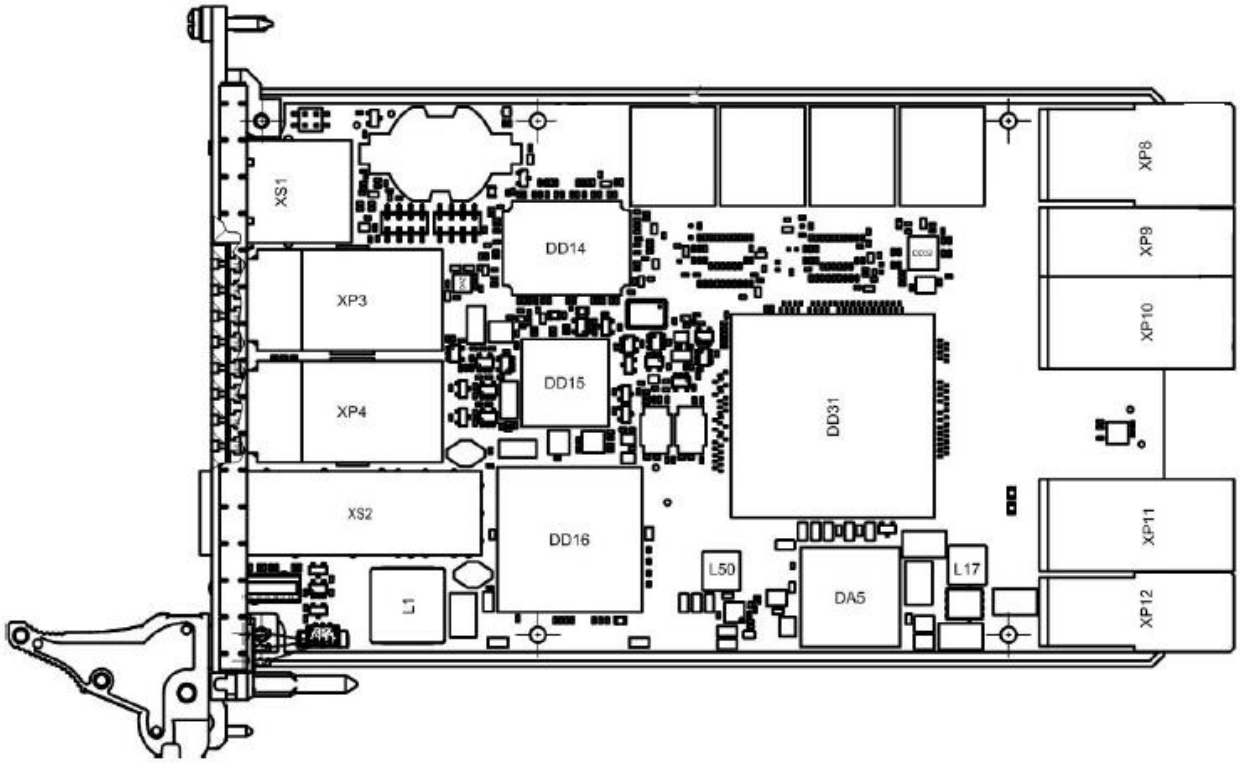


Fig. 1.2 – Location of main components of KIC551, top view (as exemplified by KIC551-01)

The appearance of the module versions may slightly differ from the one shown in figure.

1.7.3 Front panel of KIC551

Fig. 1.3 and Fig. 1.4 show the front panels of KIC551-01 and KIC551-02, respectively.

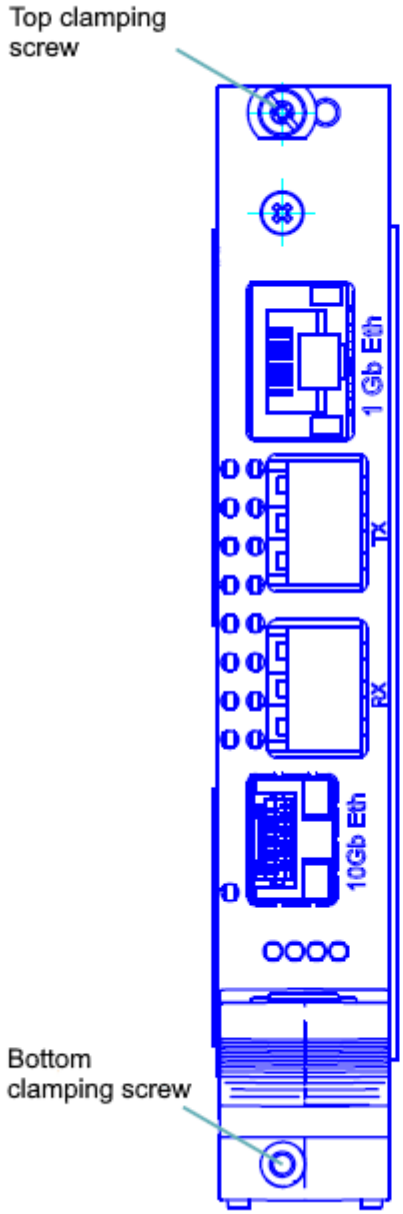


Fig. 1.3 – Front panel of KIC551-01

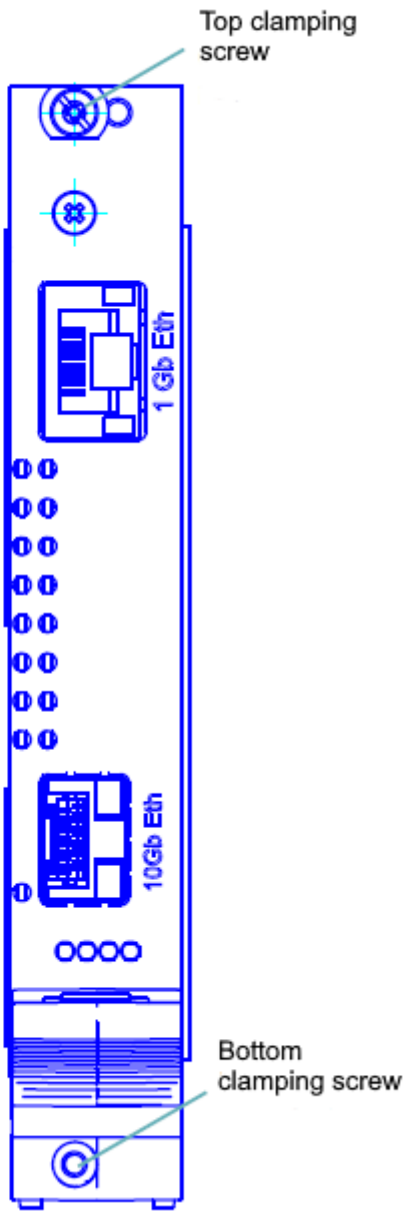


Fig. 1.4 – Front panel of KIC551-02

The appearance of the module versions may slightly differ from the one shown in figure.

The ejector's button (located on ejector's button, see Fig. 1.5) performs mechanical function – it is intended for installation/removal of KIC551 (see subpargraphs 3.7.2 Procedure of KIC551 installation and 3.7.3 Procedure of KIC551 removal).

1.7.4 Overall dimensions of KIC551

Fig. 1.5 demonstrates KIC551-01 with indication of overall dimensions.

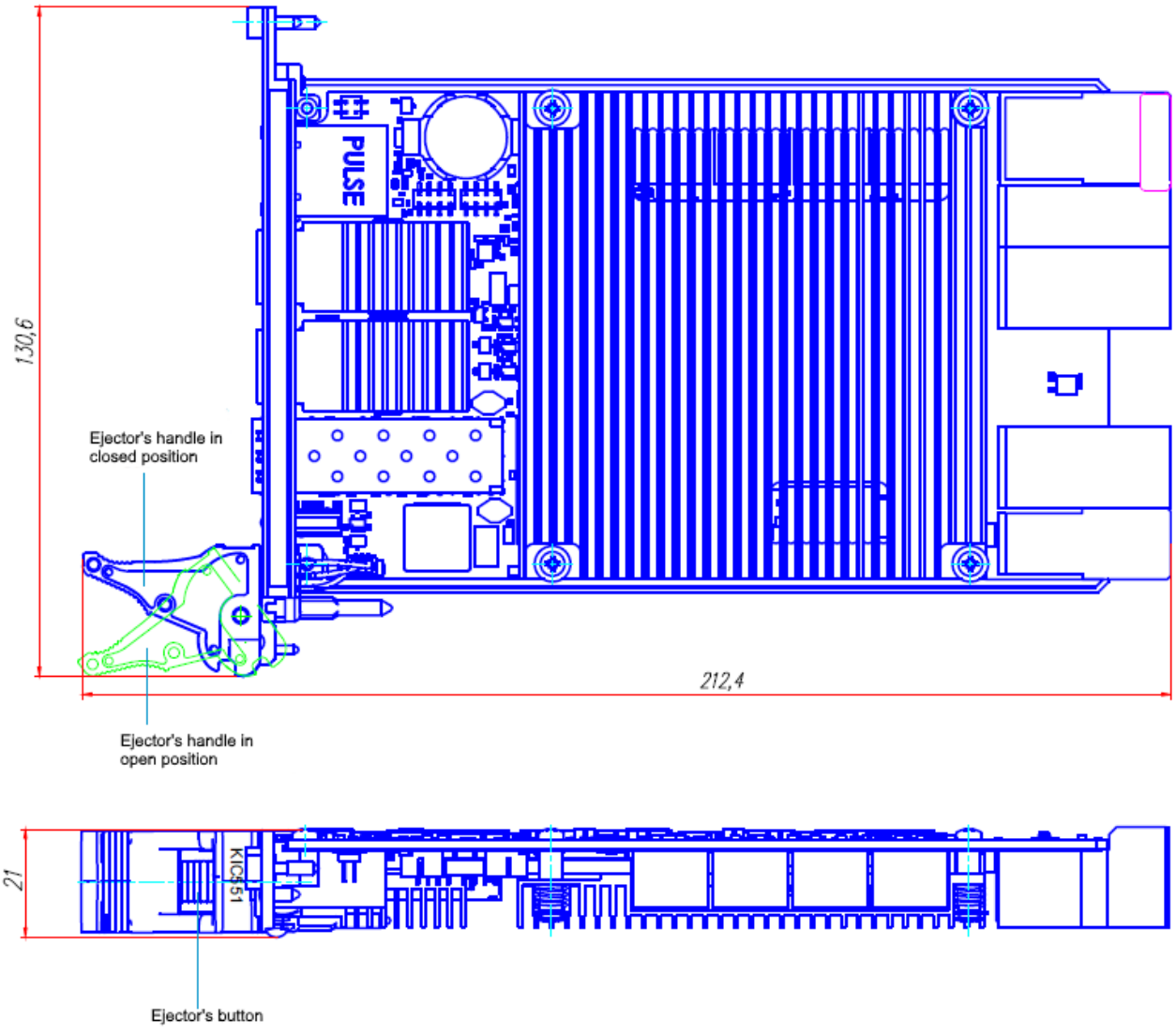


Fig. 1.5 – Overall dimensions of KIC551

1.8 Location of elements and overall dimensions of KIC551RC

1.8.1 Overall view of KIC551RC

Fig. 1.6 demonstrates the external view of KIC551RC-01. As mentioned above, the KIC551 and KIC551RC modules have the same functionality (they differ by type of cooling).
Differences between the front panel of KIC551RC-01 and KIC551RC-02 versions are explained in subparagraph 1.8.2.

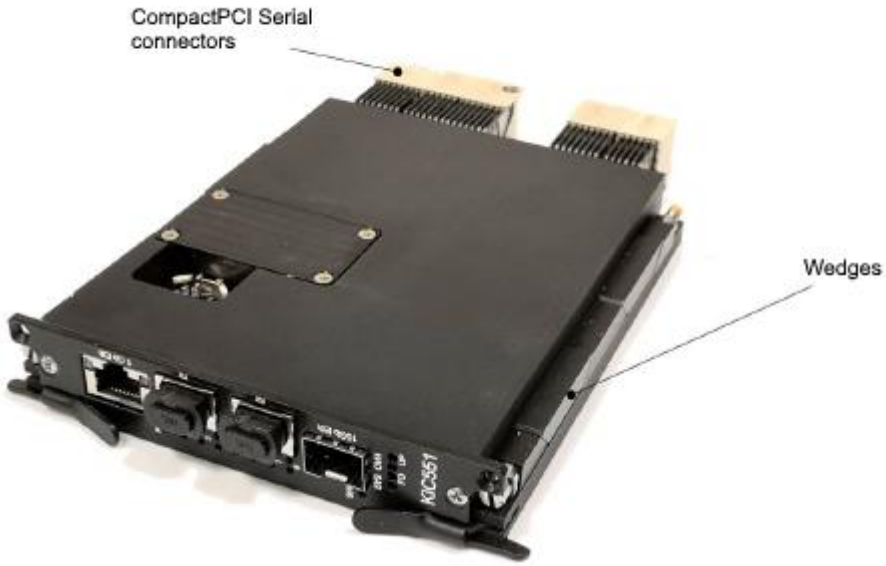


Fig. 1.6 – KIC551RC-01

The appearance of the module versions may slightly differ from the one shown in figure.

1.8.2 Front panel of KIC551RC

Fig. 1.7 shows the front panel of the KIC551RC-01 module specifying structural elements. Same as with the KIC551-02 convection cooling module (Fig. 1.4), the front panel of KIC551RC-02 has no PCIe optical interface connectors (**RX** and **TX**).

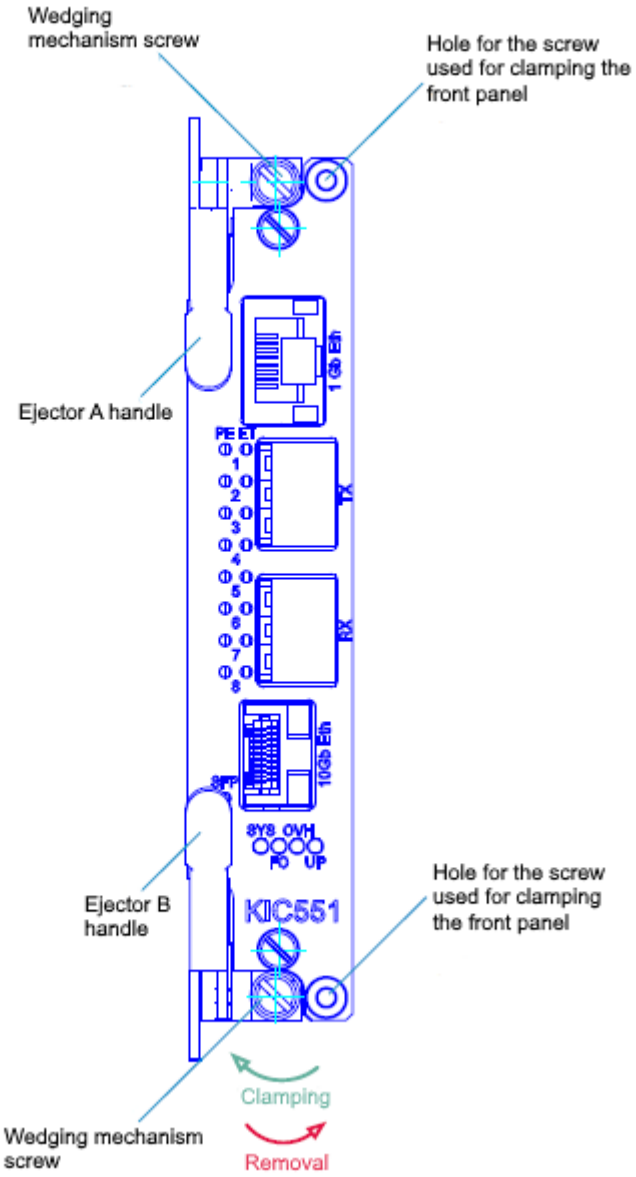


Fig. 1.7 – Main components of KIC551RC front panel (as shown by KIC551RC-01)

The appearance of the module versions may slightly differ from the one shown in figure.

A and B handles are designed for installation/removal of KIC551RC (see subparagraphs 3.7.4 Procedure for installation of KIC551RC and 3.7.5 KIC551RC removal procedure).

1.8.3 Overall dimensions of KIC551RC

Fig. 1.8 shows KIC551RC-01 with indication of overall dimensions.

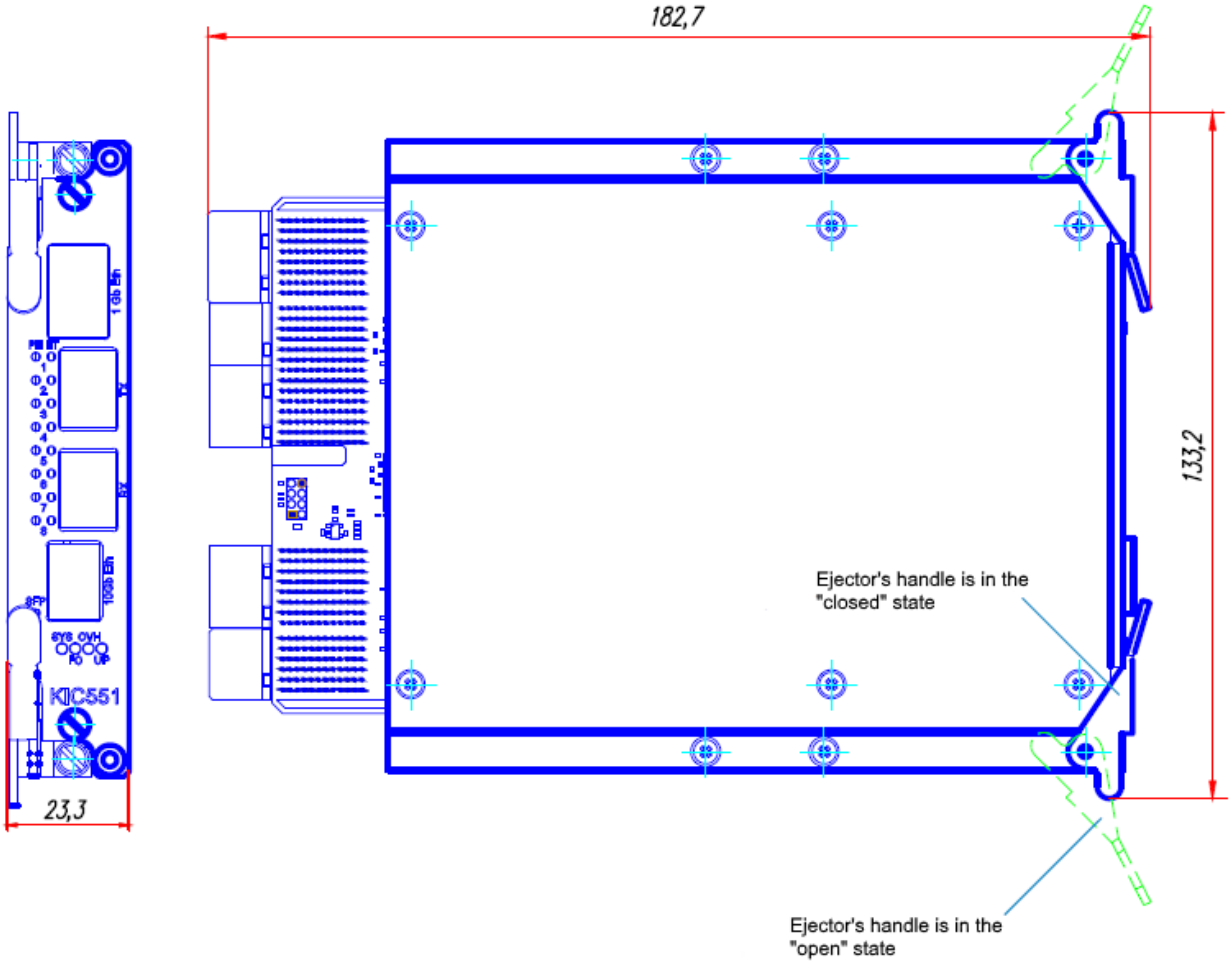


Fig. 1.8 – Overall dimensions of KIC551RC

1.9 Delivery checklist of KIC551/KIC551RC

The delivery checklist includes the following:

- KIC551 or KIC551RC module;
- package.

1.10 Packaging information

KIC551/KIC551RC placed in an antistatic bag, is supplied in the box with overall dimensions of 350 x 260 x 70 mm.

Table 1.3 – Packed weight of KIC551 and KIC551RC

Name	Packed module weight, no more than, g
KIC551	1000
KIC551RC	1200

Note

Retain the antistatic bag and consumer packaging in their original forms till the end of the warranty period.

2 Description and operation of subsystems of KIC551/KIC551RC

2.1 Block diagram

The block diagram for KIC551/KIC551RC is shown in Fig. 2.1.

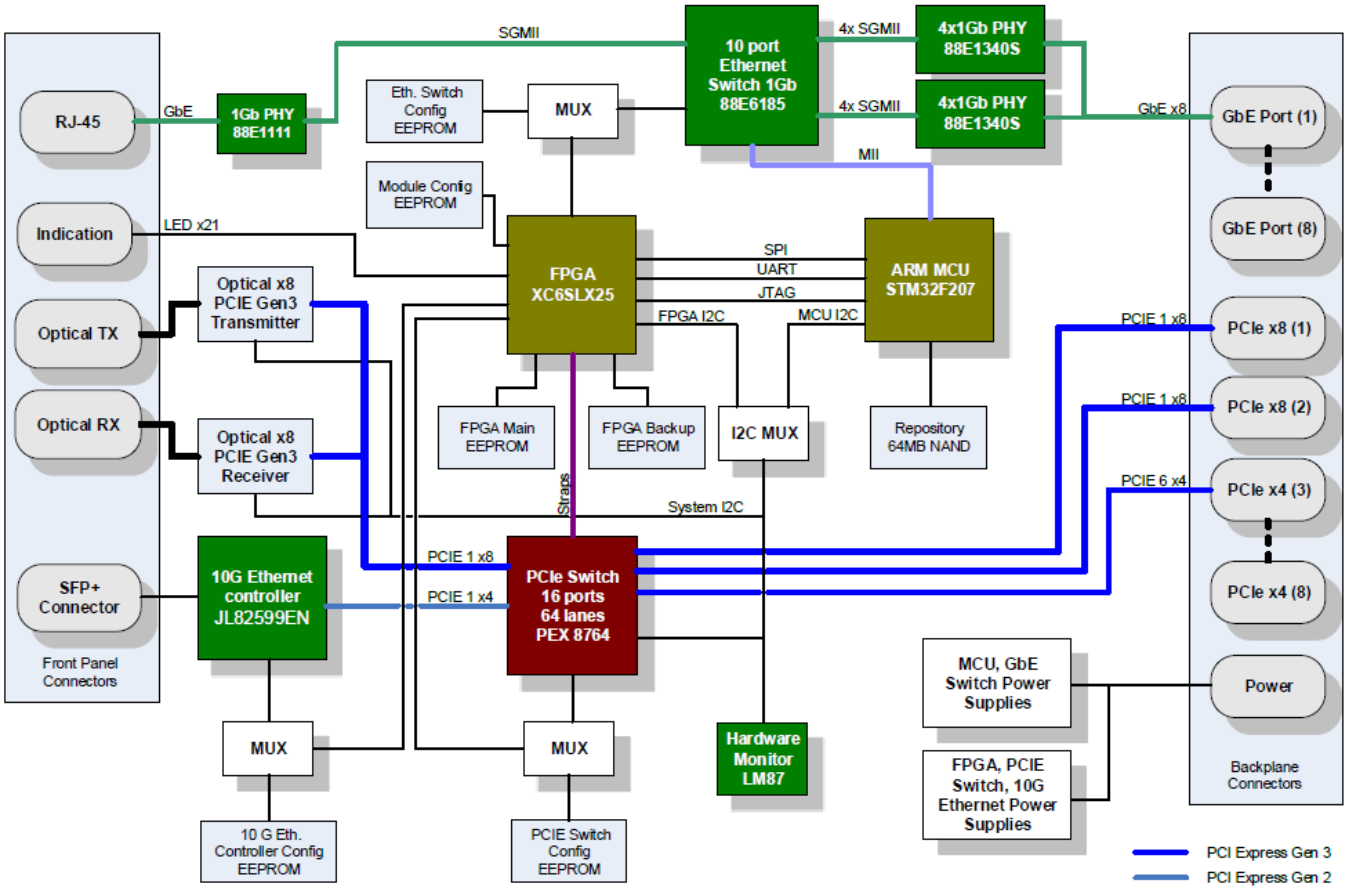


Fig. 2.1 – Block diagram for KIC551/KIC551RC

2.2 Description and operation of functional nodes

2.2.1 10 Port Ethernet Switch 1 Gbit 88E6185

The switch provides data exchange between the modules in peripheral slots and an external device connected to the front panel of the KIC551/KIC551RC module. SGMII is used as the communications interface with the PHY layer (by **88E1340S** and **88E1111** controllers). Configuration parameters are loaded from ROM via the configuration FPGA.

2.2.2 10 Gbit Ethernet JL82599EN controller

The controller is connected to the PCIe switch over the x4 Gen2 bus. Initialization and loading parameters of controller's registers is performed from ROM via the configuration FPGA. Data exchange with an external device is carried out via SFP+ module with SFI interface.

2.2.3 STM32F207 microcontroller

ARM microcontroller performs the functions of data exchange over MII via the **88E6185** switch for transferring system state data and updating FPGA firmware over SPI and UART channels. The microcontroller also performs the function of temperature and power supply voltage monitoring. The current temperature and voltage values are read through the I^2C channel from the **LM87** sensor. The user is also provided with the ability to switch the integrated I^2C channel by software to the backplane lines.

To support script algorithms, the microcontroller is equipped with a function of nonvolatile real time clock.

To ensure the Ethernet communications link the ported code of TCP/ IP lwIP stack is used. Configuration of PHY **88E1111** and **88E1340S** chips is carried out over the MDIO interface. JTAG interface is used for debugging and setting.

2.2.4 FPGA XC6SLX25

Configuration FPGA Spartan 6 is designed for control of power supply and configuration of operation modes of devices on KIC551/KIC551RC. It enables to implement the functions of loading from backup ROM if the main one is failed, and to recover it if the WD-timer is triggered. It also participates in configuring and updating firmware for PCIe and Ethernet switches.

The KIC551/ KIC551RC module has a nonvolatile memory for storing the preinstalled module's configuration, which can be selected both in automatic mode and by using the integrated microswitch. Manual assignment of the root-port slot by microswitches is also possible.
The WD-timer is set and reset in accordance with the internal FPGA algorithm. In case of a software failure, booting from the backup EEPROM is set, and after FPGA initialization, the main firmware is restored.

The required sequence of supplying power to peripheral devices on the board is implemented in the power control unit.

The FPGA also performs switching of SPI EEPROM lines for initializing **88E6185** and **JL82599EN** controllers and **PEX8764** switch. The primary operation mode – EEPROM outputs are connected to the loading outputs of the relevant circuits. The firmware updating mode makes it is possible to program the firmwares.

The list of FPGA service registers is specified at the end of this User Manual (Annex A).

2.2.5 16 ports/64 lanes PCIe Switch PEX 8764

The switch ensures data exchange between the modules, installed into peripheral slots, PCIe devices on KIC551/KIC551RC and an external connected device. The computer cluster that follows next in the hierarchy can function as the external connected device.
The switch supports Multicast transmission mode, which enables you to broadcast the packet transmitted by the host to multiple peripheral modules. In the same way, a packet sent by a peripheral device can be broadcasted to other peripherals.

2.3 Description of KIC551/KIC551RC module's units

In terms of its functions, the KIC551/KIC551RC module contains the following units:

- PCI Express switch unit;
- Gigabit Ethernet switch unit;
- 10 Gbit Ethernet network controller unit;
- PCI Express optical interface unit;
- Control unit;
- LED unit;
- Synchronization unit;
- Power supply unit.

The units interact with each other according to the diagram below (Fig. 2.2).
Due to the fact that the proper functioning of the system unit depends on the performance of the KIC551 / KIC551RC module, appropriate measures were taken at the time of designing the module to increase the durability of its main units with the possibility of duplication and emergency recovery.
As shown by the diagram, the module can be divided into two independent parts with individual control and power supply system: the top part – PCI Express with control from FPGA and power supplies of the PCI Express switch, FPGA, 10 Gbit Ethernet controller and optical transmitters/receivers, the bottom part – Gigabit Ethernet switch with control from the ARM microcontroller and power supplies of the Gigabit Ethernet switch and STM32F207 microcontroller. Below, these units are shown in more details.

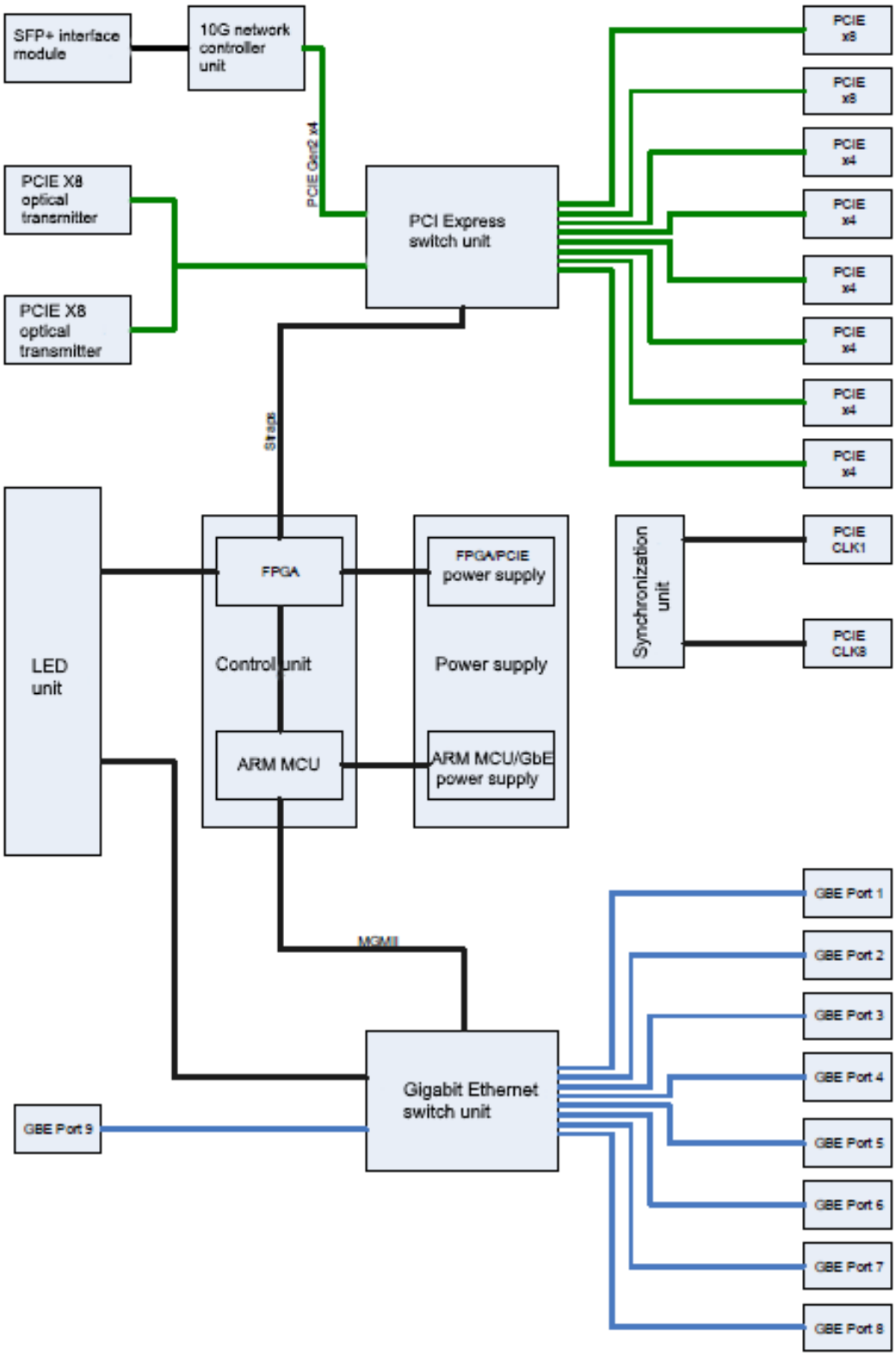


Fig. 2.2 – Diagram of the main units of KIC551/KIC551RC

2.3.1 Control unit

The control unit is designed to perform the following functions:

▪ Configuring the switch units of the module in both manual and automatic modes.

▪ Backing up, storage and update of configurations in module's nonvolatile memory.

▪ Arrangement of an interface for interaction with the user to access the module management resources.

▪ Control of power supply to all the functional blocks of the module and system.

▪ Distribution of control signals for system elements.

▪ Control of the module service life parameters: supply voltage and temperature of critical nodes.

The control unit includes: FPGA Xilinx Spartan-6 XC6SLX25T, MK STM32F207, NAND flash drive, multiplexers for access to configuration EEPROM, hardware watchdog timer for loading FPGA from the reserve EEPROM, as well as real time clock.

■ FPGA

The FPGA chip installed on the KIC551 / KIC551RC module is designed for performing the following functions:

▪ Controlling the process of supplying power to the units of the PCI Express interface module: units of the PEX8764 PCI Express switch, 10 Gbit Ethernet JL82599EN, optical modules.

▪ Control of secondary power supplies with alarm indication and start lockout.

▪ Ability to transfer the startup control to ARM MCU.

▪ Generation of reset signals both for peripheral devices and for all the module equipment, including the MCU (in order to reprogram the MCU).

▪ Control of generating clock signals for peripheral modules.

▪ Loading the preset configuration of the PEX8764 PCI Express switch using the DIP switches.

▪ Loading configuration of the PEX8764 PCI Express switch from the configuration SPI EEPROM.

▪ Loading configuration of optical modules from the configuration SPI EEPROM.

▪ Configuring the PEX8764 PCI Express switch using strap signals.

▪ Control of local configuration EEPROM for units: of the PEX8764 PCI Express switch, 10 Gbit Ethernet JL82599EN, Gigabit Ethernet switch, configuration SPI EEPROM, as well as main and reserve configuration EEPROM FPGA.

▪ Controlling indication of the status of connections of the PEX8764 PCI Express switch, system events, temperature conditions.

▪ Possibility to modify the contents of local configuration EEPROMs: of the PEX8764 PCI Express switch, 10 Gbit Ethernet JL82599EN, Gigabit Ethernet switch, as well as general configuration SPI EEPROM and EEPROM storage bitstream FPGA.

▪ Providing MCU with an access to the resources of modification of all the EEPROMs.

▪ Providing MCU with an access to the Hardware Monitor data.

■ STM32F207 Microcontroller

The main working functions of the microcontroller are as follows:

▪ Controlling the process of supplying power to the Gigabit Ethernet switch units.

▪ Controlling the Gigabit Ethernet switch.

▪ Controlling the FPGA status.

▪ Arrangement of interaction with FPGA (over UART and SPI interfaces) for implementing the function of control of power supply, configuration, reprogramming all the configuration EEPROMs, as well as control of the LM87 Hardware Monitor parameters.

▪ Arranging storage of the EEPROM Program Configuration Units (PCU) for all the module's units.

▪ Adjustable real time clock.

▪ Ensuring protected access from a local network to data warehouse.

▪ Implementation of script sequences for module and system control set from the local network.

■ NAND flash drive

The NAND flash drive has a capacity of 64 MB and is intended for storing PCU for all the devices on the board of the module, as well as other data. Using the MCU, a remote access (FTP) to the NAND drive can be organized through the Gigabit Ethernet switch from any peripheral slot of the system or through the RJ45 connector on the front panel of the KIC551/KIC551RC module. A detailed description of works with the NAND drive is given in *Section 4 Program configuration of KIC551/KIC551RC*.

■ Multiplexers for access to configuration EEPROMs

The KIC551/KIC551RC module is equipped with multiplexers for the arrangement of a separate access of FPGA or microcontroller to EEPROM configuration microchips. These multiplexers are synthesized and are located in FPGA (see Fig. 2.3).

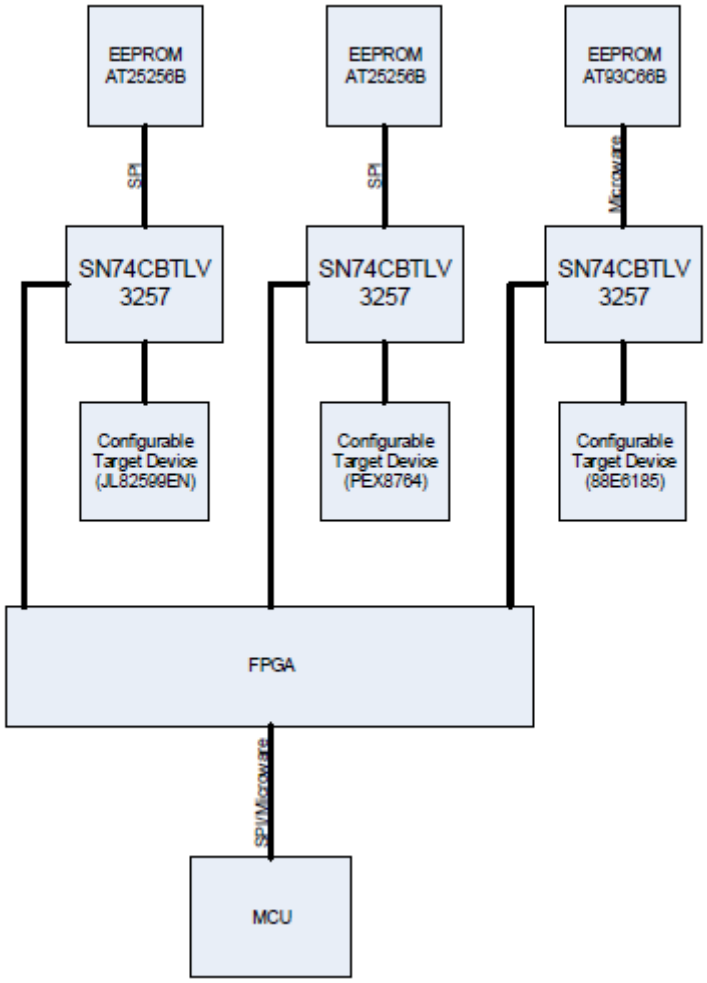


Fig. 2.3 – Diargam for multiplexing configuration EEPROM of KIC551/KIC551RC

The board of the KIC551 / KIC551RC module is also equipped with hardware multiplexers (SN74CBTLV3257), which arrange switching of interfaces (SPI or Microware) of the corresponding configuration EEPROMs between the FPGA and the configured devices themselves. These multiplexers are controlled by hardware and software: if the FPGA is successfully configured, then the multiplexers will be controlled by the FPGA, otherwise, the configuration EEPROMs will be permanently connected to their configurable devices.
Forwarding interfaces from the configuration EEPROMs to microcontroller enables to modify contents of any of the EEPROMs (including the configuration EEPROMs FPGA) both locally from the NAND flash drive and remotely via the Gigabit Ethernet interface (the MCU operates at the rate of up to 100 Mb).

■ Hardware watchdog timer for loading FPGA from the reserve EEPROM

The hardware watchdog timer is designed for switching active configuration EEPROM FPGA from the main to the reserve one in case of damages to PCU FPGA in the main configuration EEPROM FPGA.

HL13 LED is designed to determine the current active configuration EEPROM (Fig. 2.4, Table 2.1, subparagraph 4.2.5 Booting the Program Configuration Unit's FPGA (main/reserved)).

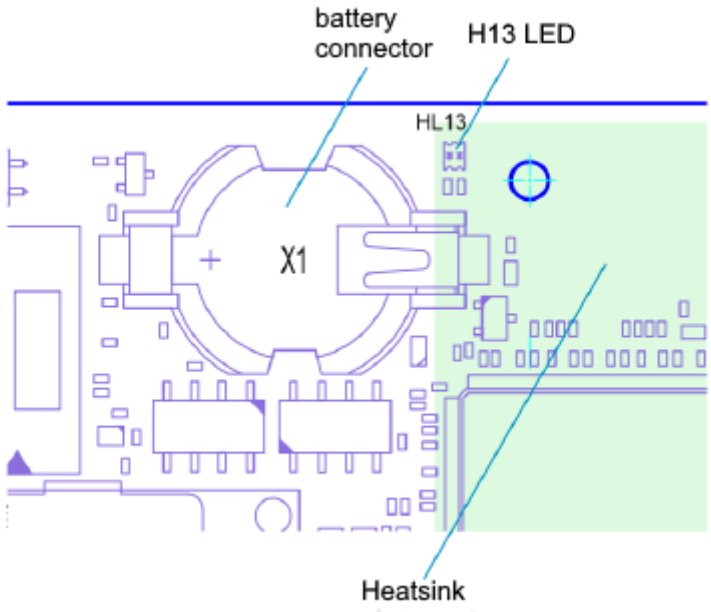


Fig. 2.4 – Location of H13 LED and power supply battery connector on KIC551/KIC551RC

Table 2.1 – Status of the HL13 LED

HL13 LED color	Active configuration EEPROM FPGA
Green	Main
Red	Reserved

The main and reserved configuration EEPROMs can be modified both locally from NAND flash drive, and remotely via the Gigabit Ethernet interface (the MCU operates at the rate of up to 100 Mb).

■ Real Time Clock

In order to record events, as well as to provide the autoconfiguration functions, the KIC551/KIC551RC module features a real-time clock implemented by the MCU hardware.

A 3.0 V lithium battery is used to supply power to the real-time clock in a de-energized state (Fig. 2.4). Please use RENATA CR1632 battery or other compatible models. The module can work without a battery. If no battery is used, setting the real time clock will be required every time the power is turned on, otherwise the clock data might be invalid.

2.3.2 LED unit

The LED unit is used for displaying the following information (Table 2.2):

Table 2.2 – LED unit

LED designation	LED color	Displayed information
PE1 – PE8	Green/Red	Status of PCI Express interfaces of the peripheral slots 2 through 9 (in accordance with the designation on the backplane).
ET1 – ET8	Green/Yellow	Status of Ethernet interfaces of the peripheral slots 2 through 9 (in accordance with the designation on the backplane).
SFP	Green/Yellow	Status of the 10 G Ethernet interface.
SYS	Red/Blue	System LED. Module status, diagnostics of integrated DC-DC converters malfunctions.
FO	Green/Red	Status of the system PCU.
OVH	Green/Red	Temperature mode of the module
UP (GP)	Green/Red	Status of the optical PCI Express interface (KIC551-01 and KIC551RC-01). The GP LEDs functions are reserved.

■ **PE1 – PE8 LEDs**

The PE1 – PE8 LEDs (Fig. 2.5) are designed for designating parameters of the PCI Express connection in each peripheral slot. The data to be displayed is generated by hardware: by the integrated features of PCI Express switch.

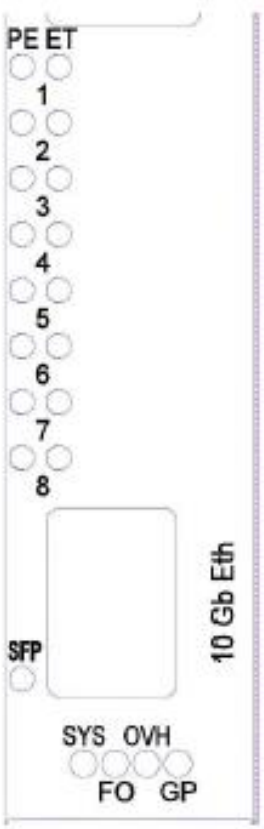


Fig. 2.5 – Front panel LEDs

The information displayed by **PE1** – **PE8 LEDs** is given in Table 2.3.

Table 2.3 – Status of PE1 – PE8 LEDs

LED color	Display mode	Status of the PCI Express connection
Green	Permanently	Connection speed – 8 Gb
Green	Flashes rapidly	Connection speed – 5 Gb
Green	Flashes slowly	Connection speed – 2.5 Gb
Red	Permanently	Connection fault
Not illuminated	-	No connection

In addition to the function of displaying the parameters of PCI Express connection, the **PE1 - PE8 LEDs** can be programmed by the user and display any set information with independent control of each of the specified LEDs. A detailed description of programming the **PE1 - PE8 LEDs** is given in the subparagraph 4.2.8.2 “Controlling the LEDs of the PE front panel“ of this User Manual.

■ ET1 – ET8 LEDs

The **ET1** – **ET8 LEDs** (Fig. 2.5) are designed for designating parameters of the Ethernet connection in each peripheral slot. The data to be displayed is generated by hardware: by the integrated features of the Gigabit Ethernet switch.
The information displayed by **ET1 – ET8 LEDs** is given in Table 2.4.

Table 2.4 – Status of the ET1 – ET8 LEDs

LED color	Display mode	Status of Ethernet connection
Green	Permanently	Connection speed – 1 Gb
Yellow	Permanently	Connection speed – 10/100 Mb
Not illuminated	-	No connection

The user can change operating conditions of the **ET1 - ET8 LEDs** by direct programming the Gigabit Ethernet switch registers (see Appendix B. List of Telnet interface commands) or by modifying the PCU of the configuration EEPROM AT93C66B Gigabit Ethernet switch.

■ SFP LED

The **SFP LEDs** (Fig. 2.5) is designed for displaying connection parameters of SFP+ interface. The information displayed by **SFP LED** is given in Table 2.5.

Table 2.5 – Status of SFP LED

LED color	Display mode	Connection status
Green	Pulse mode	Information exchange at the speed of 10 Gb
Yellow	Pulse mode	Information exchange at the speed of 1 Gb.
Not illuminated	-	No information exchange.

■ SYS LED

The SYS LED (Fig. 2.5) is designed for displaying the module status and diagnosing malfunctions of the integrated DC-DC converters. The information displayed by the **SYS LED** is given in Table. 2.6.

Table 2.6 – Status of SYS LED

LED color	Display mode	Module status
Blue	Permanent	The module is being initialized
Red	Flashing	Emergency state of the power supply. Amount of flashes corresponds to the number of the damaged DC-DC converter.
Not illuminated	-	The power is supplied. Normal state.

■ FO LED

The FO LED (Fig. 2.5) is designed for displaying the state of the system PCU loading at module's start. The information displayed by the FO LED is given in Table 2.7.

Table 2.7 – Status of FO LED

LED color	Display mode	Module status
Green	Permanent	The correct system PCU is loaded.
Not illuminated	-	The system PCU is missing or damaged (settings set by microswitches are used).

■ OVH LED

The **OVH** LED (Fig. 2.5) is designed for displaying the overheating state of the module. The temperature, which value is responsible for showing whether the module is overheated or not, is controlled by an external sensor connected to the Hardware microchip of the monitor.
The information displayed by the **OVH LED** is given in Table 2.8.

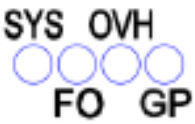
Table 2.8 – Status of OVH LED

LED color	Display mode	Module status
Not illuminated	Permanent	Overheating of the module has been detected.
	-	Module's temperature mode – standard.

■ UP LED (GP for KIC551-02/KIC551RC-02)

The UP LED (Fig. 1.7, Fig. 2.6 (a)) is designed for displaying parameters of the PCI Express connection of optical interface represented with KIC551-01/KIC551RC-01 versions. The data for display is generated by hardware: by the integrated features of the PCI Express switch.
The information displayed by the **UP LED** is given in Table 2.9 (operation mode of the UP LED fully complies with the operation mode of **PE1 – PE8** LEDs**).**

KIC551-01/KIC551RC-01 a



KIC551-02/KIC551RC-02 b

Fig. 2.6 – UP LED (GP LED)

Table 2.9 – Status of UP LED

LED color	Display mode	Status of the PCI Express connection
Green	Permanent	Connection speed – 8 Gb
Green	Flashes rapidly	Connection speed – 5 Gb
Green	Flashes slowly	Connection speed – 2.5 Gb
Red	Permanent	Connection fault
Not illuminated	-	No connection

In KIC551-02/KIC551RC-02 versions, the functions of **GP LED** (Fig. 2.5, Fig. 2.6 (b)) are reserved. In the future, when modifying the PCU of FPGA module, the **GP LED** can be used.

2.3.3 Synchronization unit

The synchronization unit is designed for generating clock pulses with specified characteristics both for the nodes of the KIC551 / KIC551RC module itself and for peripheral modules installed into the system backplane.
In terms of design, the synchronization unit is made of three parts: driving quartz-crystal oscillator, uncrontrolled bffer for integrated nodes and controlled 8-channel buffer for peripheral modules.
The clock generator works with SSC (Spread Spectrum Clock) disabled, which makes it possible to build systems with asynchronous clocking. This, for example, enables to use a KIC551/KIC551RC module in a peripheral backplane slot with a root that uses the PCI Express chip of a PEX86xx or PEX87xx switch. In this case, the clock input from the backplane is not used.
The technical specifications of peripheral clock are listed at the end of this User Manual (Annex B).
In addition, the module can support disabling unused clock channels under certain conditions (this feature is disabled by default).

2.3.4 PCI Express switch unit

The PCI Express switch unit is designed for establishing hardware connection between the switch and peripheral modules of the system, as well as for switching and routing of information packets between the host and peripheral modules with the set speed and propagation delay.

Unit of the PCI Express switch is based on the VLSI PEX8764 PLX Technology (Awago-Broadcom) switches.
Configuration of the switch port (width, speed, transparency, etc.) can be changed manually using the SA1 and SA2 microswitches (see subparagraph 3.9.1 Hardware configuration of the KIC551/KIC551RC module) or using a software by programming the system Program Configuration Unit (see subparagraph 4.2.11 Programming the system PCU).
In addition to the specified parameters, you can configure the initial settings of the VLSI switch program registers (BAR, settings of the integrated equalizers, other parameters), which detailed description is given in the SDK provided by the VLSI switch manufacturer. These settings must be written into the PCU of the PCI Express switch using a special software utility or via the Telnet interface using the microcontroller command system of the control unit (see Annex B List of Telnet interface commands).

2.3.5 Gigabit Ethernet switch unit

The Gigabit Ethernet switch unit is designed for setting up a hardware connection between the switch and peripheral modules, as well as for switching information packets between peripheral modules with the set speed.
The Gigabit Ethernet switch unit contains VLSI of the 88E6185 10-channel Gigabit Ethernet Marvell switch, 2 x 4-channel PHY Marvell 88E1340S tranceivers and galvanic isolation and negotiation node based on four HX5200NL Dual Transformer Modules.
To connect an external Gigabit Ethernet network on the front panel of KIC551 there is a Gigabit Ethernet port, connected to one of the switch channels via a separate PHY Marvell 88E1111 Gigabit Ethernet Transceiver.
Configurations of the switch VLSI and PHY integrated circuits can be changed using the MDIO interface connected to the microcontroller of the control unit (see the microcontroller command system in the subsection Annex B List of Telnet interface commands).
It is also possible to automatically download the switch configuration from the PCU of the Gigabit Ethernet switch recorded in the EEPROM (see subparagraph 4.2.3 Loading the PCU of the Gigabit Ethernet switch).
The characteristics of the Gigabit Ethernet switch unit are given at the end of this User Manual (Annex D).
The galvanic isolation of the Gigabit Ethernet ports routed to the backplane is 100 volts.

2.3.5.1 External Gigabit Ethernet interface

The front panel of KIC551/KIC551RC is equipped with the 10Base-T/ 100Base-TX/ 1000Base-T Ethernet port, connected to one of the switch channels via a separate PHY Marvell 88E1111. The RJ45 Gigabit Ethernet connector on the front panel is labelled as **1 Gb Eth** (Fig. 1.3, Fig. 1.4, Fig. 1.7).
The interface ensures automatic transfer rate detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transfer rates.

2.3.5.2 Purpose of RJ45 connectors' pins

RJ45 connector is shown in Fig. 2.7, purpose of the pins is shown in Table 2.10.

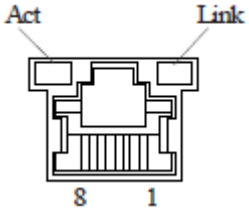


Fig. 2.7 –RJ45 Ethernet Connector

Table 2.10 – Purpose of the RJ45 Gigabit Ethernet connectors' pins

Pin	MDI / Standard Ethernet cable					
	10Base-T		100Base-TX		1000Base-T	
	I/O	Signal	I/O	Signal	I/O	Signal
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX–	O	TX–	I/O	BI_DA–
3	I	RX+	I	RX+	I/O	BI_DB+
4	–	–	–	–	I/O	BI_DC+
5	–	–	–	–	I/O	BI_DC–
6	I	RX–	I	RX–	I/O	BI_DB–
7	–	–	–	–	I/O	BI_DD+
8	–	–	–	–	I/O	BI_DD–

2.3.5.3 Status LEDs of external Ethernet interface channel

Green "Link» LED (line) is on if the line is connected.
The green "Act" (activity) LED is on if computer receives or transfers packets via the RJ45 connector.
Galvanic isolation of the Gigabit Ethernet port routed to the front panel is 500 volts.

2.3.6 10G Ethernet network controller unit

The 10 Gbit Ethernet network controller unit is designed for arranging connection of the system with the KIC551 / KIC551RC module to external devices via the 10 Gbit Ethernet interface.

The network controller unit is equipped with an Intel® JL82599EN VLSI network controller connected via the PCI Express x4 Gen 2 interface to one of the PCI Express PEX8764 switch ports.
The SFI interface with parameters listed in the SFF-8431 specification is used to connect PHY modules of the SFP + form factor. Both optical fiber and copper cable can be used as a transmission line. The type of transmission line used depends on the type of SFP + module installed.

Along with the KIC551 module, operation of the following SFP+ modules was tested:

- 10 Gbit Ethernet optical module Avago AFBR-709ISMZ 850 nm;
- 1 Gbit Ethernet optical module Network Logic NC5512-03-I;
- 1 Gbit Ethernet optical module Network Logic NC3112-03-I.

Configuration of the network controller for working with the SFI interface is set by EEPROM with a PCU 10 Gbit network controller. Same as with the Program Configuration Unit of the PCI Express switch, the PCU of the 10 Gbit Ethernet controller can be modified using a special utility program or via Telnet interface using the microcontroller's command system of the control unit.

2.3.7 PCI Express optical interface unit (KIC551-01/KIC551RC-01)

The PCI Express optical interface unit is designed for the arrangement of the high-speed interconnection via PCI Express x8 Gen3 interface using the optical transmission line.
For operation of the optical transmission line, the AFBR-820 Avago Parallel-Fiber-Optic Receiver and AFBR-810 Avago Parallel-Fiber-Optic Transmitter are used. Using these modules enables to establish a high-speed connection at a distance of up to 50 meters.
To support various configurations of building multiple-unit system, the user can quickly change the type of PCI Express port of the optical interface using microswitches: Transparent or Non-Transparent. Detailed description of microswitch settings is given in subparagraph 3.9.1 Hardware configuration of the KIC551/KIC551RC module.
The advanced settings of the PCI Express port of optical interface are available through the system PCU and are described in Paragraph 4 Program configuration of KIC551/KIC551RC.
At the time of operation, the system considers the optical transmission line as a traditional connection over the PCI Express interface.
The optical connection status is shown by the **UP LED** located on the front panel of KIC551-01/KIC551RC-01 (Fig. 2.6 (a)). Operational behavior of the **UP LED** is described in the Table 2.9 (Subparagraph 2.3.2).

Attention!

For successful software registration of the lower-level unit in the system at the start, the switch-on sequence should be observed: from the lower to the upper levels, specifically, the lower levels of the system "tree" should be enabled first, and the upper host should be switched on last.

Characteristics of the output stage of the AFBR-810 Avago Parallel-Fiber-Optic Transmitter and input stage of the AFBR-820 Avago Parallel-Fiber-Optic Receiver are added to the Annex E.
For optical transmission line, you can use Molex optical cable assemblies of the 106284 series.

2.4 Cooling system of KIC551

The customized cooling heatsink provides the best foundation for stable operation and long-term reliability of the KIC551. When used in conjunction with the system enclosure, which provides adjustable airflow data, the controlled dissipation of heat energy is guaranteed. The size, shape and design of the heatsink provide the best values of thermal resistance (Rth). In addition, the heatsink is designed for active use of the forced air cooling of modern CompactPCI Serial systems.

When designing solutions based on the KIC551, the designer must consider the overall thermal performance of the system. Use a system enclosure that meets your heat removal requirements. When performing thermal calculations, the contribution of peripheral devices to the total heat dissipation of the system should be considered. The peripheral devices, in turn, must have thermal characteristics corresponding to the operating temperature range of the module and the system in general.
Requirements for the cooling system of the KIC551 modules are given in subparagraph 3.6.1.

2.4.1.1 Data-transfer-rate-Temperature releationship (KIC551)

To confirm the stated characteristics, climatic tests of the KIC551 modules were carried out. Before the start of the tests, fans were installed into the chassis, which were turned on throughout the entire experiment. The tests at positive temperatures were carried out with a step change in temperature with an increment of 10 °C, starting from +20 °C (Table 2.11). As a test, we used a suite of test programs that load the network controller, Gigabit Ethernet and PCI Express switches.

Table 2.11 – Transfer-Rate-and- Current-Consumption-Temperature-Relationship (KIC551)

Ambient temperature, T chmb, °C	Backplane, PCIe, Mb/sec, Receive / Transmit	Backplane, Eth, Mb/sec	10G Eth, Mb/sec	Average consumption current, A
20	48537/42801	931	10264	4.1
30	48518/42855	931	10264	4.2
40	48507/42774	931	10259	4.3
50	48557/42858	931	10264	4.4
60	48448/42666	931	10264	4.7
70	48549/42804	931	10264	4.9
87	41793/43876	351	818	5.3

At a temperature of +87 °C in the climatic chamber, the Throttle mode was activated as a result of overheating on the CPC512 CPU module used in the test bench. This caused a drop in the rate of data exchange over the interfaces. When using the DMA mode of PCI Express switches, the load on the processor is reduced and the data exchange rates over the PCI Express interface will change insignificantly or will not change at all.

2.5 Cooling system of KIC551RC

To remove heat from KIC551RC a conduction heat-removal cassette is used. Cooling of the “hottest” components of the KIC551RC module’s component unit (10 Gbit Ethernet network controller and PCI Express switch) is performed by special-purpose heat pipes installed inside the heat-removal cassette.

Requirements for the cooling system for KIC551RC modules are specified in subparagraph 3.6.2.

3 Intended Use

3.1 Power consumption of KIC551/KIC551RC

The supply voltage of the KIC551 / KIC551RC is +5 V_ standby, +12 V.
The specified requirements must be taken into account that are essential to ensure stability and reliability. Table. 3.1 shows the values of the maximum permissible voltages on the power lines, exceeding which may damage the module. The power supply sources which will be used with the KIC551 / KIC551RC module, must be verified for compliance with these requirements.

Table 3.1 – Paramters of KIC551/KIC551RC power consumtpion

Voltage (V)	Minimum (V)	Maximum (V)
+5 V_standby	4.75	5.25
+12	10.8	13.2

If the power supply voltage exceeds the specified limits, the functionality of the module is not guaranteed.
The backplane must ensure optimal distribution of supply voltages. It is recommended to use only those backplanes that have two power planes for each voltage.
Connections of the power line and backplane should guarantee minimum losses and ensure consistent performance. Long power supply lines, light-gauge wires and high resistance connections should be avoided.
If possible, power supplies with a voltage monitoring function should be used. The use of an appropriate backplane may also be required.
The power supply must be sufficient for accounting possible deviations in the characteristics of the electronic components.

3.1.1 Starting current and average current consumption of the module

During the tests, the starting current and the average current consumption were measured. The results are shown in Table. 3.2.

Table 3.2 – Measurements results of starting current and average current consumption*

Module	Starting (short-time) current (+12 V)	Average current (+12 V)
KIC551-01, KIC551RC-01 **	6 A	2 A

** Values derived from the laboratory test report for consumption currents.*
*** The module versions KIC551-02, KIC551RC-02 (Tabe 1.1, Table 1.2) do not support optical PCIe interface (values of starting and average consumption currents are less than those specified in the Table 3.2).*

3.2 Compliance with safety requirements of KIC551/KIC551RC

KIC551/KIC551RC corresponds to the general safety requirements for IT equipment in accordance with the GOST R IEC 60950-2002 (for equipment powered from the mains with voltages up to 600V).

3.3 Electromagnetic compatibility of KIC551/KIC551RC

KIC551/KIC551RC corresponds to the requirements for resistance of IT equipment against electromagnetic interference in accordance with the GOST CISPR 24-2013.

KIC551/KIC551RC corresponds to the requirements for the level of industrial radio interference from IT equipment in accordance with the GOST standard 30805.22-2013.

3.4 Operating conditions of KIC551

The device remains functional in case of climatic and mechanical effects specified in Table 3.3.

Table 3.3 – Paramters of climatic and mechanical effects (KIC551)

Type of the effect	**Parameter name**	**Parameter value**	**Document**
Temperature change	Low temperature	- 40 (0*) °C	GOST 28209-89 Nb test
	High temperature	+ 85 (+70*) °C	
Humidity	Relative humidity	Up to 80%, non-condensing	GOST 28209-89
Damp heat (+55) (for versions with conformal coating) **	Relative humidity	Up to 93%	GOST 28216-89 Db test
Sinusoidal vibration	Frequency range	10...500 Hz	GOST 28203-89
	Acceleration	5 g	
Single shocks	Peak acceleration	50 g	GOST 28213-89
	Duration	11 ms	
Multiple shocks	Peak acceleration	25 g	GOST 28215-89
	Duration	6 ms	
	Number of shocks	1000	

** For module version with a commercial temperature range.*

*** Only for the \Coated versions. Only the product strength is guaranteed.*

3.5 KIC551RC operating conditions

The device remains functional in case of the following climatic and mechanical effects:

Table 3.4 – Paramters of climatic and mechanical effects (KIC551RC)

Type of the effect	Parameter name	Parameter value	Document
Elevated operating temperature	–	+85 °C	IMES.469555.002 TU
Elevated limit temperature	–	+90 °C	IMES.469555.002 TU
Reduced operating temperature	–	- 50 °C	GOST RV 20.57.306-98
Reduced limit temperature	–	- 65 °C	GOST RV 20.57.306-98
Temperature change	–	From reduced limit temperature to the elevated limit temperature	GOST RV 20.57.306-98
High hunidity	–	98% at 35 °C	
Atmospheric precipitation	–	15 mm/min	
Static dust	–	5 g/m3 at the air speed of 1 m/sec	
Dynamic dust	–	5 g/m3 at the air speed of 15 m/sec	
Sinusoidal vibration	Range of frequencies	10-500 Hz	GOST RV 20.57.305-98
	Accleration	6 g	
Single shocks	Peak acceleration	75 g, length 1-5 ms	GOST RV 20.57.305-98
Multiple shocks	Peak acceleration	15 g, length 5-15 ms	GOST RV 20.57.305-98
	Number of shocks	10000	

3.6 Cooling system requirements

Attention!!!

Since Fastwel Group is not responsible for any damages to KIC551/KIC551RC and other equipment, caused by overheating, the system developers and end users are recommended to ensure that the module's environment complies with the specified temperature requirements (see subparagraphs 3.6.1 and 3.6.2).

3.6.1 Requirements to the cooling system of the KIC551 module

The module should operate within the specified temperature ranges (subparagraph **1.2 Technical Feaures of KIC551/KIC551RC, Table 3.3**) with the forced air cooling as part of the chassis. The total power dissipated by PCI Express and Gigabit Ethernet switches as well as by 10 Gbit Ethernet network controller is ~50 W. Preliminary thermal calculation of the cooling system is recommended. The values of dissipated power and microchip limit temperatures are shown in Table 3.5.

Table 3.5 – Dissipated power and limit temperatures of microchips

Microchip	Dissipated power (W)	Limit temperature of the microchip(°C)
PCI-E Switch	30	125
10 Gigabit Ethernet Controller	10	110
Gigabit Ethernet Switch	4,5	110

Attention!

For all the KIC551 modules, forced cooling is mandatory, therefore, it is strongly recommended for the users to use the chassis with integrated units for air cooling of internal space for systems based on KIC551.

Attention!

It is recommended to use standard fans (crates manufactured by Schroff) in the systems based on KIC551 interface modules.

3.6.2 Requirements to the cooling system of the KIC551RC module

KIC551RC should function within the specified temperature ranges (subparagraph **1.2 Technical Feaures of KIC551/KIC551RC, Table 3.4)**.
Conduction-type coller for the KIC551RC module, in addition to the thermal extraction sources stated in subparagraph 3.6.1, is capable of efficiently withdraw heat from all active components of the units of elements of the module with heat extraction of more than 300 mW. This enables you to keep the temperature within the inner volume of the plate at an acceptable level. For proper operation of the heat removal plate, the design of the enclosure must provide such a heat dissipation so that the temperature at the control point of the heat removal plate does not go beyond the limits indicated in Table. 3.6.

Table 3.6 – Temperature range (in the reference point of the heat removal plate of KIC551RC)

KIC551RC interface module	KIC551RC-01	Temperature range: from -50 ÷ +85 °C
	KIC551RC-02	Temperature range: from -50 ÷ +85 °C

Location of the reference point on the heat removal plate is defined in accordance with the Fig.3.1.

Fig. 3.1 – Location of the reference point on the heat removal plate of KIC551RC

3.7 Installation and removal

3.7.1 Safety rules during installation and removal of the module

The KIC551 / KIC551RC module is easy to install. At the same time, the below rules, warnings and procedures must be strictly followed in order to properly install the module, avoid any damages to it, its system components, and prevent personal injuries. Fastwel Group is not responsible for any damages resulting from non-complience with these requirements.

Attention!

Switch off the power of the CompactPCI system before installing the module in an empty slot. Also make sure the system is powered off prior to starting to remove the module. Failure to comply with this requirement may pose danger to your health and life, as well as damage the system or module.

 **Electrostatic Sensitive Device (ESD)!**

The CompactPCI module contains electrostatic sensitive components. The following precautions should be complied with in order to avoid damaging the module:

▪ Prior to touching the module, discharge any static charge from your clothing, and also discharge any charge from the tools prior to their use.

▪ Do not touch electronic components or connector pins.

▪ If possible, always work with the board in workplaces protected against static electricity

3.7.2 Procedure of KIC551 installation

In order to install KIC551 into the system, follow the below procedure:

1. Make sure you have followed the safety requirements listed in the previous subparagraph.

 **Attention!**

Failure to follow the instructions below may damage the module and result in system malfunctions.

2. Prior to installation make sure that all the necessary module settings are made in accordance with the subparagraph 3.9.

 **Attention!**

The subsequent operations should be performed with care to avoid damaging both KIC551and other system devices.

3. To install KIC551 the following actions should be performed:

▪ Prior to installation make sure that the system power is off.

 **Attention!**

While performing this operating, **do not apply force** when you insert the module's connector into the backplane’s connector. Use the front panel’s handle to install the module into the connector.

▪ Carefully insert the module into the desired connector, sliding it along the guiderails until it touches the backplane connector.

▪ Using the front panel handle, slide the module into the backplane connector. The module is considered to be completely inserted when the handle closes with a snap.

▪ Fix the module to the front panel of KIC551 using two retention screws (see Fig. 1.3, Fig. 1.4).

▪ Connect all necessary external interface cables to the module.

▪ Make sure that both KIC551 and all the connected cables are securely fixed.

KIC551 is ready for operation.

3.7.3 Procedure of KIC551 removal

In order to remove the module, the following operations should be performed:
1. Make sure that the safety requirements listed in the subsection 3.7.1., have been met.

Attention!
The subsequent operations should be performed with care to avoid damaging both KIC551 and other devices of the system.

2. Prior to start the removal of KIC551, make sure that system power supply is off.

3. Disconnect all interface cables from the module.

4. Unscrew the retention screws on the front panel.

Careful!
Be careful when handling the module as the heatsink can become very hot. Do not touch the heatsink during module's removal.
In addition, the module should not be placed on any surface or in any container until both the module and the heatsink have cooled down to the room temperature.

5. Unblock the front panel handle by pressing the ejector's button (located in the ejector's handle, see Fig. 1.5) and, by pulling it down, remove the module from the backplane connector. After the module is removed from the backplane's connector, pull it out of the enclosure along the guiderails.

Removal of KIC551 is complete.

3.7.4 Procedure for installation of KIC551RC

Attention!
Failure to follow the instructions below may damage the module and result in system malfunctions.
In order to install the KIC551RC module into the system, follow the procedure below:
1. Make sure that the safety requirements listed in subparagraph 3.7.1 are met.
2. Prior to installation, make sure that all necessary module settings have been performed in accordance with subparagraph 3.9.

Attention!

The following operations should be performed with caution, in order not to damage either KIC551RC, or other devices of the system.

3. For installing KIC551RC the following actions should be performed:

▪ Prior to installation, make sure that the system power supply is off.

▪ Make sure that levers A and B are in the “Open” position.

▪ Make sure that the screws of the wedge splitters are unscrewed and wedge components are formed in one line. If necessary, orient the components of wedges manually.

▪ Carefully insert the module into the desired slot.

▪ Move the modules along the guiderails until it touches the backplane connector.

▪ Applying moderate force, press the module into the backplane connector. In this case, the front panel of the module will fit directly against the elements of the chassis enclosure.

▪ Move the A and B levers to the “Closed” position.

▪ Fix the module using two locking screws on the front panel of KIC551RC (see Fig. 1.7).

▪ Secure the wedge splitter screws forcefully for better thermal contact of the plate with the enclosure’s heat spreaders.

Attention!

When installing the KIC551RC module into the enclosure, do not forget to put the wedge splitters to the operating condition. Otherwise, when powered on, the module may quickly overheat and its performance could be impaired.

▪ Connect all the required external interface cables to the module.

▪ Make sure that both KIC551RC and all the connected cables are securely fixed.

KIC551RC is ready for operation.

3.7.5 KIC551RC removal procedure

Attention!

The subsequent operations should be performed with care so as not to damage either the KIC551RC or other devices in the system.

In order to remove a module, the following steps should be performed:

▪ Make sure the safety rules listed in subparagraph 3.7.1. have been met.

▪ Prior to starting the removal of the KIC551RC module, make sure the system’s power is off.

▪ Disconnect all the interface cables from the module.

▪ Uncrew the locating screws on the front panel.

Careful!

Be careful when handling the module as the heat removal plate can become very hot. Do not touch the plate when removing the module.
In addition, the module should not be placed on any surface or in any container until the plate has cooled down to the room temperature.

Unblock the wedge splitters by turning the screws until the hard stop in the direction of module removal (see Fig. 1.7).

▪ While moving levers A and B in the “Open” direction, remove the module from the backplane’s connector.

▪ While continuing to pull the A and B levers, remove the module from the enclosure along the guiderails.

Removal of KIC551RC is complete.

3.8 Battery replacement

For replacing the lithium battery, use the same battery or the one recommended by the manufacturer for such a replacement (Fig. 2.4). Suitable models include RENATA CR1632 or other compatible models.

Important note:

Observe the polarity during battery replacement.
The battery should be replaced with a similar one or the one recommended by the manufacturer.
The used battery should be disposed in accordance with local regulations.
The expected operating time of a 125 mAh battery is approximately 3-4 years while working 8 hours a day at 30°C. At the same time, the battery life highly depends on the operating temperature, as well as on how long the system is in the off state.
It is recommend to replace the battery after every 3 years of operation, without waiting for the end of its service life.

3.9 Configuration of KIC551/KIC551RC

Configuration of the KIC551/KIC551RC module includes hardware and software parts.

3.9.1 Hardware configuration of the KIC551/KIC551RC module

The hardware part includes 8 microswitches (located in the bottom part of the module), divided into two groups, where each group contains 4 microswitches: SA1 and SA2 (see Fig. 3.2).

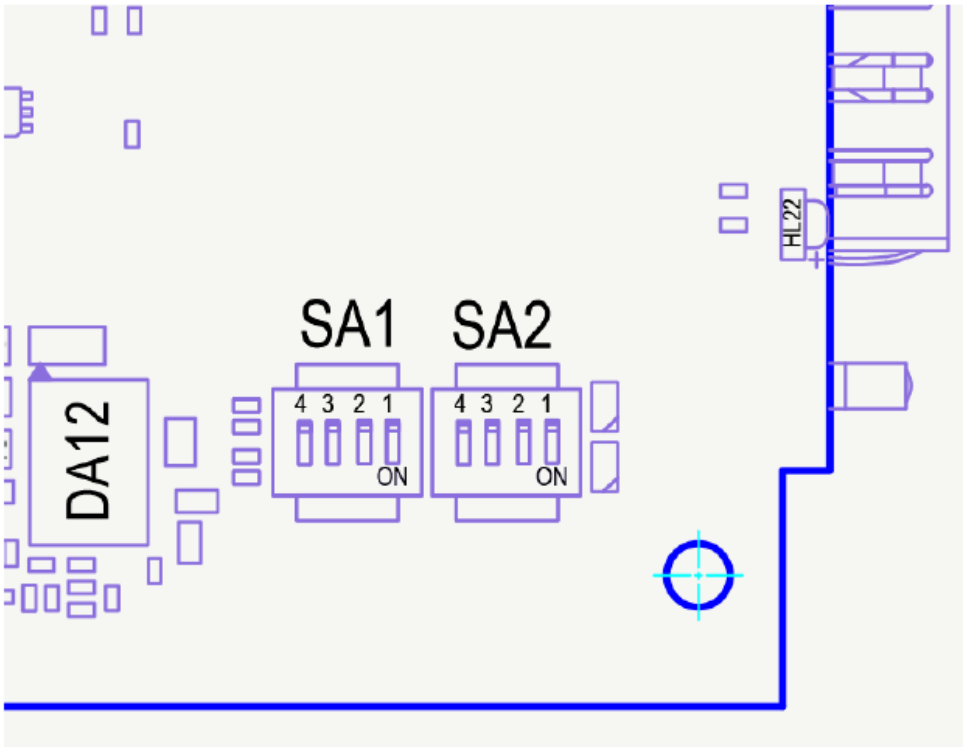


Fig. 3.2 – SA1 and SA2 microswitches

The following settings are available through the hardware component:

- Assigning the slot number in the backplane where the host is installed.
- Setting the operating port of the PCI Express optical interface: Transparent or Non-Transparent.
- Blocking the loading of FPGA configuration from the reserved EEPROM.
- Blocking the use of the software component of the module configuration.
- Switching the software configuration of the KIC551module depending on the version: with conduction cooling of KIC551RC or finned heatsink of KIC551.

● Setting the box of SA1 microswitches

Functions of the SA1 box are individual for each microswitch, included in the box. Description of the box of SA1 microswitches is given in the Table 3.7.

Table 3.7 – Box of SA1 microswitches

Switch number	Function	Value	
		ON	OFF
SA1.1	Loading PGA from the main or backup FLASH	Main	Automatic
SA1.2	Cooling type of KIC551	Conduction	Convection
SA1.3 *	The NT mode for optical PCIe port	NT	Transparent
SA1.4	Loading configuration of PCIe switch	Switching	Automatic

** SA1.3 is inactive when the optical PCIe port is set to the Upstream mode (SA2 is in OFF position (Table 3.8))*

● **Setting the box of SA2 microswitches**

Combination of the SA2 microswitches specifies the VLSI of the PCI Express switch the backplane slot number where the system's host processor is placaed.
The SA2 microswitch box enables you to designate any of the 8 x peripheral slots of a standard Compact PCI Serial backplane as the Upstream port (the host processor of the system is connected to the Upstream port). In the standard (basic) configuration, only one Upstream port is allowed in the system.

Attention!

The CPC51x processor modules of the Compact PCI Serial standard manufactured by Fastwel Group, can be used as the host processor of the system. These modules have special-purpose clock systems and additional initialization lines for operation in the peripheral slot of the backplane.

Attention!

The processor modules used as the slave devices, should have the ability to switch the FAT1 port to the Non-Transparent mode, as well as switch to the mode with external synchronization and operate in the asynchronous mode. It is recommended to use CPC51x Compact PCI Serial standard processor modules as the slave devices, but only those manufactured by Fastwel Group.

Descirption of the SA2 microswitch box is given in the Table 3.8.

Table 3.8 – Box of SA2 microswitches

Purpose of Upstream port	**SA2.1**	**SA2.2**	**SA2.3**	**SA2.4**
	CFG0	**CFG1**	**CFG2**	**CFG3**
Optical PCIe port	0	0	0	0
Slot #2. FAT Pipe1	1	0	0	0
Slot #3. FAT Pipe2	0	1	0	0
Slot #4	1	1	0	0
Slot #5	0	0	1	0
Slot #№6	1	0	1	0
Slot #№7	0	1	1	0
Slot #8	1	1	1	0
Slot #9	1	1	1	1

1 – Switch in ON position
0 – Switch in OFF position

3.9.2 Program configuration of the KIC551/KIC551RC module

Program componenet makes it possible to perform a more flexible configuration of KIC551/KIC551RC nodes' parameters. The program component settings are stored in the system Program Configuration Unit, written to the speciflized EEPROM.
In addition to the settings specified for the hardware component, the software component settings allow you to individually configure each PCI Express station of the switch (to use the KIC551/KIC551RC module in customized backplanes with parameters different from those described in the Compact PCI Serial specification), set the operation speed for the PCI Express switch, operation modes of the station ports: Transparent or Non-Transparent, activate virtual modes of the switch, and also include a programmable delay in the module initialization.
The program configuration of KIC551/KIC551RC is described in section 4.

4 Program configuration of KIC551/KIC551RC

The software used with the KIC551 / KIC551RC module includes operating and configuration software. The operating software includes the bootloader and control program in the microcontroller, as well as the control program for the FPGA.

4.1 Modification of operating software

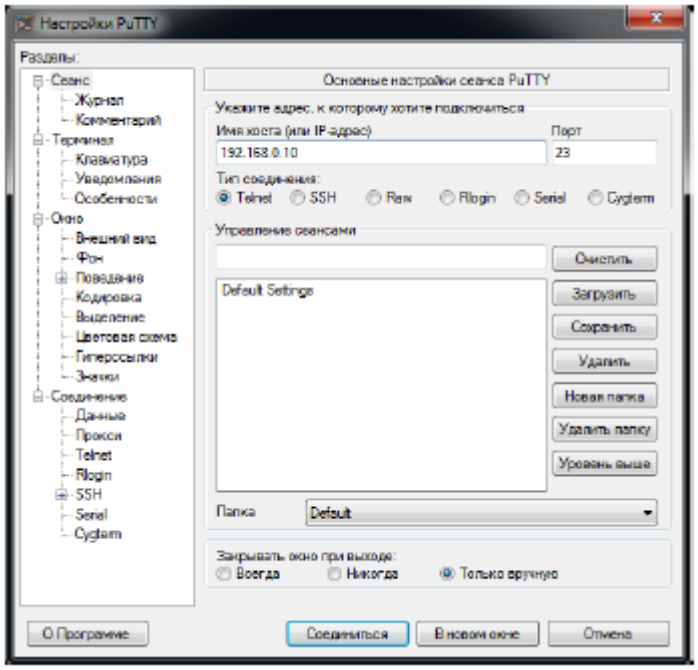
The module is supplied with the preinstalled operating software. Nevertheless, the user can modify and upgrade the operating software by itself, if necessary.

Attention!
All software modifications should be performed strictly in accordance with this User Manual.

The user can modify the following components of the operating software: the control program of the microcontroller and FPGA control program.

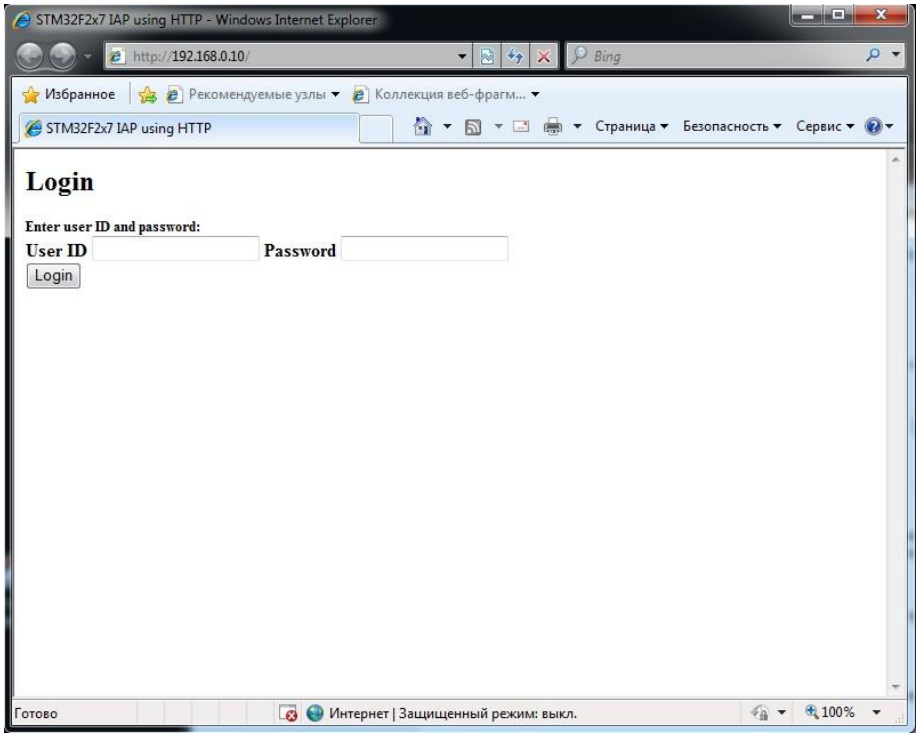
To program the micrcocontroller control program you should connect the Gigabit Ethernet interface of an external PC via RJ45 cable with the **1 Gb Eth connector**, located on the front panel of KIC551/KIC551RC (Fig. 2.7).

After feeding the power to KIC551/KIC551RC you should start the Telnet-client program on the external PC, e.g. “PuTTY” utility or similar.
Paramters of setting the Telnet-client connection using the example of the “PuTTY” utility are specified on the below screenshot:

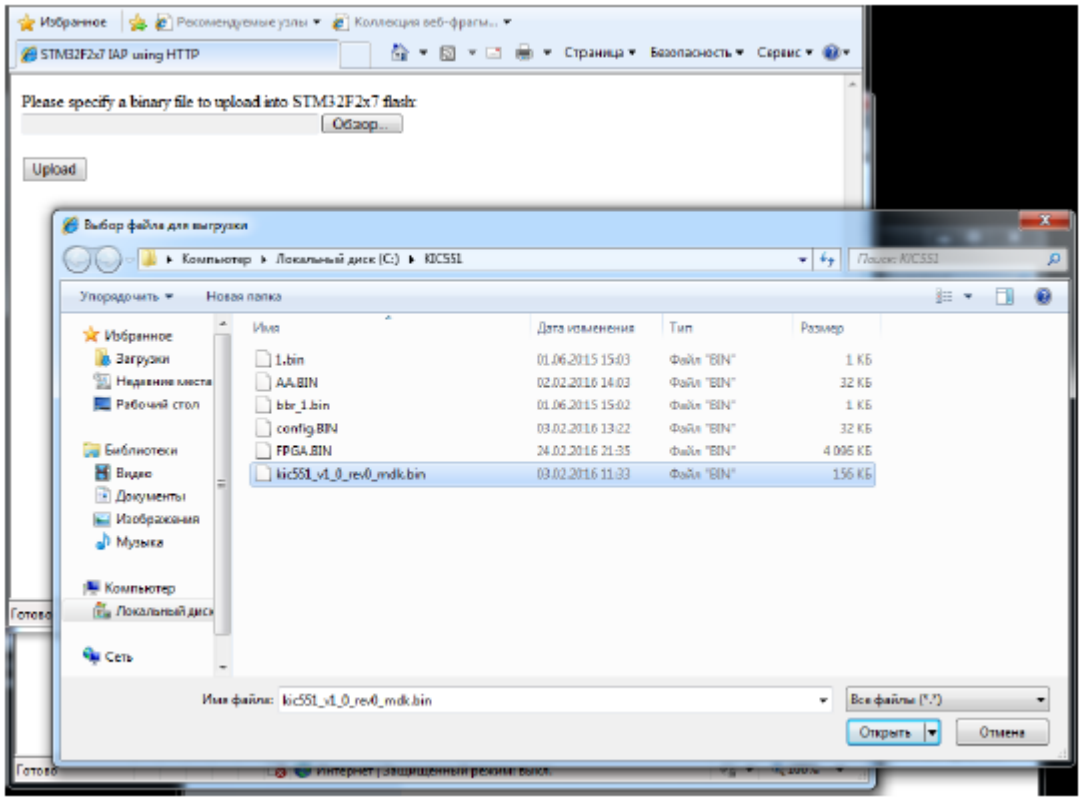


After the connection is established, a Telnet session prompt will appear:

To switch the bootloader to the mode of updating the control program, input the command (see Annex B)
Cmd>jbl
The Telnet-session window will be closed automatically. Further you should start any Internet browser program.
In the opened window of the program, in the address bar specify the KIC551 module's address: 192.168.0.10:



Enter the username in the User ID line. By default: admin
The Password line should contain password. By default: Fastwel.
In the opened window, the location of the operating software file whould be specified:



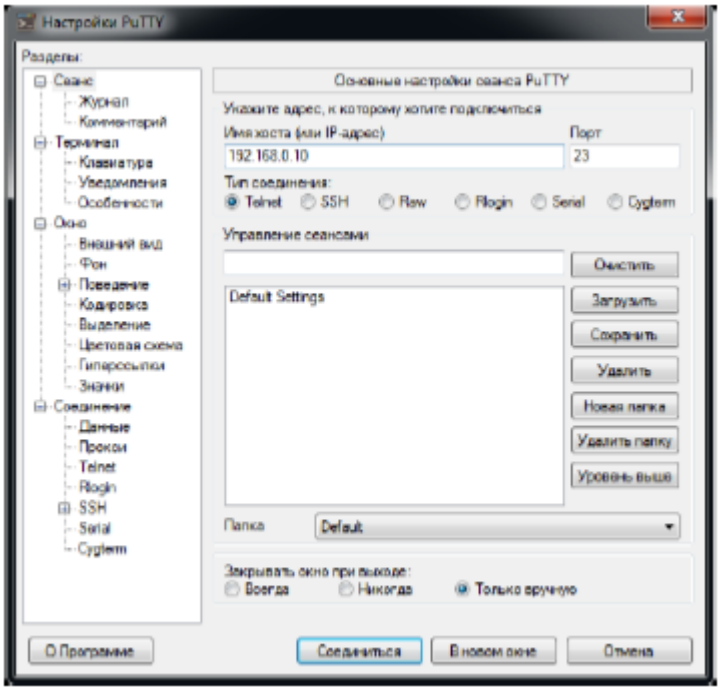
Attention!

The operating software files for programming through HTTP bootloader have the extension .bin

To load the file to the microcontroller's memory you should press the "Upload" button.
After the programming, the KIC551/KIC551RC module should be turned off.

4.1.1 Formatting the integrated NAND drive

The NAND drive mounted on the KIC551/KIC551RC module is designed for storing alternative system configurations, as well as for backup storing configuration software for all peripheral devices of the module. If necessary, the purpose of the information stored can be different.
Prior to the use, the NAND drive must be formatted in the mode assuming that all the packs are erased (initial format). Further, the formatting, if necessary, can be carried out on a regular basis.
To carry out the formatting procedure, a Telnet-client application based on the "PuTTY" or similar utility is used.
The Telnet client connection settings using the example of the PuTTY utility are shown in the screenshot below:



After the connection is established, the Telnet-session prompt will appear:

To start the formatting, you should input the command (see Annex B):
Cmd>format /LLEB

Attention!

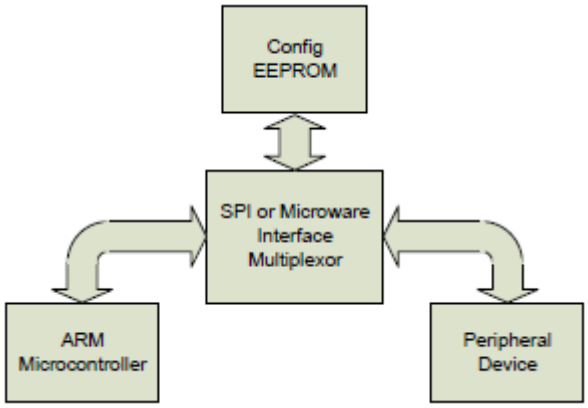
The formatting mode with erasing all the packs will take some time. You should wait for the message that the procedure has been completed successfully.
After formatting the NAND drive, the KIC551 module will be ready for loading the pack of configuration parameters.

4.2 Upgrading configuration software via Gigabit Ethernet interface of the KIC551/KIC551RC module

4.2.1 Loading the pack of configuration parameters

Operating configuration parameters for each peripheral device in the KIC551/KIC551RC module are stored in individual EEPROMs with a compatible interface. During startup or global reset, the peripheral device reads the contents of “its” EEPROM and makes the necessary settings for its parameters.

For the possibility of updating the working configurations of peripheral devices in the KIC551/KIC551RC module, a multiplex EEPROM connection is implemented, where it is possible by software, to redirect the interface of any EEPROM on the microcontroller line:



The multiplexer is controlled using the register with address 01.
Purpose of bits with the register with the address 01 “EEPROM Control» is given in the Table 4.1.

Table 4.1 – Purpose of register bits with the address 01 “EEPROM Control”

Register	Bits	Purpose	Type	By default
EEPROM CONTROL	Bit7	Bits from 7 to 4 are reserved. Value at reading - 0Eh.	RO	1
	Bit6		RO	1
	Bit5		RO	1
	Bit4		RO	0
	Bit3	Choosing EEPROM bit 3, see Table 4.2.	R/W	0
	Bit2	Choosing EEPROM bit 2, see Table 4.2.	R/W	0
	Bit1	Choosing EEPROM bit 1, see Table 4.2.	R/W	0
	Bit0	Choosing EEPROM bit 0, see Table 4.2.	R/W	0

The KIC551/KIC551RC module has a total of 6 individually addressable EEPROM chips (Table 4.2).
Compliance of bit sequences of the register with the address 01 “EEPROM Control” with the selected EEPROM microchip is shown in the Table 4.2.

Table 4.2 – Compliance of bit sequences of the register with the address 01 “EEPROM Control” with the selected EEPROM microchip

EEPROM chip	Bit 3	Bit 2	Bit 1	Bit 0	Value
Not selected (by default)	0	0	0	0	0
EEPROM of the PCI Express AT25256B switch	0	0	0	1	1
EEPROM of the Gigabit Ethernet AT93C66B switch	0	0	1	0	2
EEPROM of the 10G Ethernet AT25256B controller	0	0	1	1	3
EEPROM of AT25256B system configuration	0	1	0	0	4
Main configuration EEPROM FPGA AT45DB321D	0	1	0	1	5
Reserved configuration EEPROM FPGA AT45DB321D	0	1	1	0	6

The pack of configuration parameters contains information for configuring the peripheral devices located inside the KIC551/KIC551RC module and also defines the system configuration.
Therefore, the pack of configuration parameters includes:

1. Program Configuration Unit (PCU) of the PCI Express switch;
2. PCU of the 1 Gbit Ethernet switch;
3. PCU of the 10 Gbit Ethernet controller;
4. PCU of the FPGA, main;
5. PCU of the FPGA, reserved;
6. PCU, system.

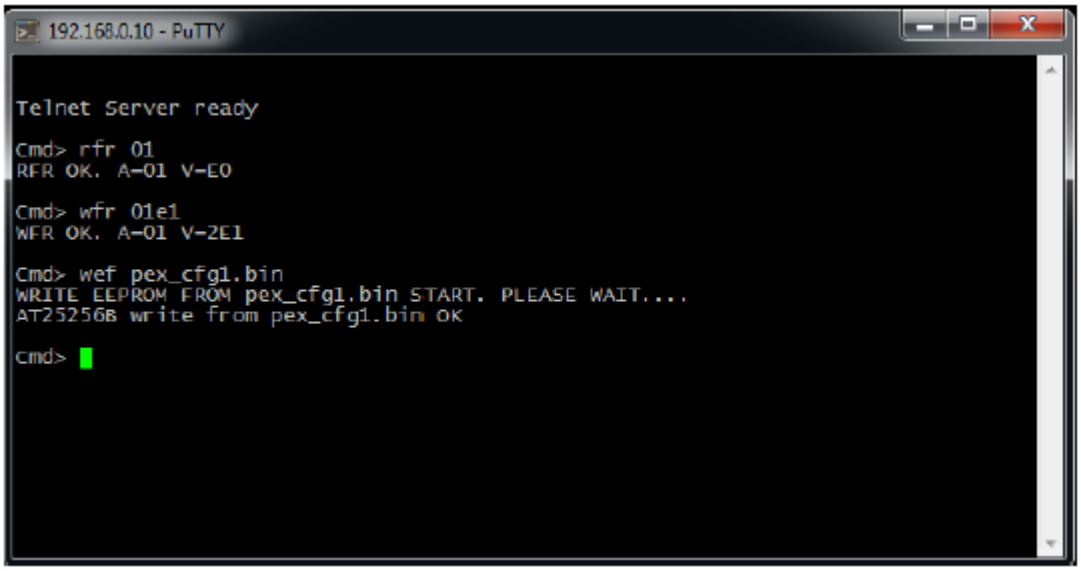
Each of the listed PCUs, is in operating condition and stored in the corresponding EEPROM chip, from where it is loaded when the KIC551 / KIC551RC module is powered on.
If PCU needs to be changed, the updated PCU is placed into the NAND drive of the KIC551/KIC551RC module using the Gigabit Ethernet interface via FTP, and then via Telnet connection by a command (see Annex B - List of Telnet interface commands) it is copied to the corresponding EEPROM chip.
The NAND drive can have several PCU copies, implementing any given configuration of this peripheral device or system. A PCU copy can either be selected by a command via Gigabit Ethernet interface or autonomously by an algorithm, loaded in the working software of the microcontroller. This will enable to flexibly reconfigure the system for solving a broad range of tasks, as well as improve the system fault tolerance at the level of packs or group of packs.

4.2.2 Loading PCU of the PCI Express switch

The PCU of the PCI Express switch is designed for configuration of the internal function registers of the PEX8764 VLSI, including BAR, Link Control, Power Management, etc. the more detailed information can be found in the documentation for the relevant VLSI (PEX_8764-AA_AB_Data_Book_v1.0_05Jun13.pdf [1], see the Annex G).
The AT25256B chip is sued as the configuration EEPROM VLSI PEX8764.
The PCU itself can be synthesized for configuring the PEX8764 VLSI using the PLX Device Editor software, provided by the manufacturer of the specified VLSI - Awago Technologies (formerly PLX Technology). The latest version can be downloaded from the website:

http://www.avagotech.com/products/pcie-switches-bridges/software-dev-kit.
In order to enjoy all the features of this software, you will need a license key, which is available from your regional representatives of Awago Technologies.

As an example, let's consider the loading a PCU located in the "pex_cfg1.bin" file in the root directory on a NAND drive using a Telnet connection.
To load a copy of the PCU from the NAND drive, you need to run the following sequence of instructions:



1. Test reading of the EEPROM register contents of multiplexer. 4 most significant bits of this register always restore 0xE.

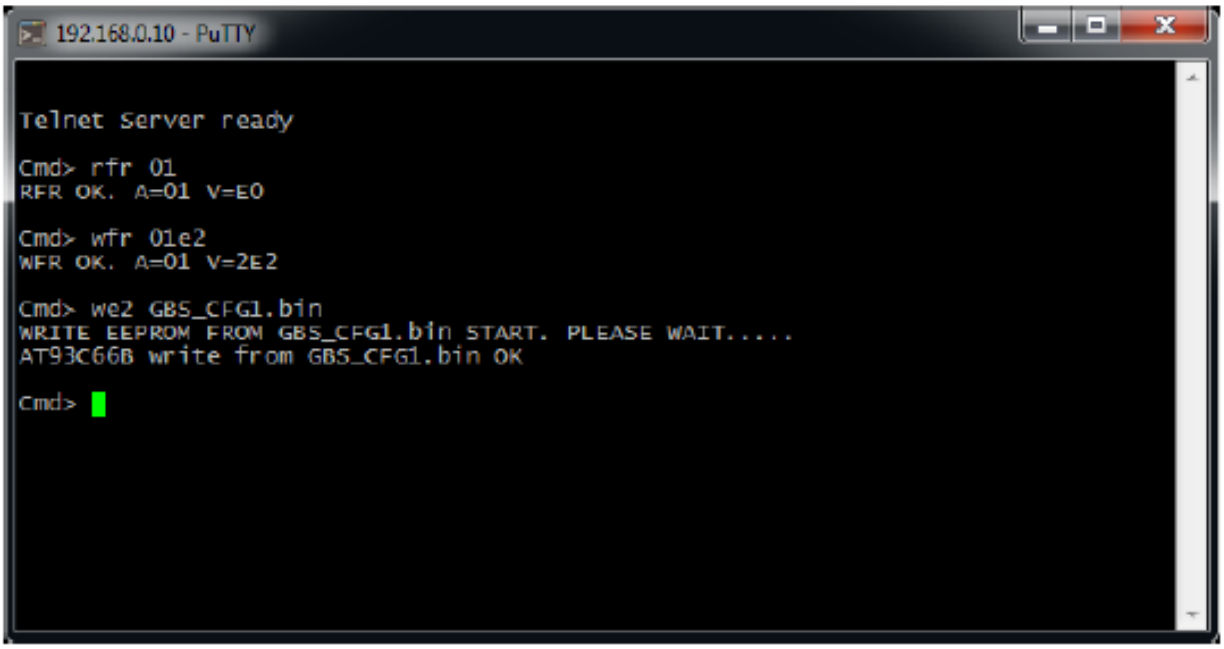
2. Switching the microcontroller to the configuration EEPROM VLSI PEX8764.

3. Loading the PCU "pex_cfg1.bin" to the configuration EEPROM VLSI PEX8764.
In order for the changes to take effect (for the newly written configuration to become active), you should perform the global reset.

4.2.3 Loading the PCU of the Gigabit Ethernet switch

The PCU of the Gigabit Ethernet switch contains the parameter settings for the Marvell 88E6185 Gigabit Ethernet switch and 88E1340 PHY chips.
Where the microcontroller functions properly, the settings of these microchips are performed by the microcontroller itself when power is supplied to the KIC551/KIC551RC module. If the microcontroller turns out to be inoperable and faulty for any reason, the PCU parameters contained in the configuration EEPROM are automatically used.
AT93C66B chip is used as the configuration EEPROM of the 88E6185 switch.
For PCU synthesis, you can use the software "SwitchGUI Customer" provided by Marvell and a specialized USB2SMI adapter developed by the same company. It is also possible to prepare the PCU using the Hex Editor utility or similar, following the instructions given in the documentation for (88E6185_Datasheet.pdf [2]) and 88E1340 (MV-S104603-00_88E1340_88E1322_Datasheet.pdf [3], see Annex G).

Below you can find an example of booting the Program Configuration Unit, placed in the file “gbs_cfg1.bin” in the root directory to the NAND drive using Telnet connection.
For booting a copy of the Program Configuration Unit from NAND drive you should perform the following sequence of instructions:



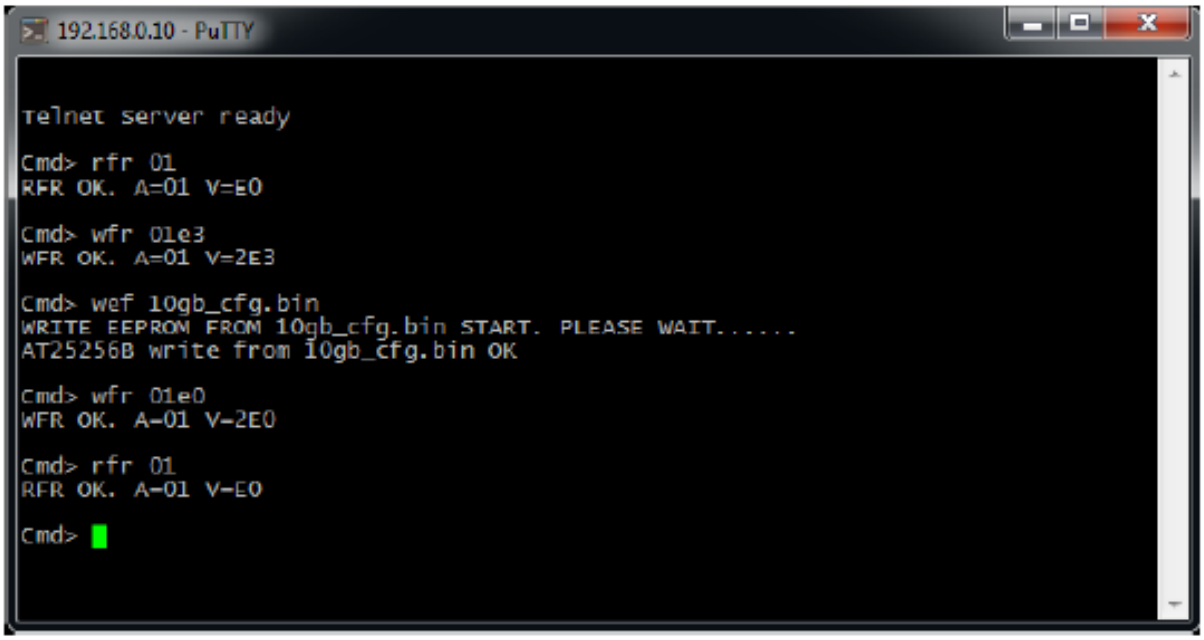
1. Test reading of the EEPROM register contents of multiplexer. 4 most significant bits of this register always restore 0xE.

2. Switching the microcontroller to the configuration EEPROM 88E6185.

3. Loading the Program Configuration Unit “gbs_cfg1.bin” to the configuration EEPROM 88E6185. In order for the changes to take effect (for the newly written configuration to become active), you should perform the power supply on/off switching cycle of the KIC551/KIC551RC module.

4.2.4 Booting the Program Configuration Unit of the 10 Gbit Ethernet controller

The Program Configuration Unit of the 10 Gbit Ethernet controller contains the settings of VLSI parameters of the Intel 82599EN controller: MAC-address, Power Management registers, LED registers, PHY registers and others.
The working Program Configuration Unit is stored in the configuration EEPROM AT25256B of the 10 Gbit Ethernet 82599EN controller.
For synthesis of the Program configuration Unit, you can use the “lanconf.exe” utility provided by Intel for its controllers. Information on the purpose and programming of service registers VLSI 82599EN can be obtained in 82599-10-gbe-controller-datasheet.pdf [4], see Annex G).
Below you can find an example of booting the Program Configuration Unit, located in the “10gb_cfg.bin” file in the root directory on NAND drive, using the Telnet connection.
For booting a copy of the Program Configuration Unit from NAND drive, you should perform the following sequence of instructions:



1. Test reading of the EEPROM register contents of multiplexer. 4 most significant bits of this register always restore 0xE.

2. Switching the microcontroller to the configuration EEPROM 82599EN.

3. Loading the Program Configuration Unit “10gb_cfg.bin” to the configuration EEPROM 82599EN.

4. Disconnecting the microcontroller from the configuration EEPROM 82599EN.

5. Confirmation that multiplexer has returned to the initial state.

In order for the changes to take effect (for the newly written configuration to become active), you should perform the power supply on/off switching cycle of the peripherals of the KIC551/KIC551RC module.

It is possible that you will have to upgrade the drivers for the 82599EN controller during the first start-up.

4.2.5 Booting the Program Configuration Unit’s FPGA (main/reserved)

To improve the system fault tolerance, the module’s control FPGA, in addition to the main configuration EEPROM, has an additional reserved EEPROM. If the contents of the main EEPROM are destroyed, FPGA loads data from the reserved EEPROM, which is automatically connected independently from any software.

If it is necessary (e.g., for programming the main EEPROM via JTAG FPGA interface), the use of the reserved EEPROM can be disabled manually using the SA1.1 microswitch (position “ON” – means the reserved EEPROM is disabled, see Fig. 3.2 - Microswitches SA1 and SA2, Table 3.7 – Box of SA1 microswitches).

The HL13 LED is located on the module’s board, indicating which of the configuration FPGA EEPROMs is active (see Fig. 2.4, Table 2.1 – States of HL13 LED).

If necessary, the main EEPROM can also be reprogrammed via Telnet, same as the previous Program Configuration Units.

The contents of the reserved EEPROM can also be updated via Telnet, provided that it is the reserved EEPROM which was used for booting the module. This can be achieved by forcibly erasing the contents (having written an empty Program Configuration Unit into it) of the main EEPROM and perform the power supply on/off switching cycle of the KIC551/KIC551RC module.

After updating the reserved EEPROM, you should restore the working Program Configuration Unit in the main EEPROM.

Attention!

If the booting was performed from the main EEPROM, the reserved EEPROM will be unavailable.

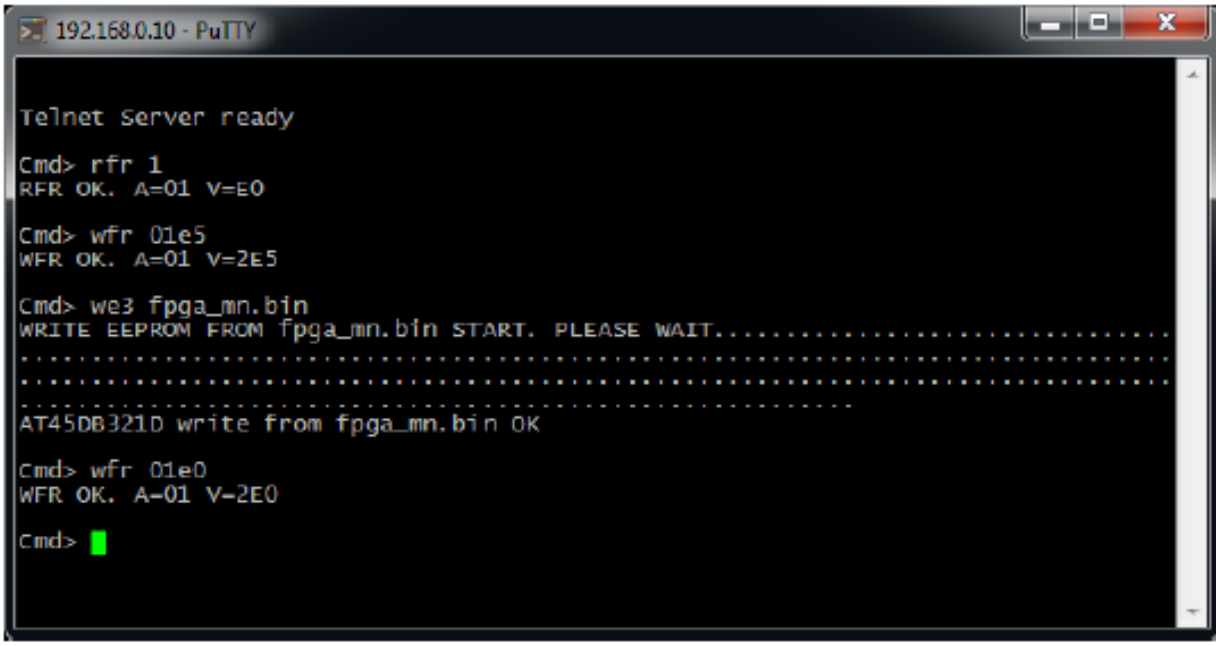
To control the version of the Program Configuration Unit loaded into the FPGA using Telnet connection, you can read its version written to the register 0x7F:

The figure shows that V=10. That means that the Program Configuration Unit has the version 1.0.

Attention!

Working Program Configuration Unit's FPGA of the KIC551/KIC551RC module is provided by the manufacturer or its authorized representatives. Loading the Program Configuration Unit created by other persons may result in blocking the operation of the KIC551 module.

Working Program Configuration Units of the main and reserved FPGAs are stored in the configuration EEPROM AT45DB321D.
Below is an example of loading the Program Configuration Unit from the main EEPROM, located in the "fpga_mn.bin" file in the root directory on NAND drive using the Telnet connection.
To load a copy of the Program Configuration Unit from NAND drive, you should perform the following sequence of instructions:



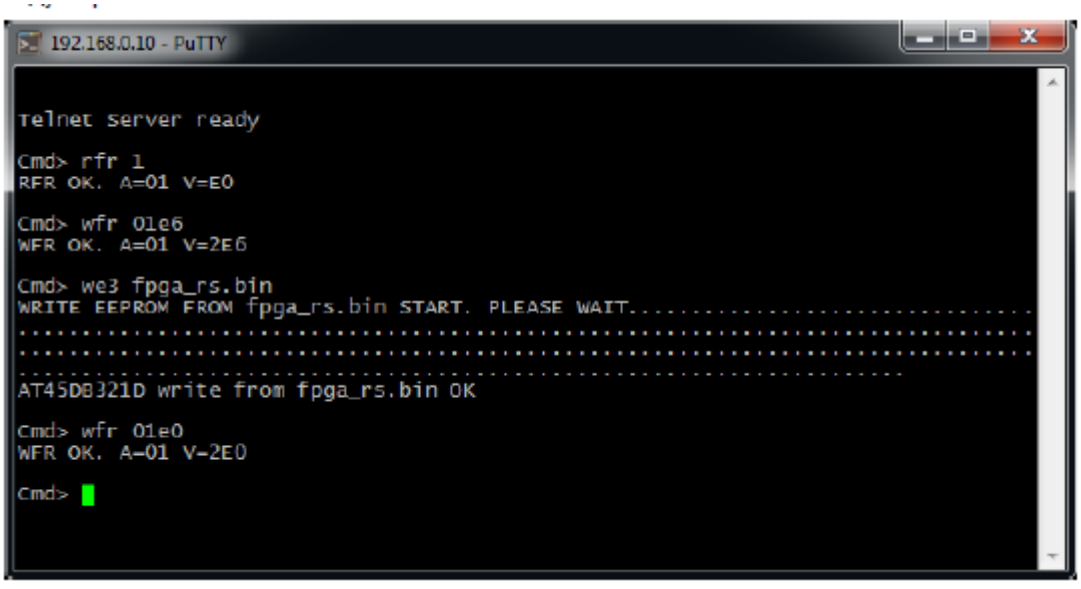
1. Test reading of the EEPROM register contents of multiplexer. 4 most significant bits of this register always restore 0xE.

2. Switching the microcontroller to the main configuration EEPROM FPGA. In this case, the illumination color of the HL13 LED will become green.

3. Loading the Program Configuration Unit “fpga_mn.bin” to the main configuration EEPROM FPGA. The process can take several minutes.

4. Disconnecting the microcontroller from the main configuration EEPROM FPGA.

In order for the changes to take effect (for the newly written configuration to become active), you should perform the power supply on/off switching cycle of the KIC551/KIC551RC module or use the program initialization of FPGA by means of the microcontroller (where the peripheral devices connected to the KIC551/KIC551RC module will also be initialized).
For booting the Program Configuration Unit “fpga_rs.bin” of the reserved EEPROM FPGA, the sequence of actions will be as follows:



1. Test reading of the EEPROM register contents of multiplexer. 4 most significant bits of this register always restore 0xE.

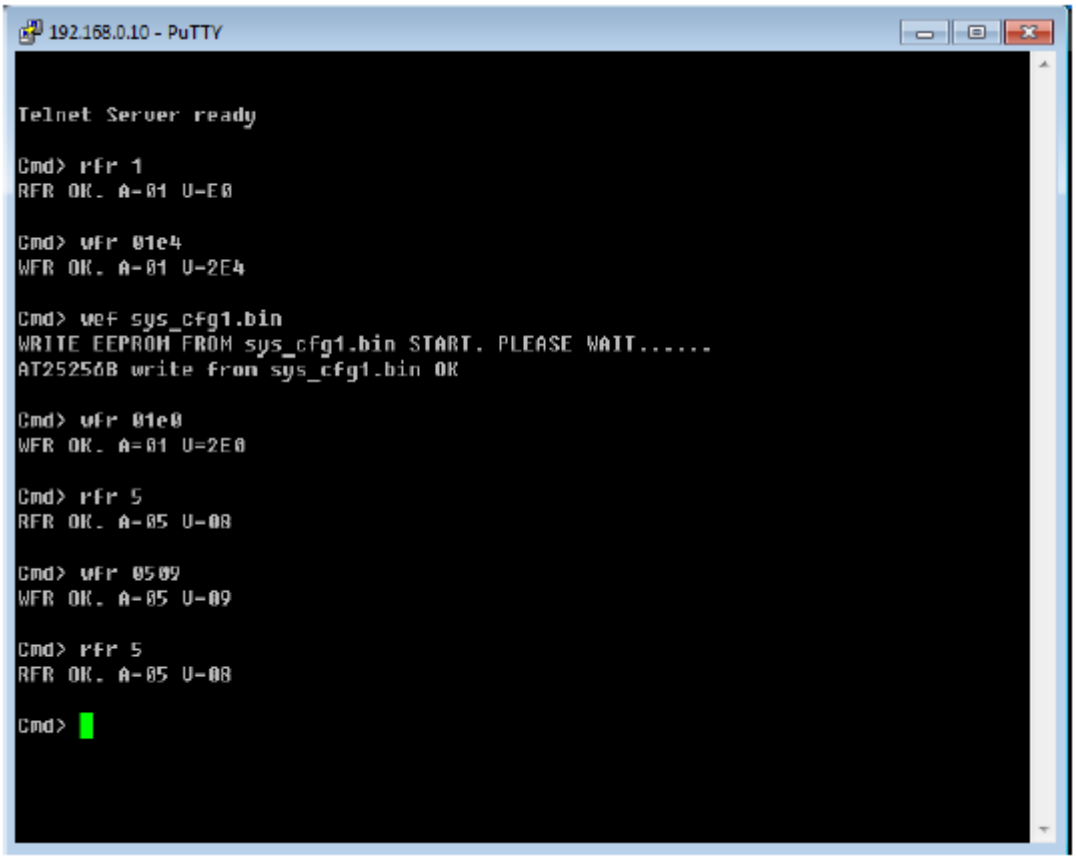
2. Switching the microcontroller to the reserved configuration EEPROM FPGA. The illumination color of the HL13 LED will remain to be red.

3. Loading the Program Configuration Unit “fpga_rs.bin” to the reserved configuration EEPROM FPGA. The process may take several minutes.

4. Disconnecting the microcontroller from the reserved configuration EEPROM FPGA.
If the main configuration EEPROM FPGA was erased to modify the reserved configuration EEPROM FPGA, then its contents should be restored following the above algorithm.
In order for the changes to take effect (for the newly written configuration to become active), you should perform the power supply on/off switching cycle of the KIC551/KIC551RC module or use the FPGA program initialization by means of the microcontroller (where the peripheral devices connected to the KIC551/KIC551RC module will also be initialized).

4.2.6 Booting the system Program Configuration Unit

The system Program Configuration Unit contains settings of the PCI Express VLSI strap signals of the PEX8764 switch, which define interaction over PCI Express lines between the KIC551/KIC551RC module and peripherals installed in the system backplane. In addition to the described strap signals, the system Program Configuration Unit contains settings for some service registers.
The specified parameters for setting the strap signals enable to define configuration of the PCI Express ports, location of the Upstream port, assign which of the ports will work in the NT mode, set the operation speed of PCI Express lines, etc.
In case of each system initialization, if the SA1.3 switch is set to the “OFF” position (by default), the contents of the system Program Configuration Unit are automatically loaded into the configuration registers of the VLSI PCI Express of the PEX8764 switch.
To prepare the Program Configuration Unit of system settings, you can use the “Hex Editor” utility or a similar tool.
A detailed description of the system settings Program Configuration Unit is given in the subpargraph 4.2.11 Programming the system Program Configuration Unit.
The working PCU is stored in the configuration system EEPROM AT25256B.
Below is an example of booting the system settings Program Configuration Unit, located in the “sys_cfg1.bin” file in the root directory on NAND drive, using the Telnet connection.



1. Test reading of the EEPROM register contents of multiplexer. 4 most significant bits of this register always restore 0xE.

2. Switching the microcontroller to the system configuration EEPROM.

3. Loading the Program Configuration Unit “sys_cfg1.bin” to the system configuration EEPROM.

4. Disabling microcontroller from the system configuration EEPROM.

5. Reading the control register “System Control“ (value V=08h).

6. Reconfiguration start command: setting bit 0 of the “System Control” register (value V=09h).

7. Confirmation of the end of reconfiguration (bit 0 must be reset): reading the control register “System Control” (value V=08h). If the Program Configuration Unit is booted successfully, **FO** LED on the front panel of KIC551 module lights up green.
In order for the changes to take effect (for the newly written configuration to become active), you should restart the system or, depending on the type of changes made into the new Program Configuration Unit, perform the power supply on/off switching cycle of the KIC551/KIC551RC module.

Attention!

Due to the fact that the units of microcontroller and FPGA-PCI Express are independent, if a false Program Configuration Unit is loaded to the system configuration EEPROM, the user can take advantage of the above method to restore the full operational capability of the system.

Therefore, the user can remotely change the Program Configuration Unit of system settings and change the system configuration, respectively. In addition, the system can autonomously replace the Program Configuration Unit of the system settings according to the algorithm recorded in the microcontroller from a prespecified set of system PCUs located on the built-in NAND drive.

4.2.7 Management and control of the main parameters of the system

In addition to the functions of storing and loading the PCU, the microcontroller enables you to implement additional functions for managing the state of the system, as well as monitoring the readings of key sensors (measuring temperature and voltages).
Management functions supported by the microcontroller:

- Enabling /disabling the common power supply of the system (only if there is a power supply of +5 V_standby).
- Enabling the system start programmable delay.
- System configuration restart.
- Initialization of optical modules.
- Initialization of the hardware monitor.
- Enabling / Disabling the integrated 10 Gbit Ethernet controller.
- Switching the direction of I^2C interface.
- Enabling / Disabling the standard LEDs self-testing mode.
- Managing each of the 8 x front panel **PE** LEDs including the choice of illumination color.

If necessary, the set of management functions can be expanded.
Alongside with the management functions, the microcontroller supports the following control functions:

- The values of the main power supply voltages of the KIC551/KIC551RC module (LM87 resource).
- The temperature values of the of the KIC551/KIC551RC module's PCB (LM87 resource).
- Temperature values of the VLSI core power supply source of the PCI Express switch (LM87 resource).
- The values of the microcontroller's temperature (microcontroller's resource).
- Working efficiency of secondary power supplies of the KIC551/KIC551RC module.
- Current status of configuration EEPROM of the KIC551/KIC551RC module.
- Installed host and peripheral modules across the slots.

If necessary, the set of control functions can also be expanded.
The control and management functions can be accessed locally from the microcontroller or remotely – via Telnet connection using the FPGA registers modification commands (see **Annex B List of Telnet interface commands**).

4.2.8 Management functions

4.2.8.1 Enabling / Disabling the system power supply

This function enables you to manage the system power supply, usually installed in the system crate.
To support the function of enabling/disabling, the system power supply should have the features compatible with the ATX specification, version 2.2:

- Control input PS_ON#;

▪ additionally: output of standby voltage “+5 V_standby” (5VSB) with load current no less than 3 A.

Control input PS_ON# of the power supply source should be connected to the “Utility Connector”, located on the crate’s backplane.
The system power is managed in accordance with the Table 4.3 by setting or resetting bit 0 of the “Power Control” register with the address 03 (the addresses are given in hexadecimal form).

Table 4.3 – Register 03, Bit 0

State	Function
0	Disabling the primary power source of the system
1	Enabling the primary power source of the system (by default)

Attention!
For proper operation of the power supply, the duration of the enabling / disabling cycle should be no less than 5 seconds.

An example of the sequence of commands for disabling the power supply:
CMD>rfr 03 - Reading the current state of the “Power Control” register. Then, bit 0 should be reset in the read value (for example, for the read value V = 03h).
CMD>wfr 0302 – Power supply source is disabled.
To enable the power supply source, you should set the bit 0 of register 03:
CMD>rfr 03 - Reading the current state of the “Power Control» register. Then, bit 0 should be set in the read value (for example, for the read value V=02h).
CMD>wfr 0303 – Power supply source is enabled.

4.2.8.2 Enabling / Disabling the Programmable Delay of System Start and Delay Time Management

If necessary, this function enables you to delay system initialization by activating the PLT_RST # signal at the initial startup. Setting the delay time is software-based.

The maximum available delay time is 54 seconds, with a programming pitch of 426 ms.
The program delay is disabled by default.
Unlike the functions managed through the FPGA service registers, the program delay parameters are configured in the eighth byte of the PCU system settings. A detailed description of the delay byte is given in subparagraph **4.2.11 Programming the system PCU**.

Restart of system configuration

The system configuration restart function enables you to activate a newly written system PCU without the need to perform the power supply on/off cycle.

In order to initiate the data reboot procedure from the system Program Configuration Unit, you should set the bit 0 of the “System Control” register with address 05 (Table 4.4).

Table 4.4 – Register 05, bit 0

State	Function
0	Normal operating mode, restart is over (by default)
1	The restart process is enabled

Attention!
New version of the Program Configuration Unit should be stored in the configuration EEPROM prior to the boot start. In this case the configuration EEPROM should be connected to the FPGA (register’s value with the address 01: 0E0h).

Example of a command sequence for rebooting the system configuration:

CMD>rfr 05 - Reading the current state of the “System Control” register. Next, set the read value to bit 0 (for example, for the read value V=08h).

In order to reboot the system configuration, bit 0 of register 05 is set using the command:

CMD>wfr 0509 – Reboot of the configuration PCU has been initiated.
CMD>rfr 05 - Reading the current state of the “System Control” register. In the read value, check the bit 0. If bit 0 is reset, the reboot process is complete.

An example of a complete reboot cycle for a configuration PCU is described in the subsection 4.2.6 Booting the system PCU.

Initialization of optical modules

This function works with KIC551-02/KIC551RC-02 modules, equipped with optical receiver and transmitter.

The function of the optical receiver and transmitter modules initialization makes it possible to disable the specified elements of the KIC551-02/KIC551RC-02 module by a forced installation of the "Reset" line of the optical modules to the active state.

In order to activate this mode, set bit 1 of the “System Control” register with the address 05 (Table 4.5).

Table 4.5 – Register 05, bit 1

State	Function
0	Standard operating mode. Optical modules are enabled (by default)
1	Optical modules are disabled

An example of a sequence of commands for enabling/disabling optical modules.

To disable optical modules:

CMD>rfr 05 - Reading the current state of the “System Control” register. Further, in the read value, bit 1 should be set (for example, for the read value V = 08h).

To disable the optical modules, bit 1 of register 05 is set by the following command:

CMD>wfr 050A - Optical modules are disabled.

In order to enable the optical modules:

CMD>rfr 05 - Reading the current state of the “System Control” register. Next, in the read value, you should reset bit 1 (for example, for the read value V = 08h).

To enable the optical modules, bit 1 of register 05 is reset by the following command:

CMD>wfr 0508 - Optical modules are enabled.

Initialization of Hardware Monitor

This feature allows hardware to disable the Hardware chip of the LM87 monitor or to quickly set the internal registers of this chip to its original state.

To activate the specified mode, you should set bit 2 of “System Control” register with the address 05 (Table 4.6).

Table 4.6 – Register 05, bit 2

State	Function
0	Standard operation mode. Hardware monitor is enabled (by default)
1	Hardware Monitor is disabled

An example of a sequence of commands for enabling / disabling the Hardware Monitor.

To disable the Hardware Monitor:

CMD>rfr 05 - Reading the current state of the “System Control” register. Further, in the read value, bit 2 should be set (for example, for the read value V = 08h).

TO disable the Hardware Monitor, bit 2 of register 05 is set by the following command:

CMD>wfr 050C - Hardware Monitor is disabled.

In order to enable the Hardware Monitor:

CMD>rfr 05 - Reading the current state of the “System Control” register. Further, in the read value, you should reset bit 2 (for example, for the read value V = 08h).

To enable the Hardware Monitor, bit 2 of register 05 is reset by the following command:

CMD>wfr 0508 - Hardware Monitor is enabled.

Enabling/Disabling the integrated 10 Gbit Ethernet controller

This function makes it possible to enable/disable the integrated 10 Gbit Ethernet controller.

The function is accessed via bit 3 of the “System Control” register with address 05 (Table 4.7).

Table 4.7 – Register 05, bit 3

State	Function
0	10 Gbit Ethernet controller is disabled
1	10 Gbit Ethernet controller is enabled (by default)

Example of command sequence for enabling / disabling a 10 Gbit Ethernet controller.
In order to disable the 10 Gbit Ethernet controller:

CMD>rfr 05 - Reading the current state of the “System Control” register. Further, in the read value, you should reset bit 3 (for example, for the read value V = 08h).

In order to disable the 10 Gbit Ethernet controller bit 3 of register 05 will be reset by the following command:
CMD>wfr 0500 - 10 Gbit Ethernet controller is disabled.

In order to enable 10 Gbit Ethernet controller:
CMD>rfr 05 - Reading the current state of the “System Control” register. Further, in the read value, bit 3 should be set (for example, for the read value V = 00h).

In order to enable 10 Gbit Ethernet controller, bit 3 of register 05 is set by the following command:
CMD>wfr 0508 - 10 Gbit Ethernet controller is enabled.An example of the instructions sequence for enabling/disabling the 10 Gbit Ethernet controller.
To disable the 10 Gbit Ethernet controller:
CMD>rfr 05 – Reading the current status of the “System Control” register. Then, bit 3 should be reset in the read value (E.g., for the read value V = 08h).
To disable the 10 Gbit Ethernet controller, bit 3 of register 05 is reset by the command:
CMD>wfr 0500 - 10 Gbit Ethernet controller is disabled.

To enable the 10 Gbit Ethernet controller:
CMD>rfr 05 - Reading the current status of the “System Control” register. Then, bit 3 should be set in the read value (E.g., for the read value V = 00h).
To enable the 10 Gbit Ethernet controller, bit 3 of the register 05 is set by the command:
CMD>wfr 0508 - 10 Gbit Ethernet controller is enabled.

Switching direction of the I^2C interface
This function enables you to connect the I^2C bus of the peripherals integrated into the module to an FPGA or microcontroller.
The function is accessed via bit 4 of the “System Control” register with the address 05 (Table 4.8).

Table 4.8 – Register 05, bit 4

State	Function
0	I^2C bus is connected to the microcontroller (by default)
1	I^2C is connected to the FPGA

An example of a sequence of commands for switching the I^2C bus.
To connect the I^2C bus to FPGA:

CMD>rfr 05 – Reading the current status of the “System Control» register. Then, bit 4 should be set in the read value (E.g., for the read value V=08h).
To connect I^2C bus to the FPGA, bit 4 of register 05 is set by the command:
CMD>wfr 0518 - I^2C bus is connected to the FPGA.
To connect the I^2C bus to the microcontroller:

CMD>rfr 05 – Reading the current status of the “System Control» register. Then, bit 4 should be reset in the read value (E.g., for the read value V=018h).

For the connection of I^2C bus with microcontroller, bit 4 pof the register 05 is reset by the command:

CMD>wfr 0508 - I^2C bus is connected to the microcontroller.

Enabling/Disabling the mode of standard LED self-testing.

The front panel LED self-test function is designed for visual examination of the following LEDs located on the module’s front panel:
PE1 - PE8, SYS, OVH, FO and UP.

During the examination, the specified LEDs are enabled for about 1 second illuminated with one color, and after a pause of 1 second with no illumination, they turn on for 1 second illuminated with another light.

Access to the function is enabled via bit 0 of the LED Control register with the address 06 (Table 4.9).

Table 4.9 – Register 06, bit 0

State	Function
0	Standard mode of LED operation (by default)
1	LED self-testing mode

Control of the Front Panel PE LEDs

The function enables to control the front panel **PE1** - **PE8** in the manual mode.

To control the LEDs, two registers are used: the register with the address 06 "LED Control" and the register with the address 07 "LED Data".

Bits 1 and 2 of the “LED Control» register define the illumination color: red, green or orange.
Eight bits of the “LED Data» register determine which of the LEDs - **PE1** - **PE8** will be enabled.
Whereby bit 0 of the register corresponds to the LED **PE1, bit 1 – PE2, etc.**

In this case, the algorithm for using the function may be as follows:
1. In the register "LED Control", the desired color of the LEDs is set by using the bits 1 and 2.
2. In the register “LED Data», the relevant bit for enabling the desired LED is set.

Table 4.10 shows the options for setting the color bits of the “LED Control” register:

Table 4.10 – Register 06, bits 1 and 2

LED illumination color	Bit 2	Bit 1
Control of the manual signal indication is enabled	0	0
Green	0	1
Red	1	0
Orange*	1	1

** Since orange is obtained by mixing red and green, due to the physical design of the two color LEDs, the result color can vary from yellow to red depending on the viewing angle.*

Description of the bits of the "LED Data" register is given in the table:

Table 4.11 – Register 07

Register 07 "LED Data"	"PE" LED
Bit 7	PE8
Bit 6	PE7
Bit 5	PE6
Bit 4	PE5
Bit 3	PE4
Bit 2	PE3
Bit 1	PE2
Bit 0	PE1

If bit in the "LED Data» register is set, then the relevant **PE** LED is enabled.

4.2.9 Control functions

Control of the main parameters of the KIC551 module using the LM87 Hardware Monitor.

To monitor the main supply voltages and temperatures, the KIC551 / KIC551RC board has a built-in LM87 Hardware Monitor.

The readings are taken by the Telnet-client interface, by issung the command:

Cmd> lm87?

The result of this command is shown below:

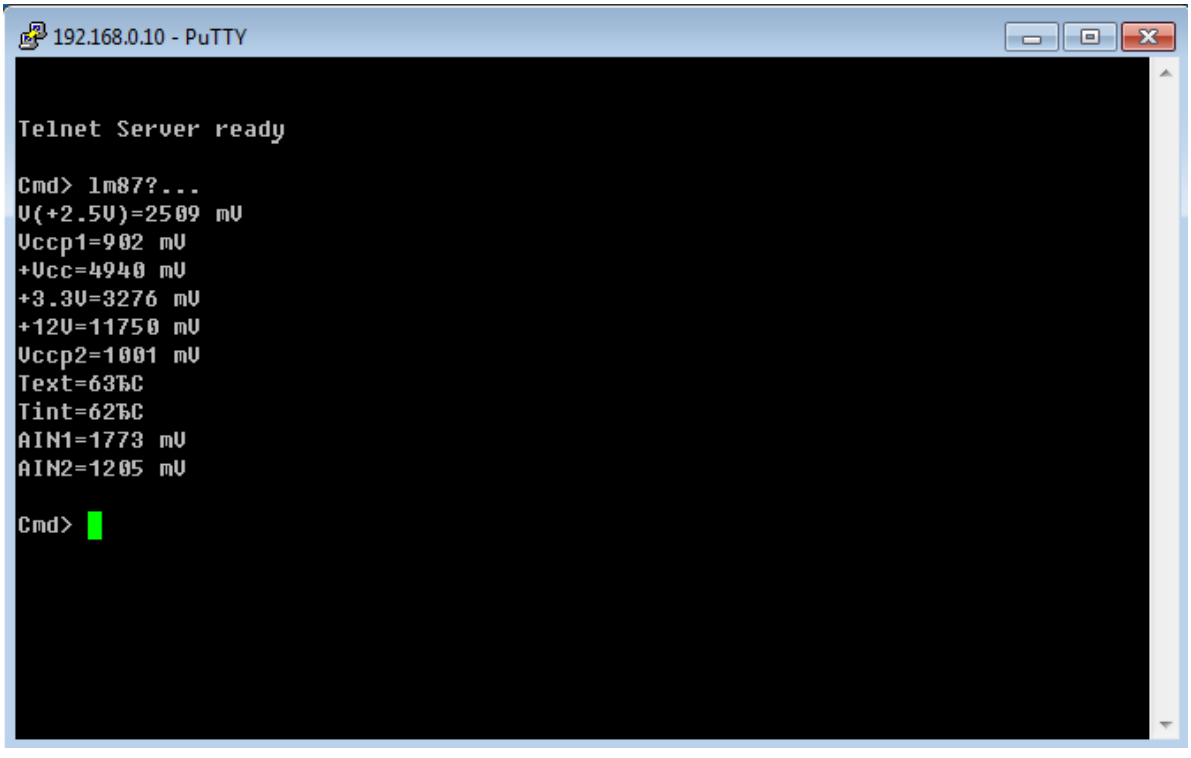


Table 4.12 provides the description of the monitored parameters corresponding to the specified values:

Table 4.12 – Main supply voltages

Notation	Description	Nominal value	Tolerance, %
V (+2.5 V)	Power voltage of optical transmitters/receivers	+ 2.5 V	5
Vccp1	Power supply voltage of the VLSI core of the PCI Express switch	+0.9 V	5
+Vcc	Reference power supply voltage of LM87	+5 V	5
+3.3 V	Main system power supply voltage	+3.3 V	5
+12 V	Input power supply voltage of the module	+12 V	10
Vccp2	Power supply voltage of digital units of PHY microchips	+1 V	5
AIN1	Power supply voltage of VLSI output buffers of PCI Express switch	+1.8 V	5
AIN2	Power supply voltage of the VLSI core of 10Gb Ethernet switch	+1.2 V	5

Table 4.13 – Monitored temperature values

Notation	Description	Maximum temperature
Text	Temperature of the PCB at the point under VLSI of PCI Express switch	105
Tint	Temperature of the printed circuit board in the free area	105

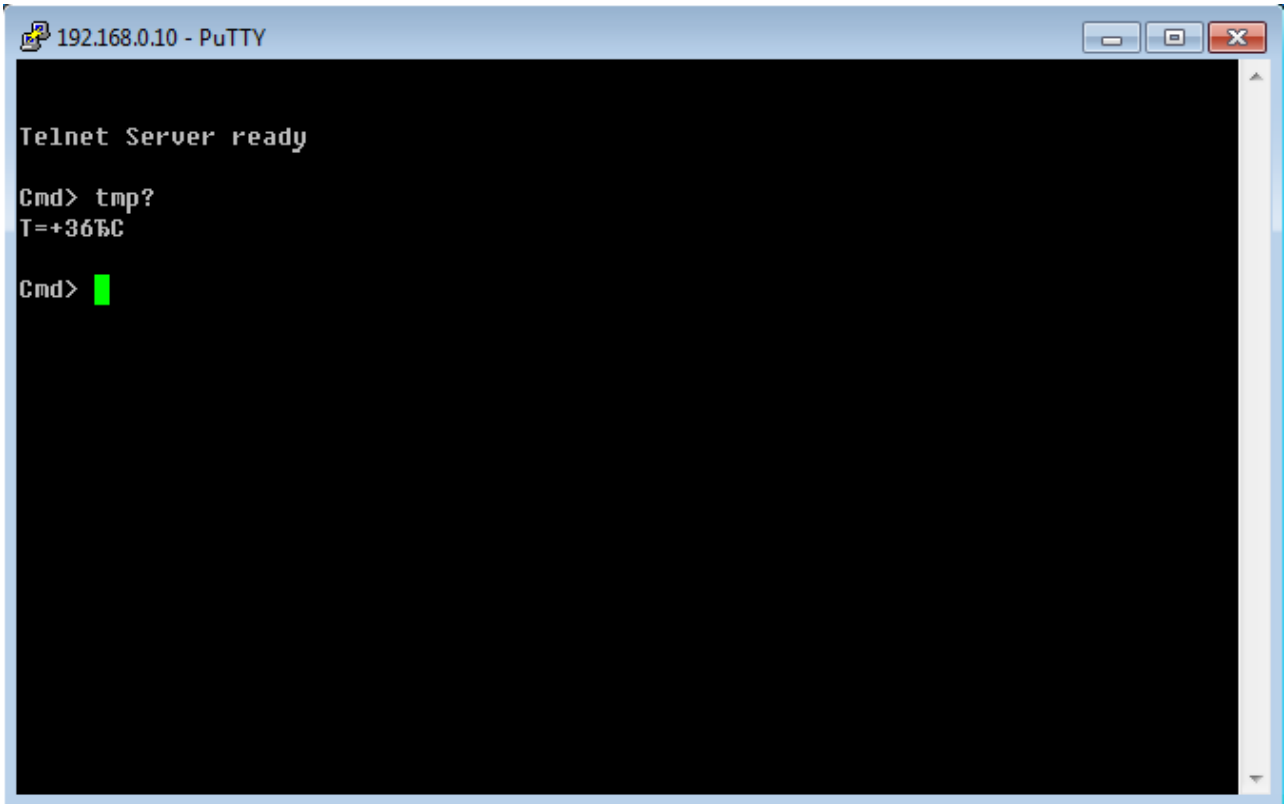
In addition, temperature of VLSI chip of PCI Express switch is controlled by a software-based method using a query of the special-purpose VLSI register (Table 4.13).

Control of the microcontroller temperature

In addition to temperature control by LM87 hardware monitor, the microcontroller's temperature can also be controlled by an integrated microcontroller temperature sensor.

Taking readings as with the Hardware monitor is via the Telnet-client interface by issuing the command:

Cmd> tmp?



The microcontroller recovers the temperature of its chip.

Controlling performance of the secondary power supply units of KIC551/KIC551RC

In order to remotely monitor operation of the secondary power sources and to quickly diagnose possible malfunctions, the module's FPGA has a register with the address 02 – "Power Status" (Table 4.14).

Table 4.14 – Register 02

Bit	Function
7	Control of system main power source. 0 - prohibited, 1 – permitted
6	Reserved
5	Power source of Gigabit Ethernet switch. 0 – failure, 1- operation
4	Power supply source +3.3 V. 0 - failure, 1- operation
3	Power supply source +2.5 V. 0 - failure, 1- operation
2	Power supply source +1.8 V. 0 - failure, 1- operation
1	Power supply source +1.2 V. 0 - failure, 1- operation
0	Power supply source +0.9 V. 0 - failure, 1- operation.

Bit 7 of the 02 register indicates whether the main power source control is available or not. During the first module's power-on, the main power supply is blocked in order to avoid an emergency situation.

Bit 5 of register 02 is intended for registering the event in the microcontroller's system log, since if the power supply of the Gigabit Ethernet switch fails, you will not be able to use the Telnet connection.

[1] Starting from the eeprog 1.1 utility version

Bits from 4 to 0 indicate the states of output voltages of the relevant module's power supply sources.

Controlling the current status of EEPROM configuration

This function is designed for proper addressing to configuration EEPROM while operating in the automatic mode at high speed, mainly in case of autonomous operation of microcontroller unit with EEPROM (Table 4.15).

Table 4.15 – Register 00

Bit	Function
7	Reserved
6	Reserved
5	Main EEPROM FPGA. 0 – available, 1 – unavailable
4	Reserved EEPROM FPGA. 0 – available, 1 – unavailable
3	EEPROM system configuration. 0 – available, 1 - unavailable
2	EEPROM 10Gb Ethernet controller. 0 – available, 1 - unavailable
1	EEPROM Gigabit Ethernet switch. 0 – available, 1 - unavailable
0	EEPROM PCI Express switch. 0 – available, 1 - unavailable

Control of the installed host and peripheral modules by slots

The specified function returns data on the state of peripheral slots of the system. All the devices will be recognized: both standard ones with the lines PCIE_PRSNT# set to logical zero and the special-purpose ones specified in the system Program Configuration Unit (in this case the lines PCIE_PRSNT# of these modules can be used as outputs of Reset signal to be broadcasted by KIC551/KIC551RC to the other peripheral devices in the backplane).

Table 4.16 – Register 04

Bit	Function
7	Slot 9 of backplane. 0 – available, 1 – unavailable.
6	Slot 8 of backplane. 0 – available, 1 – unavailable.
5	Slot 7 of backplane. 0 – available, 1 – unavailable.
4	Slot 6 of backplane. 0 – available, 1 – unavailable.
3	Slot 5 of backplane. 0 – available, 1 – unavailable.
2	Slot 4 of backplane. 0 – available, 1 – unavailable.
1	Slot 3 of backplane. 0 – available 1 – unavailable.
0	Slot 2 of backplane. 0 – available 1 – unavailable.

The slots are numbered in accordance with the numbers specified on the backplane (Slot #1 – system slot).

The modules installed into peripheral slots and not defined in the register 04 "System Status", are not detected by the system and will be operating on an individual basis (there won't be any in the general PCI space). In this case, communication with these modules can be set via Gigabit Ethernet interface of the backplane and via I^2C bus.

4.2.10 Additional control functions

In addition to the described control functions implemented via FPGA registers, the control MCU of the module has several functions implemented without the use of FPGA resources. For their operation, these functions use a standard I^2C bus stipulated in the Compact PCI Serial Specification.

4.2.11 Programming the system PCU

The system Program Configuration Unit contains information on the initial configuration of the system at the time of the start.

Flash EEPROM type AT25256 is used for storing the Program Configuration Unit.

In EEPROM bytes of the Program Configuration Unit are located in a sequential order (0, 1, 2, …), starting from the zero address.

4.2.11.1 Byte 0 – signature byte

The sequence always starts with the signature byte, the value of which indicates the accuracy of the contents of the Program Configuration Unit. When booting successfully, the front panel **FO** indicator lights up green. In those cases when this byte is not equal to 55h or, if the switch SA1.3 is set to “ON”, the PCU boot is interrupted, and for the settings of the system parameters the “default” settings are used according to the position of the switches SA1 and SA2 (see hardware description of the KIC551 / KIC551RC module, subsection 3.9.1. Hardware settings of the KIC551 / KIC551RC module).

In Table 4.17 below, there is an allotment of a standard bit sequence of the system Program Configuration Module.

In accordance with the consumer’s requirements, the Table 4.17 can be supplemented by other parameters required to be reset at system start. The FPGA Program Configuration Unit will be adjusted accordingly too.

Table 4.17 – Sequence of bits of the system Program Configuration Unit

Byte #	Bit #	Functional purpose	Bit value	Byte value in hexadecimal form
0	7	Signature mark confirming the accuracy of the Program Configuration Unit’s content. Is equal to 55h if the content is accurate. If the differs from 55h, the content of the Program Configuration Unit is ignored.	0	55
	6		1	
	5		0	
	4		1	
	3		0	
	2		1	
	1		0	
	0		1	
1	7	Reserve	0	0x
	6		0	
	5	Reserve	0	
	4		0	
	3	STN3 CFG1	Z	
	2		0/1	
	1	STN3 CFG0	Z	
	0		0/1	
2	7	STN2 CFG1	Z	xx
	6		0/1	

Byte #	Bit #	Functional purpose	Bit value	Byte value in hexadecimal form
	5	STN2 CFG0	Z	
	4		0/1	
	3	STN1 CFG1	Z	
	2		0/1	
	1	STN1 CFG0	Z	
	0		0/1	
3	7	STN0 CFG1	Z	xx
	6		0/1	
	5	STN0 CFG0	Z	
	4		0/1	
	3	NT1 UPSTRM PORTSEL 2	Z	
	2		0/1	
	1	NT1 UPSTRM PORTSEL 1	Z	
	0		0/1	
4	7	NT1 UPSTRM PORTSEL 0	Z	xx
	6		0/1	
	5	NT0 UPSTRM PORTSEL 2	Z	
	4		0/1	
	3	NT0 UPSTRM PORTSEL 1	Z	
	2		0/1	
	1	NT0 UPSTRM PORTSEL 0	Z	
	0		0/1	
5	7	VS0 UPSTRM PORTSEL 2	Z	xx
	6		0/1	
	5	VS0 UPSTRM PORTSEL 1	Z	
	4		0/1	
	3	VS0 UPSTRM PORTSEL 0	Z	
	2		0/1	
	1	VS MODE 1	Z	
	0		0/1	
6	7	VS MODE 0	Z	xx
	6		0/1	
	5	MGMT CFG EN	Z	
	4		0/1	
	3	P2P MODE	Z	
	2		0/1	
	1	GEN1 GEN2	Z	
	0		0/1	
7	7	Start Up Timer Enable	0/1	xx
	6	Start Up Timer Bit 6	0/1	
	5	Start Up Timer Bit 5	0/1	
	4	Start Up Timer Bit 4	0/1	
	3	Start Up Timer Bit 3	0/1	
	2	Start Up Timer Bit 2	0/1	
	1	Start Up Timer Bit 1	0/1	
	0	Start Up Timer Bit 0	0/1	
8	7	Customized LED Enable	0/1	xx
	6	Reserve	0/1	

Byte #	Bit #	Functional purpose	Bit value	Byte value in hexadecimal form
	5	Reserve	0/1	
	4	Reserve	0/1	
	3	LED PE1 Definition	0/1	
	2		0/1	
	1		0/1	
	0		0/1	
9	7	LED PE2 Definition	0/1	xx
	6		0/1	
	5		0/1	
	4		0/1	
	3	LED PE3 Definition	0/1	
	2		0/1	
	1		0/1	
	0		0/1	
10	7	LED PE4 Definition	0/1	xx
	6		0/1	
	5		0/1	
	4		0/1	
	3	LED PE5 Definition	0/1	
	2		0/1	
	1		0/1	
	0		0/1	
11	7	LED PE6 Definition	0/1	xx
	6		0/1	
	5		0/1	
	4		0/1	
	3	LED PE7 Definition	0/1	
	2		0/1	
	1		0/1	
	0		0/1	
12	7	LED PE8 Definition	0/1	xx
	6		0/1	
	5		0/1	
	4		0/1	
	3	Reserve	0/1	
	2	Reserve	0/1	
	1	Reserve	0/1	
	0	Reserve	0/1	

4.2.11.2 Bytes from 1 to 6 – strap signals of PCI Express switchboard

After the signature byte 0 there are six bytes (from 1 to 6) containing the strap signal settings for VLSI of PCI Express switchboard. To read more about these signals see [1] (Annex G).

4.2.11.3 Byte 7 – Setting the prestart delay timer

The delay is set after supplying power and permitting clock pulses to the backplane. The setting the delay may be required using special-purpose peripheral modules with an increased initialization time. Maximum delay time amounts to 54 s, interval – 426 ms.

Table 4.18 – Setting the values of prestart delay timer (byte 7 of system Program Configuration Unit)

Byte number	7 Start Up Timer Enable	6	5	4	3	2	1	0
Byte function	Timer On/Off	27.3s	13.6s	6.8s	3.4s	1.7s	852ms	426ms

The delay is set in accordance with Table 4.18 by adjusting the relevant bits 6-0. The specified delay (bits 6-0) is active if bit 7 (Start Up Timer Enable) is reset. Otherwise, the delay is switched off (by default).

4.2.11.4 Bytes from 8 to 12 – setting configuration of front panel LEDs PE1 – PE8

During operation of KIC551 with non-standard backplanes with a unique allocation and bit depth of PCI Express ports, for proper display of ports' activities it is required to reassign the PE1 – PE8 LEDs of the front panel to the other PCI Express ports (e.g. PCI Express x4 ports, placed on the standard backplane in slots #4 and #5, in the **customized backplane** can be aggregated into PCI Express x8 port and can be placed in the slot #6).

ANNEX A

List of FPGA internal function registers

#	Address	Name	Description		Type	Default value
1	00	EEPROM STATUS	Bit7	Reserved	RO	0
			Bit6	Reserved	RO	0
			Bit5	FPGA MAIN EEPROM. 0-EEPROM accessable, 1-EEPROM busy	HD	0
			Bit4	FPGA RESERVE EEPROM. 0-EEPROM accessable, 1-EEPROM busy	HD	0
			Bit3	SYSTEM EEPROM. 0-EEPROM accessable, 1-EEPROM busy	HD	0
			Bit2	10 Gbit Ethernet Controller EEPROM. 0-EEPROM accessable, 1-EEPROM busy	HD	0
			Bit1	Gigabit Ethernet Switch EEPROM. 0-EEPROM accessable, 1-EEPROM busy	HD	0
			Bit0	PCI Express Switch EEPROM. 0-EEPROM accessable, 1-EEPROM busy	HD	0
2	01	EEPROM CONTROL	Bit7	Reserved. Always return 0Eh	RO	1
			Bit6		RO	1
			Bit5		RO	1
			Bit4		RO	0
			Bit3	EEPROM Select Bit3	R/W	0
			Bit2	EEPROM Select Bit2	R/W	0
			Bit1	EEPROM Select Bit1	R/W	0
			Bit0	EEPROM Select Bit0	R/W	0
3	02	POWER STATUS	Bit7	Main System Power Supply Control. 0 - prohibited, 1 -accessable	HD	1
			Bit6	Reserved	RO	0
			Bit5	Gigabit Ethernet Switch DC-DC. 0 - malfunction, 1- work	HD	1
			Bit4	3.3V DC-DC. Main. 0 - malfunction, 1- work	HD	1
			Bit3	2.5V DC-DC. 0 - malfunction, 1- work	HD	1
			Bit2	1.8V DC-DC. 0 - malfunction, 1- work	HD	1
			Bit1	1.2V DC-DC. 10 Gbit Ethernet Controller Core. 0 - malfunction, 1- work	HD	1
			Bit0	0.9V DC-DC. PCI Express Switch Core. 0 - malfunction, 1- work	HD	1
4	03	POWER CONTROL	Bit7	Reserved	RO	0
			Bit6	Reserved	RO	0
			Bit5	Reserved	RO	0
			Bit4	Reserved	RO	0
			Bit3	Reserved	RO	0
			Bit2	Reserved	RO	0
			Bit1	Reserved	RO	0
			Bit0	System Power Control. 0 - ATX Power Supply OFF, 1 - ATX Power Supply ON	R/W	1
5	04	SYSTEM STATUS	Bit7	PCI Express Backplane Slot 9. 0 - Vacant, 1 - Occuped	RO	HD
			Bit6	PCI Express Backplane Slot 8. 0 - Vacant, 1 - Occuped	RO	HD
			Bit5	PCI Express Backplane Slot 7. 0 - Vacant, 1 - Occuped	RO	HD
			Bit4	PCI Express Backplane Slot 6. 0 - Vacant, 1 - Occuped	RO	HD
			Bit3	PCI Express Backplane Slot 5. 0 - Vacant, 1 - Occuped	RO	HD

#	Address	Name		Description	Type	Default value
			Bit2	PCI Express Backplane Slot 4. 0 - Vacant, 1 - Occuped	RO	HD
			Bit1	PCI Express Backplane Slot 3. 0 - Vacant, 1 - Occuped	RO	HD
			Bit0	PCI Express Backplane Slot 2. 0 - Vacant, 1 - Occuped	RO	HD
6	05	SYSTEM CONTROL	Bit7	Reserved	RO	0
			Bit6	Reserved	RO	0
			Bit5	Reserved	RO	0
			Bit4	I2C Interface Direction. 0 - Connect to MCU, 1 - Connect to FPGA	R/W	0
			Bit3	10 Gbit Ethernet Controller. 0 - Disable, 1 - Enable	R/W	1
			Bit2	Hardware Monitor Reset. 0 - Work, 1 - Reset	R/W	0
			Bit1	Optical Modules Reset. 0 - Work, 1 - Reset	R/W	0
			Bit0	Update Configuration. 0 - Work, 1 - Update	R/WS	0
7	06	LED CONTROL	Bit7	Reserved	RO	0
			Bit6	Reserved	RO	0
			Bit5	Reserved	RO	0
			Bit4	Reserved	RO	0
			Bit3	Reserved	RO	0
			Bit2	Red Light. 0 - No Light, 1 - Light	R/W	0
			Bit1	Green Light. 0 - No Light, 1 - Light	R/W	0
			Bit0	Test Mode. 0 - Disable, 1 - Enable	R/W	0
8	07	LED DATA	Bit7	PE LED8 Control. 0 - Off, 1 - On	R/W	0
			Bit6	PE LED7 Control. 0 - Off, 1 - On	R/W	0
			Bit5	PE LED6 Control. 0 - Off, 1 - On	R/W	0
			Bit4	PE LED5 Control. 0 - Off, 1 - On	R/W	0
			Bit3	PE LED4 Control. 0 - Off, 1 - On	R/W	0
			Bit2	PE LED3 Control. 0 - Off, 1 - On	R/W	0
			Bit1	PE LED2 Control. 0 - Off, 1 - On	R/W	0
			Bit0	PE LED1 Control. 0 - Off, 1 - On	R/W	0
9	7F	FIRMWARE VERSION	Bit7	FPGA Firmware Version	RO	HD
			Bit6		RO	HD
			Bit5		RO	HD
			Bit4		RO	HD
			Bit3		RO	HD
			Bit2		RO	HD
			Bit1		RO	HD
			Bit0		RO	HD

Annex B

List of Telnet Interface Commands

inf? – Output of firmware information
date? – Output of data
time? – Output of time
date DD.MM.YY – Setting the date
time HH:MM:SS – Setting the time
getsn – Reading serial number
setsn NNNNNNNN pw – Setting the serial number to NNNNNNNN(N=0..9) with password (password – Dolomant, starting with the upper case letter)
tmp? – output of the temperature of ARM integrated sensor
wpr XXYYYYZZZZZZZZ – writing the ZZZZZZZZ value to the YYYY register at the physical address XX (88E6185)
rpr XXYYYY – reading register YYYY at the physical address XX (88E6185)
initfs – initialization of the NAND drive file system
format [param] – NAND drive formatting, param – can have the value /LLEB (deletion of all blocks)
wfr XXYY – Writing to FPGA register the YY value at the XX address
rfr XX – Reading FPGA register at the XX address
weX fname – Writing a file named fname to SPI EEPROM (X=f for AT25256B, X=2 for AT93C66B or X=3 for AT45DB321D). If the file name is not specified, file name eepwr.bin will be used by default. SPI interface should be switched prior to the writing.
reX fname – reading SPI EEPROM to the file named fname (X=f for AT25256B, X=2 for AT93C66B or X=3 for AT45DB321D). If the file name is not specified, file name eeprd.bin will be used by default. SPI interface should be switched prior to the reading.
lm87en – starting of measurements using the LM87 hardware monitor
lm87? – reading the measured parameters from LM87
lm87sth XX - setting an upper actuation temperature threshold of “OVH” XX indicator on LM87. XX – threshold from an external temperature sensor in hexadecimal form and true complement representation (for below-freezing temperatures).
i2cw XXYYZZ - set reg YY on I^2C-device XX to ZZ
i2cr XXYY - read reg YY on I^2C-device XX
tcpstat – output of information on the status of TCP/IP stack
ipmac? – output of the current static IP address and MAC address, as well as IP address assigned by DHCP server. In order to change the static IP address the **ip.txt** file should be placed to the root directory of the NAND drive. Address format: 192.168.0.21. In order to change the MAC address, the **mac.txt** file should be placed to the root directory of the NAND drive. Address format: 0008B4AA0011. The static IP address is assigned in 1 minute, if there is no DHCP server in the system.

rinfo – output of network information on a remote computer
jbl – moving from the application to the network HTTP loader

Annex C

Characteristics of the peripherals' clock signals

Symbol	Parameters			Min	Typ.	Max.	Units	Notes
F_{in}	SRC/SRC# Input Frequency PLL Mode			95		105	MHz	6
	SRC/SRC# Input Frequency Bypass Mode			95		400	MHz	6
T_{rise} / T_{fall}	Rise and Fall Time (measured between 0.175V to 0.525V)			175		700	ps	2
ΔT_{rise} / ΔT_{fall}	Rise and Fall Time Variation					125		2
T_{pd}	Input to Output Propagation Delay	PLL Mode	PI6C20800B	-250		250	ps	
			PI6C20800BI	-450		450		
		Bypass Mode	PI6C20800B	-7.5		7.5	ns	
			PI6C20800BI	-8		8		
T_{skew}	Output-to-Output Skew (PI6C20800B)					50	ps	3
	Output-to-Output Skew (PI6C20800BI)					65		3
V_{HIGH}	Voltage HIGH (Measured at 100MHz @ 3.3V)			600		900	mV	2
V_{OVS}	Max. Voltage					1150		
V_{UDS}	Min. Voltage			-300				
V_{LOW}	Voltage LOW			-150		+150		2
V_{cross}	Absolute crossing poing voltages			250		550		2
ΔV_{cross}	Total Variation of V_{cross} over all edges					140		2
T_{DC}	Duty Cycle (Measured at 100 MHz)			45		55	%	3
$T_{jcyc-cyc}$	Jitter, Cycle-to-cycle (PLL Mode, Measurement for differential waveform)					60	ps	4
	Jitter, Cycle-to-cycle (BYPASS mode as additive jitter)							
J_{add}	Additive RMS phase jitter for PCIe 2.0			<0		1	ps	5
J_{add}	RMS phase jitter for PCIe 3.0	PLL L-BW @ 2M & 5M 1st H3			1.115	3	ps	
		PLL L-BW @ 2M & 4M 1st H3			1.211	3		
		PLL L-BW @ 2M & 5M 1st H3			1.116	3		
		PLL L-BW @ 2M & 4M 1st H3			1.425	3		
		PLL H-BW @ 2M & 5M 1st H3			0.646	1		
		PLL H-BW @ 2M & 4M 1st H3			0.644	1		
		PLL H-BW @ 2M & 5M 1st H3			0.646	1		
		PLL H-BW @ 2M & 4M 1st H3			0.579	1		

Notes:

1. Test configuration is R_s = 33.2Ω, Rp = 49.9Ω, and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.
4. Measured using M1 timing analyzer from Amherst.
5. Additive jitter is calculated from input and output RMS phase jitter by using PCIe 2.0 filter. ($J_{add} = \sqrt{(\text{output jitter})^2 - (\text{input jitter})^2}$)
6. –0.5% downnspread input

Annex D

Characteristics of the Gigabit Ethernet unit switch

Gigabit Ethernet unit switch has the following features:

- Distributed Switching Architecture (DSA) for cascading multiple devices and stacking multiple systems
- IEEE 802.1X MAC-based authentication
- Port-based VLANs supported in any combination
- High-speed switch fabric
  - High-performance look-up engine with support for up to a 8K MAC address entries with automatic learning and aging tags, IPv4 Type of Service (TOS), Differentiated Services (DiffServ), and IPv6 traffic class
  - Port-based VLANs supported in any combination
- QoS determined by port ID, IEEE 802.1p and multimedia traffic tags, IPv4 Type of Service (ToS), Differentiated Services (DiffServ), IPv6 Traffic Class, 802.1Q VLAN ID, destination MAC address, and source MAC address
- Supports port-based VLANs and up to the full 4K 802.1Q VLANs
- Extensive RMON statistics counters
- Link aggregation for up to 16 trunks of up to 8 ports each
- Port mirroring
- IEEE 802.1D/w/s Spanning Tree Protocol Support

Annex E

Characteristics of the output stage of AFBR-810 Avago Transmitter and input stage of AFBR-820 Avago Receiver

- Characteristics of the output stage of AFBR-810 Avago Transmitter:

Parameter	Symbol	Min	Typ	Max	Units
Output Optical Power: Average	$P_{O\ AVE}$			-1.5	dBm
Output Optical Power: Disabled	$P_{O\ OFF}$			-30	dBm
Extinction Ratio	ER	3			dB
Output Optical Modulation Amplitude	OMA	-5.25			dBm
Output OMA: Squelched				-27	dBm
Encircled Flux					
Center Wavelength		830		860	nm
Spectral Width - rms				0.85	nm
Output Rise/Fall Time				50	ps
Power On Initialization Time Tx Outputs	$t_{PWR\ INIT}$			500	ms
Reset Assert Time Tx Outputs	$t_{RSTL\ ON}$			500	ms
Reset De-assert Re-initialization Time Tx Outputs	$t_{RSTL\ OFF}$			500	ms
Output Disable Assert Time for Fault	$t_{DIS\ ON}$			100	ms
Output Squelch Assert Time for LOS	$t_{SQ\ ON}$			80	µs
Output Squelch De-assert Time for LOS	$t_{SQ\ OFF}$			80	µs
Inter-channel Skew				150	ps
Channel Latency			400		ps
Relative Intensity Noise OMA	RIN_{12} OMA			-124	dB/Hz
Accumulated Deterministic Jitter				30	ps
Accumulated Total Jitter				60	ps
Reference Link Output Eye Width	$t_{EYE\ REF}$	40			ps

Characteristics of AFBR-820 Avago optical receiver's input stage:

Parameter	Symbol	Min	Typ	Max	Units
Input Optical Power Sensitivity (OMA)				-11	dBm
Input Optical Power Saturation	$P_{SAT\ AVE}$	-1.0			dBm
Operating Center Wavelength		830		860	nm
Return Loss		12			dB
LOS Asserted Threshold – OMA	$P_{LOS\ OMA}$	-26	-19		dBm
LOS De-asserted – OMA			-17	-12	dBm
LOS Hysteresis		0.5	2		dB

Annex F

List of compatible equipment

- 10 Gbit Ethernet optical transceiver Avago AFBR-709ISMZ 850 nm;
- 1 Gbit Ethernet optical transceiver Network Logic NC5512-03-I;
- 1 Gbit Ethernet optical transceiver Network Logic NC3112-03-I;
- Twelve channel Transmitter and Receiver AFBR-820 Avago;
- Twelve channel Transmitter and Receiver AFBR-810 Avago;
- Schroff crate;
- System power supply source, compatible with ATX specification, version 2.2.

Annex G

List of references and web resources

1. Documentation for VLSI circuit PEX8764 (PEX_8764-AA_AB_Data_Book_v1.0_05Jun13.pdf).

2. Documentation for 88E6185 microchip (88E6185_Datasheet.pdf).

3. Documentation for 88E1340 microchip (MV-S104603-00_88E1340_88E1322_Datasheet.pdf).

4. Documentation for VLSI circuit 82599EN (82599-10-gbe-controller-datasheet.pdf), see https://www.intel.ru/content/dam/www/public/us/en/documents/datasheets/82599-10-gbe-controller-datasheet.pdf

ANNEX H: DISCLAIMER

This Disclaimer contains special operating conditions of Fastwel in the following areas: intellectual property, warranty policy, conditions of the order and delivery.

1 INTELLECTUAL PRORETY

1.1 If any infraction, interference, improper use, illegitimate exploitation and/or violation of the industrial and/or intellectual property rights of any third party and/or property, exploitation during the use of Fastwel Embedded Module will take place – Fastwel does not guarantee to replace the materials, computer programs, procedures or equipment affected by the complaint and under no circumstances doesn't bear responsibility in any form for possible refusal in case of such a replacement.
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1.3 Fastwel is not responsible for possible incidents and losses, related to the operation of end devices, in which the original Fastwel equipment is used.

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2.1 When the detected flaws in an element can be corrected without decreasing the foreseen technical features and functionality for it, User may demand Fastwel the urgent correction of the failures in additionally agreed period and an increasing of the period of the guarantee of the element equal as the time elapsed from the formal request to repair the failures, until the receipt of the repaired element. All costs associated to the correction of failures, included those of assembly, dismantle, transport, tests, etc, if they exist, shall be prosecuted according the Warranty Policy of Fastwel.

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3.1 The general rule is that all Fastwel equipment prices are determined with due consideration of delivery under the EXW terms and conditions (Incoterms 2010). Delivery of the products under other terms and conditions should be preliminary agreed and stated in writing between the parties.
3.2 Unless otherwise expressly agreed with Fastwel, all the deliveries of Fastwel equipment will be carried out only after the official purchase order is obtained and provided that the ordered products have been prepaid in full. Other terms and conditions of cooperation should be made in writing.
3.3 Any delivery of Fastwel electronics is submitted with the right package in accordance with the current rules and standards in the Member States of the European Economic Area. The purchaser independently bears all risks regarding the compliance of package and marking of Fastwel products with legislation requirements being in effect at the place of purchased products destination (in the buyer's country). The specified condition excludes unequivocally any liability of Fastwel for possible non-compliance of package and marking of products with the requirements of legislation of the country of products destination.
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3.5 Each package unit is labeled on the exterior area with the indications of product's Part Number and Serial Number.
3.6 The support documents for the order should be made either in English or in Russian unless otherwise agreed between parties in writing.
3.7 Fastwel does not pay penalties and does not cover costs associated with delay in the delivery of the products caused by actions of the third parties, force-majeure etc. - Fastwel doesn't bear any responsibility for non-execution or inadequate execution of the obligations in a case when it is caused by actions of the third parties (for example producers or suppliers of accessories), force majeure etc.
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4.1 Fastwel has the obligation to respect the current Russian legislation (including, but not limited to environmental, labor, social laws) in each moment and to apply it to its embedded electronics considering all and each execution phase, that is to say, from the design until the commissioning and subsequent maintenance. In this regard Fastwel is not liable to the user or other persons in connection with possible changes of the company's rules (including, but not limited to warranty, ordering policy) caused by changes of the Russian legislation.
4.2 Unless otherwise expressly agreed in writing, Fastwel provides no training for assembly\installation\adjustment\operation of its equipment.