CPC109
Controller Module

Excerpts from User Manual

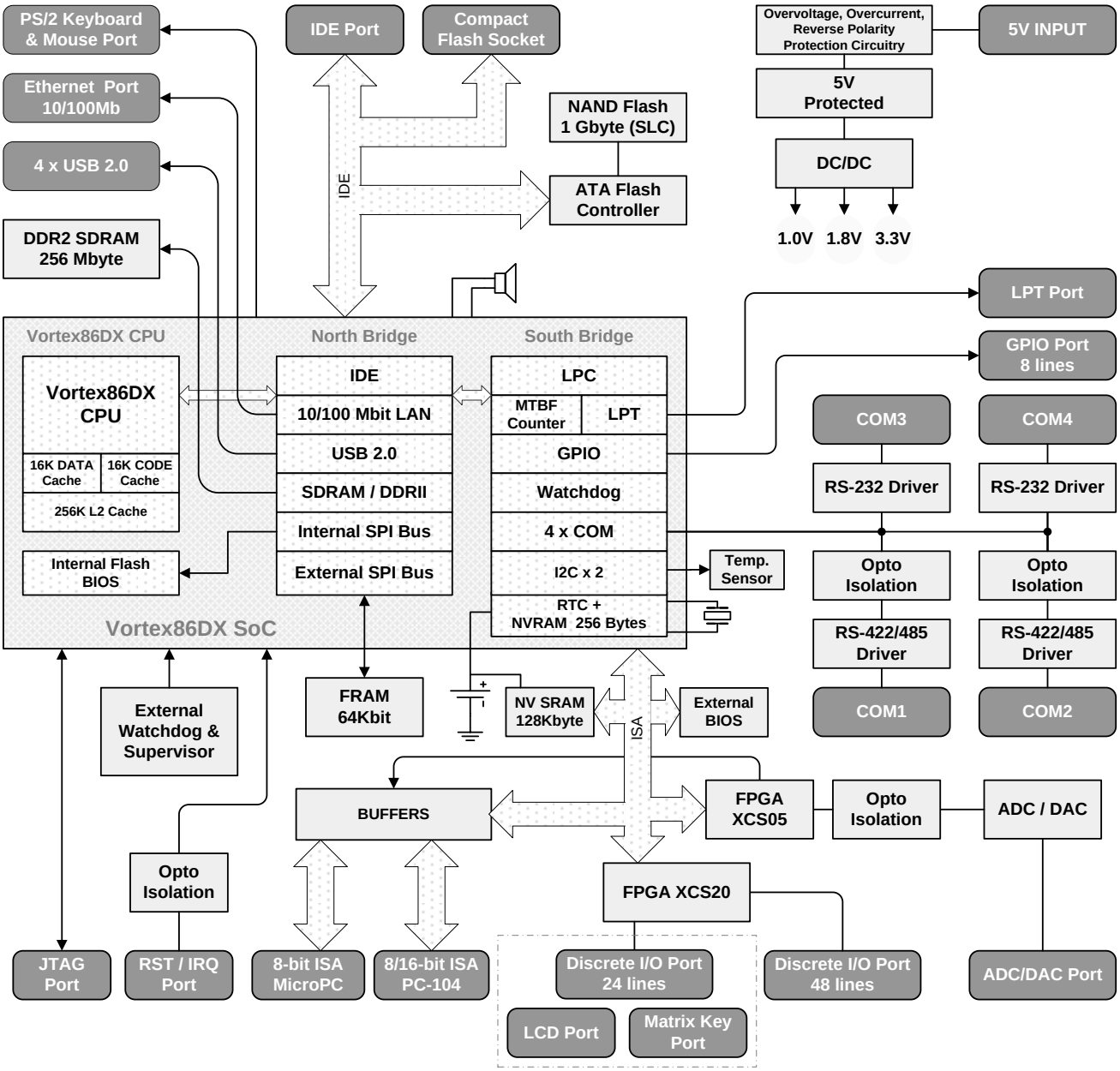
Version 2.0

December 2015

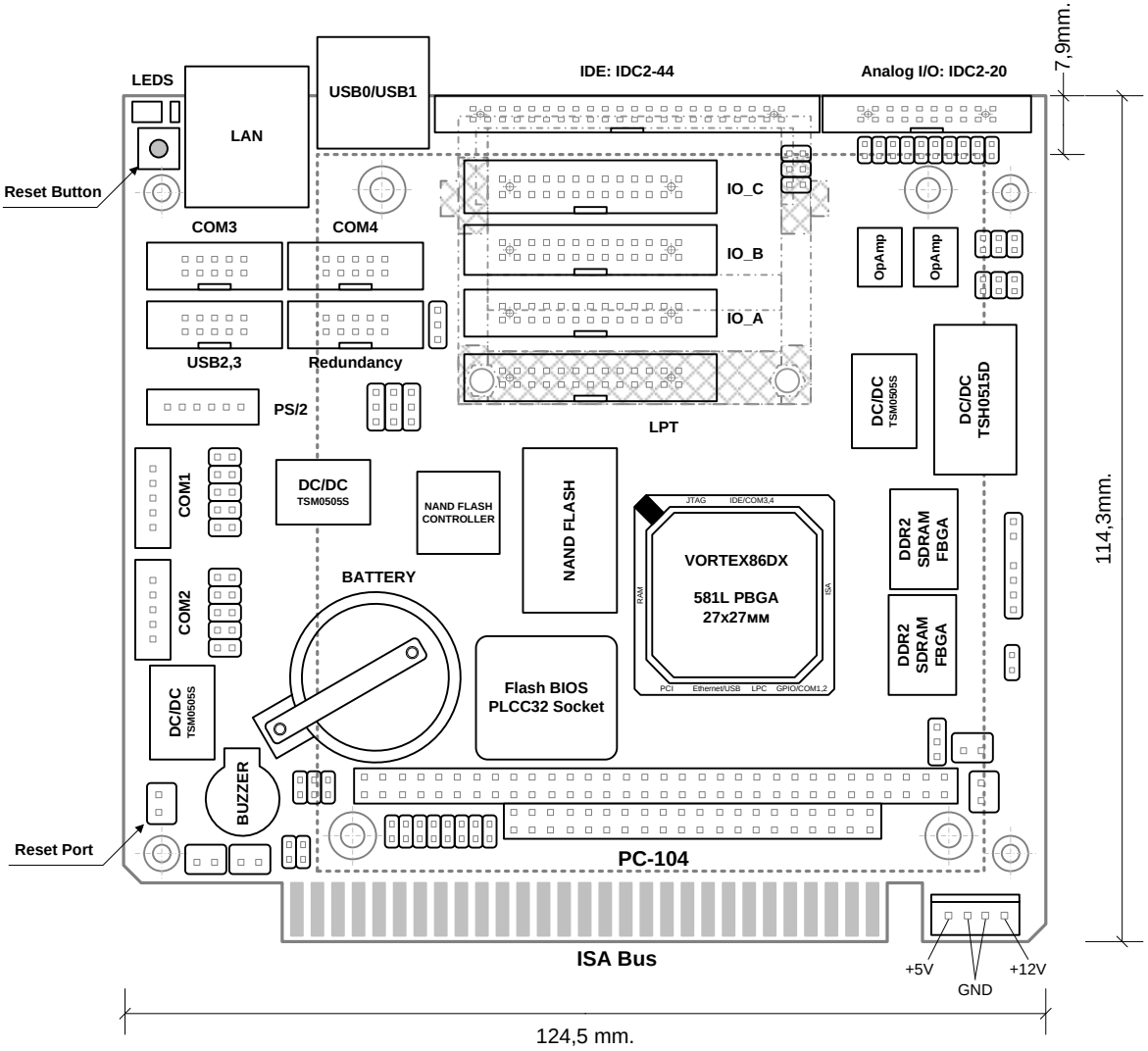
[1] Description

Note: square brackets to the left of headings include the heading number from the original manual.

[1.5] Functional Diagram



[1.6] Layout



[1.7] Versions

Code	Version	COM1, COM2 (RS-422/485)	Temp. Sensor	NV SRAM	Discrete I/O	Analog I/O
CPC10901	MX	Isolated, lightning protection	+	128 KB	72 channels (varistor protected inputs)	8 inputs / 2 outputs (isolated)
CPC10902	BS	Isolated, lightning protection	+	128 KB	72 channels (varistor protected inputs)	–
CPC10903	LC	Isolated	–	–	–	–

[1.10.13] Discrete Input/Output Port (XP11, XP12, XP13)

Universal input/output port (XP11, XP12, XP13 connectors) is compatible with UNIO96-5 module with regard to pinouts and control. The port is realized on the basis of FPGA programmable chip (XCS20) and provides input/output of 72 logic signals. The channels are devided into 3 groups of 24 channels each and routed to 26-contact dedicated connectors. Each channel has varistor protection against pulse noise (5.6 V overvoltage protection).

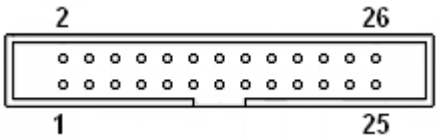
Functions of the port can be reprogrammed in-system with special utilities without need to switch power off.

The channels of the port can be used to control the process interface units with galvanic isolation, for pulse counting, frequency measurement and generation, timing charts generation etc.

Binary files with circuit variants for UNIO port programming are supplied with the module; they have the same names and descriptions as for UNIO96-5 (DIC310) module («n00», «p55», «t00» etc.), but **differ in the file format**. The module is supplied with the n00 n00 n00 circuit variant with optional support for matrix keyboard and LCD (UNIO port: IO_C). The latest versions, if any, are available via FTP site.

As a counterpart connector it is recommended to use 26-contact 2-row 1 mm pitch socket for ribbon cable: Leotronics 2040-3262.

XP11, XP12, XP13 Headers



[1.10.14] Matrix Keyboard and LCD Port (XP13)

This port shares connector with discrete I/O port. Operation mode is selected by writing to appropriate internal register of XS20 (function of [72:48] port line is set in BIOS Setup after reset of the module).

A 4x4 matrix keyboard (e.g. FK-3) or 4x5 matrix keyboard can be directly connected to XP13 header. A matrix keyboard can be operated only if the driver is running.

Binary representation of the row number code allows to read simultaneous pressing of two and more keys in a row.

Important note:

When using XP13 header for connection of a matrix keyboard or LCD it is necessary to close X22 [1-2] jumper (see Jumper Settings section (*TBA*)).

LCD port allows direct connection of text or graphic displays with HD68130, HD44780, SED1330, T6963 controllers or other hardware compatible with this port displays (see XP13 Connector Pinout table and Pinouts of Cables for connection of typical indicator displays in Appendix A). Contrast is adjusted with R67 potentiometer within the ranges –7…+5 V or 0…+5 V depending on X38 jumper setting; adjustment signals are routed to XP16 connector. LCD backlight LEDs (up to 200 mA) are connected to XP15 header.

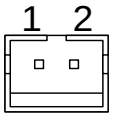
As a conterpart for XP13 connector it is recommended to use 26-contact 2-row 1 mm pitch socket for ribbon cable: Leotronics 2040-3262.

For connection of FK-3 matrix keyboard (16-key dust and moisture protected keyboard, Fastwel) it is recommended to use BLS-8 socket for ribbon cable.

For connection of LCD it is recommended to use BLD-16 or BLD-20 sockets for ribbon cable depending on display model.

To make a cable for connection to XP15 and XP16 headers use JST PHR-2 socket with JST SPH-002T-P0.5S contacts.

XP15, XP16 Contacts



[1.10.16] Analog Input/Output Port (XP19)

CPC109 controller module has isolated input/output port (XP19 connector) with 500V isolation from system; it allows to measure signals at 8 analog inputs with high input resistance (200 kohm) with 12-bit resolution within 0..5 V, 0..10 V, ±5 V, ±10 V, ±20 mA, 0..20 mA ranges.

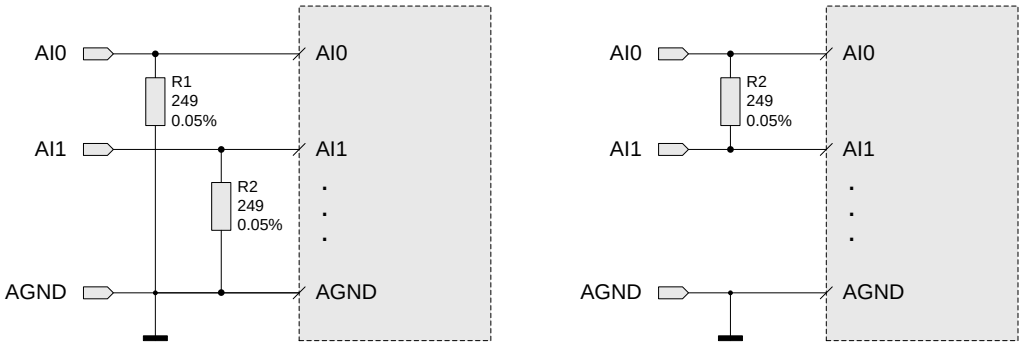
Voltage measurement ranges are selected by software for any channel by direct unsigned code for unipolar or twos complement code for bipolar ranges. For current measurement it is necessary to set appropriate switches (see Jumper Settings section (TBA)).

Voltage and current measurement is possible both in single-wire and two-wire pseudodifferential modes

In two-wire voltage measurement mode the voltage values are read at two channels and the resulting value is obtained as a result of subtraction of the two initial values. For example, if the "-4.5 V" value is obtained from one channel (differential input “+”) and "-3.2 V" value is obtained from another channel (differential input “-”), then the resulting value is "1.3 V". Connection type for each of the two channels (“+” and “-”) in this mode is unconditional. The voltage at each channel must not exceed ±10V relative to common wire (AGND signal).

For current measurement in two-wire mode it is necessary to use only adjacent channels (AI0 and AI1, AI2 and AI3, AI4 and AI5, AI6 and AI7). It is also necessary to properly set jumpers; settings for single- and two-wire modes differ. For current measurement in two-wire mode the shunting resistor (249 ohm, 0.05 %, 0.25 W) is connected between adjacent channels.

Single-Wire and Two-Wire Current Measurement Modes



CPC109 also allows to output two analog signals with 12-bit resolution in the ranges 0..5 V, 0..10 V, and ±5 V (direct unsigned code for unipolar or twos complement code for bipolar ranges; the code format and the ranges are set with jumpers – see Analog Outputs Voltage Ranges Selection section TBA).

Main specifications of analog inputs and outputs can be found in Specifications section of this document.

Declared voltage and current measurement accuracy of the ADC and voltage generation accuracy of the DAC is guaranteed only if the correcting coefficients written to FRAM during metrological tests of the module are used. The value of voltage/current at ADC input, and the value of voltage at DAC output taking into account correcting coefficients are calculated using the following formula:

U = A*X+B,

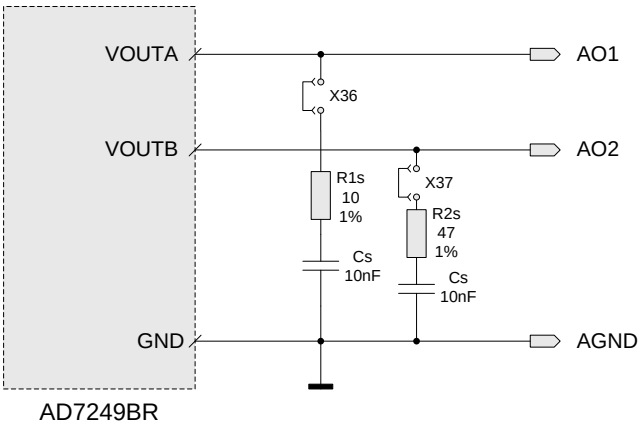
where X – voltage value,

A and B – correcting coefficients stored in FRAM.

The correcting coefficients reading procedure is described in “SOC Vortex86-DX BIOS interface for reading the ADC and DAC correcting coefficients, serial number, and MAC address” section (TBA)

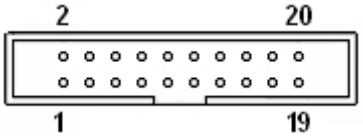
It is possible to connect snubber circuits (10 ohm, 10 nF) to analog output channels (see Jumper Settings section (TBA)). This is necessary when operating with capacitive load.

Connection of Snubber Circuits to Analog Outputs



Recommended counterpart connector – 20-contact 1 mm pitch socket (Leotronics 2040-3202 or IDC2-20).

XP19 Connector



[2.1] Specifications

Power	
Power voltages "-12 V" is used only for extended temperature range displays.	+5 V ± 5%; -12 V
Consumption current for +5 V (wo external devices), max:	
CPC10901	900 mA
CPC10902	700 mA
CPC10903	600 mA
Max allowed consumption current for external circuits; typical value for +25°C (limited by built-in self-resettable fuses):	
+5V_EXTP (XP5: LPT port)	750 mA
+5V_EXTR (XP6, XP7: COM3/COM4 ports)	750 mA
+5V_EXTK (XP8: PS/2 Kbd/Ms port)	750 mA
+5V_EXTA (XP11: Discrete I/O port)	750 mA
+5V_EXTB (XP12: Discrete I/O port)	750 mA
+5V_EXTC (XP13: Discrete I/O port)	750 mA
+5V_EXTL (XP14: PC-buzzer port; XP15: LCD port)	750 mA
Max allowed total consumption current for external and internal circuits; typical value for +25°C (limited by built-in self-resettable fuse)	3 A

Analog Inputs	
ADC chip	MAX1270A
Number of channels	8
Resolution	12 bit
Input resistance of a channel in voltage measurement mode (R_{IN})	200 kohm
Shunt resistor for current measurement (R_{SHUNT})	249 ohm ± 0.05% (0.25 W)
Measurement ranges	± 5 V, ± 10 V (two's complement code)
	0…5 V, 0…10 V (binary code)
	± 20 mA (two's complement code)
	0…20 mA (binary code)
Inputs overvoltage protection	±16.5 V
Conversion time for any analog input with averaging for N. N = 1, 4, 8, 16	12.5 μs * N
Isolation from system	500 V

Analog-to-Digital Conversion Specifications

Measurement range	ADC code	LSB unit weight	Max permissible basic reduced error, %	
			Normal conditions	Operating temperature range
0 … 5 V	0 … 4095	1.221 mV	±0.1	±0.15
-5 … +5 V	-2047 … 2047	2.442 mV	±0.1	±0.15
0 … +10 V	0 … 4095	2.442 mV	±0.1	±0.15
-10 … +10 V	-2047 … 2047	4.884 mV	±0.1	±0.15
0 … 20 mA	0 … 4075	4.908 μA	±0.1	±0.15
-20 … +20 mA	-2037 … 2037	9.817 μA	±0.1	±0.15

Analog Outputs	
DAC chip	AD7249B
Number of channels	2
Resolution	12 bit
Output ranges	±5 V; 0..10 V; 0..5 V (code write format is set with X32 jumper)
Output load	2 kohm max
Conversion time for any analog output	10 μs max
Isolation from system	500 V

Digital-to-Analog Conversion Specifications

Conversion range	DAC code	LSB unit weight	Max permissible basic reduced error, %	
			Normal conditions	Operating temperature range
0 … 5 V	0 … 4095	1.221 mV	± 0.1	± 0.15
0 … +10 V	0 … 4095	2.442 mV	± 0.1	± 0.15
-5 … +5 V	0 … 4095	2.442 mV	± 0.1	± 0.15

Discrete Inputs/Outputs (Electric specifications of discrete input/output channels are defined by FPGA chip - XILINX XCS20-3TQ144I)	
Logic «0» input voltage	0.8 V max
Logic «1» input voltage	2.0 V min
Logic «0» output voltage (at 12 mA)	0.4 V max
Logic «1» output voltage (at 1 mA)	4.5 V min
Logic «1» output voltage (at 4 mA)	2.4 V min
Logic «0» / Logic «1» output capacity (TTL-levels)	12.0 / 4.0 mA

Serial Ports	
Max exchange rate in RS-232 mode	250 Kbit/s
Max exchange rate in RS-422/485 mode	750 Kbit/s (Exchange rate via serial ports is defined by a value in frequency divider register)
Isolation of COM-ports (RS-422/485) from system	500 V
ESD protection	15 kV (IEC1000-4-2)

USB, Ethernet Ports	
USB ports type	USB Host
USB devices type	1.1, 2.0
Ethernet channel exchange rate	10 / 100 Mbit/s
Ethernet activity LEDs	Green LED – activity Yellow LED – operation mode (full/half duplex)
Ethernet port isolation	500 V

IDE Port	
Built-in FFD size	1 GB
Compact Flash cards support	Type I/II
Supported IDE modes	Up to Ultra-DMA 100
Number of IDE devices	Up to 2

Built-in Temperature Sensor	
Temperature masurement range	-55...+125°C (twos complement code with sign)
Sensor type	LM92CIM (National Semiconductor)
Typical absolute temperature measurement error	± 0.5°C (+10...+50°C) ± 1.0°C (-10...+85°C) ± 2.0°C (-40...+85°C)
Resolution	12 bit + sign
LSB unit weight	0.0625°C
Conversion time	Up to 1000 ms

Environmental Conditions	
Operating temperature range	-40...+85°C
Storage temperature	Storage conditions “1” according to GOST 15150-69
Humidity	95% at +25°C noncondensing

Mechanical Conditions	
Vibration stability	5 g (амплитуда ускорения)
Single shock stability	100 g (пиковое ускорение)
Multiple shock stability	50 g (пиковое ускорение)
Dimensions (max)	124.5 × 122.7 × 25.4 mm
Weight (max)	0.140 kg
MTBF (min) *The value is calculated according to: Telcordia Issue 1 model, Method I Case 3, for continuous operation at a surface location, at normal environmental conditions and at ambient temperature 30°C.*	140 000 hours

[2.4] Input/Output Address Space

Address	Function	Note
0000h – 001Fh	8237 DMA Controller #1	–
0020h – 0021h	8259 Master Interrupt Controller	–
0022h – 0023h	Indirect Access	WDT0
0024h – 002Dh	ISA bus	External bus access
002Eh – 002Fh	Reserved	N/A
0030h – 003Fh	ISA bus	External bus access
0040h – 0043h	8253 Programmable Timer	–
0044h – 0047h	ISA bus	External bus access
0048h – 004Bh	Reserved	N/A
004Eh – 005Fh	ISA bus	External bus access
0060h – 0064h	8042 Keyboard Controller	–
0065h	WDT0	–
0066h	ISA bus	External bus access
0067h – 006Dh	WDT1	–
006Eh – 006Fh	ISA bus	External bus access
0070h – 007Fh	RTC, NMI Mask Register	–
0080h – 009Fh	DMA Page Registers	–
00A0h – 00B1h	8259 Slave Interrupt Controller	–
00B2h – 00BFh	ISA bus	External bus access
00C0h – 00DFh	8237 DMA Controller #2	–
00E0h – 01EFh	ISA bus	External bus access
01F0h – 01F8h	Primary IDE Controller	–
01F9h – 0277h	ISA bus	External bus access
0278h – 027Fh	LPT port	(Possible assignment)
0280h – 028Fh	Internal control registers	Matrix keyboard, LEDs, analog I/O, internal control registers ports (XCS05 FPGA)
0290h – 029Fh 02A0h – 02AFh 02B0h – 02BFh	UNIO	UNIO discrete I/O ports (XCS20 FPGA)
02C0h – 02E7h	ISA bus	External bus access
02E8h – 02EFh	COM2	(Possible assignment)
02F0h – 02F7h	ISA bus	External bus access
02F8h – 02FFh	COM4	(Possible assignment)
0300h – 0377h	ISA bus	External bus access

Address	Function	Note
0378h – 037Fh	LPT port	(Possible assignment)
0380h – 03AFh	ISA bus	External bus access
03B0h – 03BBh	MDA Adapter	(Possible assignment)
03BCh – 03BFh	LPT port	(Possible assignment)
03C0h – 03CFh	EGA, VGA Adapter	(Possible assignment)
03D0h – 03DFh	CGA Adapter	(Possible assignment)
03E0h – 03E7h	ISA bus	External bus access
03E8h – 03EFh	COM1	(Possible assignment)
03F0h – 03F7h	Floppy Controller #1	(Possible assignment)
03F8h – 03FFh	COM3	(Possible assignment)
0400h – 04CFh	ISA bus	External bus access
04D0h – 04D1h	Reserved	N/A
04D2h – 0777h	ISA bus	External bus access
0778h – 077Fh	Reserved	N/A
0780h – 0CF7h	ISA bus	External bus access
0CF8h – 0CFFh	Host PCI controller configuration registers	–
0D00h – EDFFh	ISA bus	External bus access
EE00h – EF3Fh	Reserved	N/A
EF40h – FBFFh	ISA bus	External bus access
FC00h – FC0Dh	Reserved	N/A
FC0Eh – FFEFh	ISA bus	External bus access
FFF0h – FFFFh	Reserved	N/A

Internal Input / Output Addresses

Address	Port	Note
BA+00h	BA	See Base Address Control Register section. Setting base address (BA) for internal FPGA registers **(default: BA=0280h)**
BA+01h	LEDs control port	LEDs programmed control
BA+02h BA+03h	LCD control ports	
BA+04h	Matrix keyboard port	Support for 4x4 or 4x5 matrix keyboards
	UNIO IO [71:48] port control	Permission to use UNIO IO [71:48] port for matrix keyboard or LCD
BA+05h	Interrupt source control port, NMI / IRQ	Interrupt control port at NMI / IRQ line of the processor (external WDT, Power Fail, SYSTEM EVENT, ISA$IOCHK#)
BA+06h BA+07h	IRQ7, 11, 12, 15 interrupts control ISA control port	IRQ7, 11, 12, 15 interrupts control port of the processor. Sets source for interrupt lines (XCS20, ISA$IRQx, ADC/DAC Ready, SYSTEM EVENT, MXKEY). Enable / disable ISA bus buffers.
BA+08h – BA+0Bh	ADC / DAC ports	Sets channel number, measurement range, represents ADC measurement result. Sets number and output value of DAC.
BA+0Ch BA+0Dh	Digital potentiometer and built-in temperature sensor ports	Set output value of digital potentiometer, represents the measured temperature value.
BA+0Eh BA+0Fh	Identifier of XCS05 chip	Codes from “p100” to “p255”
BA+10h – BA+1Fh	UNIO ports	IO_A [23:0] discrete input/output channels of CPC109 UNIO port
BA+20h – BA+2Fh	UNIO ports	IO_B [23:0] discrete input/output channels of CPC109 UNIO port
BA+30h – BA+3Fh	UNIO ports	IO_C [23:0] discrete input/output channels of CPC109 UNIO port

[2.8] Internal Registers

[2.8.1] Base Address Control Register

Allows to set base address (BA) for internal registers.

Address	Action	Bits							
		7	6	5	4	3	2	1	0
BA+00h	Write	-	-	BA9	BA8	BA7	BA6	-	-
BA+00h	Read	*0*	*0*	BA9	BA8	BA7	BA6	*0*	*0*

BA[9:6] Allows to set BA of internal control registers or address segment in IO area, where these registers will be available to the system. On the coincidence of ISA_SA[9:6] bus address bits and BA[9:6] bits within read/write cycles in IO area, the internal registers will be addressed.
Default setting (after power-on or hardware reset) – BA = 0280h.
For example, to set *BA=0300h* it is necessary to write *30h* to the port.
Bits 5 and 4 of the BA are always written as '0'.

[2.8.2] LEDs Register

Allows controlling two LEDs and reading their current state.

Address	Action	Bits							
		7	6	5	4	3	2	1	0
BA+01h	Write	-	-	-	-	-	-	LEDR	LEDG
BA+01h	Read	-	-	-	-	-	-	SLEDR	SLEDG

LEDG Green LED control. Writing '1' switches on, writing '0' switches off the green LED.
LEDR Red LED control. Writing '1' switches on, writing '0' switches off the red LED
SLEDG Green LED status. '1' – “on”, '0' – “off” (default).
SLEDR Red LED status. '1' – “on”, '0' – “off” (default).

[2.8.3] LCD Control Register

Includes two byte registers: data register (**BA+02h**) and control signals register (**BA+03h**). The port is controlled with the help of drivers.

Address	Action	Bits							
		7	6	5	4	3	2	1	0
BA+02h	**Write**	DLC[7:0]							
BA+03h	**Write**	-CS	-	RS	E	-	-	-	-

DLC[7:0] LCD data.

-CS, RS, E LCD control signals.

[2.8.4] Matrix Keyboard Control/Status Register

The register is used to read the status of a matrix keyboard. Keyboard is controlled with the help of driver. The register represents the status of a matrix keyboard (5×4 or 4×4). The port is written automatically on a change of a keyboard status (pressing or releasing of a button); write is blocked until reading of data from **BA+04h** port.

The port is also used to enable interrupt from a matrix keyboard, to enable use of IO_C(23:0) port for LCD/matrix keyboard control, or as an additional discrete IO port.

Address	Action	Bits							
		7	6	5	4	3	2	1	0
BA+04h	Read	-	ROW[2:0]			COL[3:0]			
BA+04h	Write							IMKE	UCE

COL[3:0] Column code (from binary "0000" to "1111"), where a button is pressed. Pressing of a button (or several buttons from different columns) induces writing '1' to relevant bits of the code. If no one button is pressed, the code is "0000".

ROW[2:0] Row code (from 1 to 5), where a button is pressed or released.

IMKE Enable interrupt from a matrix keyboard. Writing '1' to this bit enables interrupt from a matrix keyboard on the status change (key pressed/released), writing '0' – disabled (default).

UCE Enables/disables using IO_C(23:0) port as a configurable discrete IO port (UNIO). To control a matrix keyboard and LCD this bit is set to '0' (default). For using IO_C(23:0) port as a configurable discrete IO port this bit is set to '1'.

Attention!

For generation of interrupts from a matrix keyboard the bit UCE should be set to '0'. In case the bit UCE is set to '1', configurable discrete IO port is used as a source in interrupt generation.

[2.8.5] System Interrupts Control/Status Port

The port enables/disables using external signals in NMI interrupt generation and "SYSTEM EVENT" signal on writing to the port. Interrupts generation is based on "OR" principle. The port also allows to define a hardware source for NMI and "SYSTEM EVENT".

Address	Action	Bits							
		7	6	5	4	3	2	1	0
BA+05h	Write	IOCHK_EN	PFO_EN	WDO_EN	EXT_EN	-	-	SE_NMI_EN	NMI_EN
BA+05h	Read	IOCHK	PFO	WDO	EXT	-	-	SE_NMI_EN	NMI_EN

IOCHK_EN 'ISA_IOCHK#' to NMI. Enable – '1', disable – '0'.

PFO_EN 'Power Fail' to NMI. Enable – '1', disable – '0'.

WDO_EN 'WatchDog Timeout' to NMI. Enable – '1', disable – '0'.

EXT_EN 'RMTRES' to NMI. Enable – '1', disable – '0'.

SE_NMI_EN 'SYSTEM EVENT' to NMI. Enable – '1', disable – '0'.

NMI_EN Enable NMI. NMI generation on event at 'ISA_IOCHK#' or "SYSTEM EVENT" – enabled, if set to '1'; disabled, if set to '0' (meanwhile 'Z'-state at hardware NMI line).

IOCHK 'ISA_IOCHK#' flag - '1': active level of 'ISA_IOCHK#' signal.

PFO 'POWER FAIL' flag - '1': input power voltage "+5V" is below 4.7 V.

WDO 'WATCHDOG Timeout' flag - '1': timeout of the built in the supervisor watchdog timer (WDT2).

EXT 'RMTRES' flag - '1': external interrupt event flag (XP16-XP17).

Attention!

After each interrupt generation on events at "ISA_IOCHK#', 'POWER FAIL', 'WATCHDOG Timeout', 'RMTRES' it is necessary to reset the relevant interrupt flag by consequntly writing '0' and '1' to the appropriate interrupt enable bit. Otherwise, further interrupt generation from this port is not possible.

For example, after the interrupt generation on 'RMTRES' event, it is necessary to reset the flag 'EXT_EN' by writing '0' in it, and then set it to '1' in interrupt handler.

[2.8.6] Interrupts Control/Status Registers

The port sets the interrupt source for IRQ7, IRQ11, IRQ12, IRQ15 lines of the processor. It is possible to set independently for each line ISA bus interrupts (IRQ7, IRQ11, IRQ12, IRQ15) or interrupts from a matrix keyboard, UNIO ports, Ready signals of ADC and DAC, external interrupt source, Power Fail and watchdog timer signals. This port is also used to switch on/off the buffer elements of ISA bus.

Address	Action	Bits							
		7	6	5	4	3	2	1	0
BA+06h	Write/Read	i15SEL[1:0]		i12SEL[1:0]		i11SEL[1:0]		i7SEL[1:0]	
BA+07h	Write	IUA	IUE	IUC	IAE	IOC_EN	IOB_EN	IOA_EN	ISAE
BA+07h	Read	IUA	IUE	IUC	AIO_ST	IOC_ST	IOB_ST	IOA_ST	ISAE

i7SEL[1:0] IRQ7 selector code. Options: 'Z' – state (b'00, default); UNIO (b'01); "SYSTEM EVENT" (b'10); ISA$IRQ7 (b'11).

i11SEL[1:0] IRQ11 selector code. Options: 'Z' – state (b'0, default) ; UNIO (b'01); ADC/DAC Ready (b'10); ISA$IRQ11 (b'11).

i12SEL[1:0] IRQ12 selector code. Options: 'Z' – state (b'00, default); {MXKEY или IO_C} (b'01); ADC/DAC Ready (b'10); ISA$IRQ12 (b'11).

i15SEL[1:0] IRQ15 selector code. Options: 'Z' – state (b'00, default); UNIO (b'01); "SYSTEM EVENT" (b'10); ISA$IRQ15 (b'11).

IUA UNIO port interrupts combination. '1' – interrupts from IO_A[23:0], IO_B[23:0] channels are “AND” combined, '0' – “OR” (default). The “AND” combination is possible only if all interrupt enable bits from all UNIO ports (IOC_EN, IOB_EN, IOA_EN) are set.

IUE Enable interrupt from UNIO port. '1' –general UNIO port interrupt enabled, '0' – disabled.

IUC Enable participation of interrupt from IO_C (or MXKEY) port in general UNIO interrupt. '1' – interrupt from IO_C port / matrix keyboard (depending on the state of 'UCE' bit of MXKEY control port) participates in generation of general UNIO interrupt, '0' – does not participate.

IAE Enable interrupt on "ADC/DAC Ready". '1' – enabled, '0' – disabled. Setting this bit to '0' also resets the state of AIO_ST flag.

IOC_EN Enable interrupt from UNIO IO_C port - '1' (XP13). '1' – interrupt from IO_C port or matrix keyboard enabled, '0' – disabled. Setting this bit to '0' also resets the state of IOC_ST flag.

IOB_EN Enable interrupt from UNIO IO_B port - '1' (XP12). '1' – interrupt from IO_B port enabled, '0' – disabled. Setting this bit to '0' also resets the state of IOB_ST flag.

IOA_EN Enable interrupt from UNIO IO_A port - '1' (XP11). '1' – '1' – interrupt from IO_A port enabled, '0' – disabled. Setting this bit to '0' also resets the state of IOA_ST flag.

ISAE	ISA bus buffer elements control. '0': disabled (outputs in 'Z'-state – default after power-on or reset). '1': ISA bus buffer elements enabled.
AIO_ST	Interrupt on "ADC/DAC Ready" flag.
IOC_ST	Interrupt from UNIO IO_C port / matrix keyboard flag - '1' (XP13).
IOB_ST	Interrupt from UNIO IO_B port flag - '1' (XP12).
IOA_ST	Interrupt from UNIO IO_A port flag - '1' (XP11).

Depending on the 'UCE' bit ('BA+04h' port) state, the bit 'IOC_ST' represents the fact of interrupt generation from UNIO IO_C port or from a matrix keyboard.

Attention!

After each interrupt generation from UNIO ports, from analog IO port it is necessary to reset the relevant interrupt flag by consequntly writing '0' and '1' to the appropriate interrupt enable bit. Otherwise, further interrupt generation from this port is not possible.

For example, after the interrupt generation from IO_A port it is necessary to reset the flag 'IOA_EN' by writing '0' in it, and then set it to '1' in interrupt handler.

Attention!

To prevent false interrupt generation right after enabling interrupt generation from UNIO ports, it is necessary to configure interrupts at first and then to set the bit enabling interrupt from UNIO port ('IOA_EN', 'IOB_EN' or 'IOC_EN') in Interrupt Control Register.

[2.8.7] ADC/DAC Control Register

The port is used for current and voltage measurement at eight analog inputs and for voltage forming at two analog outputs. The port has control register (**BA+08h**) for setting the number of a channel for measurement, for setting the measurement range and averaging code, ADC data register (**BA+08h, BA+09h**, IOCS16 is not formed during reading), DAC data register (**BA+0Ah, BA+0Bh**, IOCS16 is not formed when writing). Analog-to-digital conversion is started immediately after write to control register, digital-to-analog conversion is started after write to 16-bit DAC data register (writing only to the lower byte of the register is not allowed)

Address	Action	Bits							
		7	6	5	4	3	2	1	0
BA+08h	Write	-	SEL[2:0]			RNG[1:0]		AV[1:0]	
BA+08h	Read	ADC[7:0]							
BA+09h	Read	ADC11				ADC[11:8]			
BA+0Ah	Read	ADCR	DACR	-	-	-	-	-	-
BA+0Ah	Write	DAC[7:0]							
BA+0Bh	Write	-	-	-	CH	DAC[11:8]			

AV[1:0] ADC sample averaging code. This field can be used, if ADC sample filtering is needed (hardware averaging for 4, 8, or 16 samples).
AV[1:0] = b'00 – no averaging; AV[1:0] = b'01 – averaging for 4 samples;
AV[1:0] = b'10 – averaging for 8; AV[1:0] = b'11 – averaging for 16.

RNG[1:0] ADC measurement range code for the input set by SEL[2:0] code. 0..+5V – binary code b'00; ±5V – b'01; 0..+10V – b'10; ±10V – b'11.

SEL[2:0] ADC input code (binary code from b'000 to b'111). Sets the number of an input for measurement.

ADC[11:0] ADC data. Twos complement code for the result of A2D conversion for bipolar ranges; direct binary code for unipolar ranges.

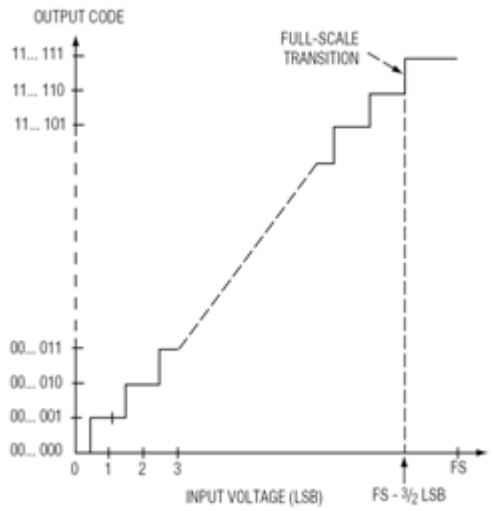
ADCR ADC ready flag. Reflects availability of A2D conversion result.
'1' – ready, '0' – conversion in progress.

DACR DAC ready flag. Reflects availability of D2A conversion result.
'1' – ready, '0' – conversion in progress.

DAC[11:0] DAC data. D2A data code for the output set in CH bit. Direct signless binary code for all ranges (0…FFFh).

CH DAC output. The number of analog output: '0' – AO0 output, '1' – AO1 output.

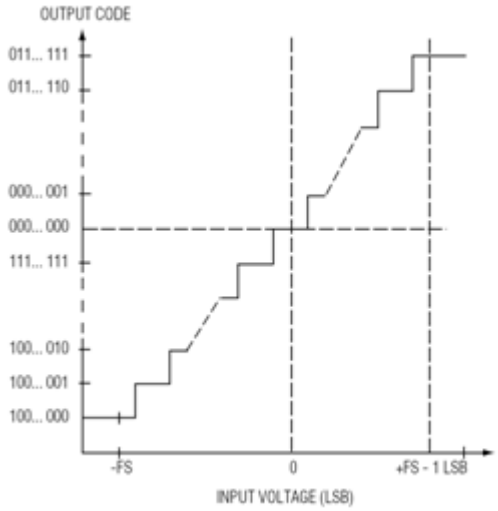
ADC / DAC Transfer Function



ADC/DAC transfer function
for unipolar voltage measurement ranges

1 LSB = FS / 4095 – voltage measurement

1 LSB = FS / 4075 – current measurement



ADC/DAC transfer function
for bipolar voltage measurement ranges

1 LSB = (2·|FS|) / 4095 – voltage measurement

1 LSB = (2·|FS|) / 4075 – current measurement

LSB – LSB weight for ADC data code;

FS – Numerical value of the upper range limit (volts):

«5» for 0…5V and -5…+5V ranges;

«10» for 0…10V and -10…+10V ranges;

«20» for 0…20 mA and -20…20 mA ranges.

OUTPUT CODE – 12-bit ADC / DAC data code.

Important!

When measuring the current it is necessary to take into account the input resistance of the channel (see Technical Specifications section).

$$I = U_{ADC} / (R_{shunt} \,||\, R_{in})$$

For current measurement within 0…20 mA range it is necessary to set the ADC measurement range binary code: RNG[1:0] = b'00, for the range ±20 mA – b'01 binary code.

[2.8.8] XCS05 and XCS20 Circuit Version Code Registers

XCS05 and XCS20 circuit version codes are available for read via BA+0Eh and BA+0Fh byte ports.

Address	Action	Bits							
		7	6	5	4	3	2	1	0
BA+0Eh	Read	Ver_05				Rev_05			
BA+0Fh	Read	Ver_20				Rev_20			

Ver_05 – numeric code of the XCS05 circuit version;
Rev_05 – numeric code of the XCS05 circuit revision;
Ver_20 – numeric code of the XCS20 circuit version;
Rev_20 – numeric code of the XCS20 circuit revision.

[2.8.9] Discrete Input/Output UNIO Ports Registers

Used to control 72 discrete input/output channels.

The channels are divided into 3 groups:

- IO_A[23:0] channels
  (similar to FPGA1 in UNIO96-5 module, excluding Base Address: **BA1=BA+10h**)
- IO_B[23:0] channels
  (similar to FPGA2 in UNIO96-5 module, excluding Base Address: **BA2=BA+20h**)
- IO_C[23:0] channels
  (similar to FPGA3 in UNIO96-5 module, excluding Base Address: **BA3=BA+30h**)
  For operation of the port it is necessary to disable LCD and matrix keyboard. Interrupt from this port shares the line with the matrix keyboard port. Interrupt from this port is enabled by setting the 'UCE' interrupt control port bit to '1'.

The assignment of input/output ports' internal registers with BA1, BA2, BA3 base addresses is similar to UNIO96-5 ports.

[2.8.10] UNIO Ports Circuit Codes Identification

Each UNIO port has its own identificator matching the circuit code, for example n00, t00, p55 etc. The identificator can be read via byte ports with BAx+0Eh, BAx+0Fh, where BAx – base address of a UNIO port within CPC109.

Address	Action	Bits							
		7	6	5	4	3	2	1	0
BAx+0Eh	**Read**	***a ... z***							
BAx+0Fh	**Read**	***SN[7:0]***							

a...z ASCII-code of lowercase letters from a to z.

SN[7:0] Circuit number code, from 0 to 255.

[2.9] Pinouts of Connectors

Symbol “#” in signal name – logic «0» active level.

[2.9.5] XP11 Connector Pinout: UNIO IO_A(23:0) Port

XP11: IDC26, 2 mm (Leotronics, 2073-3262)				
Pin #	**Signal**		**Pin #**	**Signal**
1	IO_A(12)		2	+5V_EXTA
3	IO_A(13)		4	IO_A(10)
5	IO_A(14)		6	IO_A(11)
7	IO_A(15)		8	IO_A(9)
9	IO_A(23)		10	IO_A(8)
11	IO_A(21)		12	IO_A(22)
13	IO_A(16)		14	IO_A(20)
15	IO_A(18)		16	IO_A(17)
17	IO_A(19)		18	IO_A(7)
19	IO_A(0)		20	IO_A(6)
21	IO_A(1)		22	IO_A(5)
23	IO_A(2)		24	IO_A(4)
25	IO_A(3)		26	GND

[2.9.6] XP12 Connector Pinout: UNIO IO_B(23:0) Port

XP12: IDC26, 2 mm (Leotronics, 2073-3262)				
Pin #	**Signal**		**Pin #**	**Signal**
1	IO_B(12)		2	+5V_EXTB
3	IO_B(13)		4	IO_B(10)
5	IO_B(14)		6	IO_B(11)
7	IO_B(15)		8	IO_B(9)
9	IO_B(23)		10	IO_B(8)
11	IO_B(21)		12	IO_B(22)
13	IO_B(16)		14	IO_B(20)
15	IO_B(18)		16	IO_B(17)
17	IO_B(19)		18	IO_B(7)
19	IO_B(0)		20	IO_B(6)
21	IO_B(1)		22	IO_B(5)
23	IO_B(2)		24	IO_B(4)
25	IO_B(3)		26	GND

[2.9.7] XP13 Connector Pinout: UNIO IO_C(23:0) / MXKEY&LCD Port

XP13: IDC26, 2 mm (Leotronics, 2073-3262)								
Pin #	**UNIO**	**MXKEY**	**LCD**		**Pin #**	**UNIO**	**MXKEY**	**LCD**
1	IO_C(12)	–	–		2	+5V_EXTC		
3	IO_C(13)	ROW1 (E)	–		4	IO_C(10)	COL3 (B)	–
5	IO_C(14)	COL2 (C)	–		6	IO_C(11)	ROW2 (F)	–
7	IO_C(15)	ROW3 (G)	–		8	IO_C(9)	COL1 (D)	–
9	IO_C(23)	COL4 (A)	–		10	IO_C(8)	ROW4 (H)	–
11	IO_C(21)	ROW5	–		12	IO_C(22)	–	RS
13	IO_C(16)	–	R/W		14	IO_C(20)	–	E
15	IO_C(18)	–	DLC0		16	IO_C(17)	–	DLC1
17	IO_C(19)	–	DLC2		18	IO_C(7)	–	DLC3
19	IO_C(0)	–	DLC4		20	IO_C(6)	–	DLC5
21	IO_C(1)	–	DLC6		22	IO_C(5)	–	DLC7
23	IO_C(2)	–	-CS		24	IO_C(4)	–	-RESET
25	IO_C(3)	–	–		26	GND		

[2.9.13] XP14, XP15, XP16 Connectors Pinout

XP14: Buzzer

XP14: B 2B-PH-KL (JST), 2 mm	
Pin #	**Signal**
1	+5V_EXTL
2	SPK_DRV

XP15: LCD Power/Backlight

XP15: B 2B-PH-KL (JST), 2 mm	
Pin #	**Signal**
1	LED B/L+ (+5V_EXTL)
2	LED B/L- (GND)

XP16: LCD Contrast

XP16: B 2B-PH-KL (JST), 2 mm	
Pin #	**Signal**
1	Contrast Adj.
2	GND

[2.9.16] XP19 Connector Pinout: Analog Inputs/Outputs

XP19: Isolated Analog Inputs/Outputs

XP19: IDC2-20, 2 mm (BH2-20)			
Pin #	**Signal**	**Pin #**	**Signal**
1	AI0	2	AGND
3	AI1	4	AGND
5	AI2	6	AGND
7	AI3	8	AGND
9	AI4	10	AGND
11	AI5	12	AGND
13	AI6	14	AGND
15	AI7	16	AGND
17	DAC0	18	AGND
19	DAC1	20	AGND

AGND – analog ground, isolation from system: 1000 V.

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