Fastwel

COM Express

CPC1301

Pentium Core (2) Duo / Celeron M Based COM Express Module

User Manual

Rev. 001b E

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CE

The product described in this manual is compliant to all related CE standards.

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001	Initial version	CPC1301	October 2008
001a	Reassertion of data; I^2C Controller and Watchdog Timer sections replaced	CPC1301	April 2009
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Notation Conventions

Warning, ESD Sensitive Device!

This symbol draws your attention to the information related to electro static sensitivity of your product and its components. To keep product safety and operability it is necessary to handle it with care and follow the ESD safety directions.

Warning!

This sign marks warnings about hot surfaces. The surface of the heatsink and some components can get very hot during operation. Take due care when handling, avoid touching hot surfaces!

Caution: Electric Shock!

This symbol warns about danger of electrical shock (> 60 V) when touching products or parts of them. Failure to observe the indicated precautions and directions may expose your life to danger and may lead to damage to your product.

Warning!

Information marked by this symbol is essential for human and equipment safety.
Read this information attentively, be watchful.

Note...

This symbol and title marks important information to be read attentively for your own benefit.

General Safety Precautions

This product was developed for fault-free operation. Its design provides conformance to all related safety requirements. However, the life of this product can be seriously shortened by improper handling and incorrect operation. That is why it is necessary to follow general safety and operational instructions below.

Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.

Warning!

When handling this product, special care must be taken not to hit the heatsink (if installed) against another rigid object. Also, be careful not to drop the product, since this may cause damage to the heatsink, CPU or other sensitive components as well.

Please, keep in mind that any physical damage to this product is not covered under warranty.

Note:

This product is guaranteed to operate within the published temperature ranges and relevant conditions. However, prolonged operation near the maximum temperature is not recommended by Fastwel or by electronic chip manufacturers due to thermal stress related failure mechanisms. These mechanisms are common to all silicon devices; they can reduce the MTBF of the product by increasing the failure probability. Prolonged operation at the lower limits of the temperature ranges has no limitations.

Caution, Electric Shock!

Before installing this product into a system and before installing other devices on it, always ensure that your mains power is switched off.

Always disconnect external power supply cables during all handling and maintenance operations with this module to avoid serious danger of electrical shock.

Unpacking, Inspection and Handling

Please read the manual carefully before unpacking the module or mounting the device into your system. Keep in mind the following:

ESD Sensitive Device!

Electronic modules and their components are sensitive to static electricity. Even a non-perceptible by human being static discharge can be sufficient to destroy or degrade a component's operation! Therefore, all handling operations and inspections of this product must be performed with due care, in order to keep product integrity and operability:

- Preferably, unpack or pack this product only at EOS/ESD safe workplaces. Otherwise, it is important to be electrically discharged before touching the product. This can be done by touching a metal part of your system case with your hand or tool. It is particularly important to observe anti-static precautions when setting jumpers or replacing components.
- If the product contains batteries for RTC or memory back-up, ensure that the module is not placed on conductive surfaces, including anti-static mats or sponges. This can cause short-circuit and result in damage to the battery and other components.
- Store this product in its protective packaging while it is not used for operational purposes.

Unpacking

The product is carefully packed in an antistatic bag and in a carton box to protect it against possible damage and harmful influence during shipping. Unpack the product indoors only at a temperature not less than +15°C and relative humidity not more than 70%. Please note, that if the product was exposed to the temperatures below 0°C for a long time, it is necessary to keep it at normal conditions for at least 24 hours before unpacking. Do not keep the product close to a heat source.

Following ESD precautions, carefully take the product out of the shipping carton box. Proper handling of the product is critical to ensure correct operation and long-term reliability. When unpacking the product, and whenever handling it thereafter, be sure to hold the module preferably by the front panel, card edges or ejector handles. Avoid touching the components and connectors.

Retain all original packaging at least until the warranty period is over. You may need it for shipments or for storage of the product.

Initial Inspection

Although the product is carefully packaged, it is still possible that shipping damages may occur. Careful inspection of the shipping carton can reveal evidence of damage or rough handling. Should you notice that the package is damaged, please notify the shipping service and the manufacturer as soon as possible. Retain the damaged packing material for inspection.

After unpacking the product, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socketed components), contact Fastwel's official distributor from which you have purchased the product for additional instructions. Depending on the severity of the damage, the product may even need to be returned to the factory for repair. DO NOT apply power to the product if it has visible damage. Doing so may cause further, possibly irreparable damage, as well as result in a fire or electric shock hazard.

If the product contains socketed components, they should be inspected to make sure they are seated fully in their sockets.

Handling

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

In order to keep Fastwel's warranty, you must not change or modify this product in any way, other than specifically approved by Fastwel or described in this manual.

Technical characteristics of the systems in which this product is installed, such as operating temperature ranges and power supply parameters, should conform to the requirements stated by this document.

Retain all the original packaging; you will need it to pack the product for shipping in warranty cases or for safe storage. Please, pack the product for transportation in the way it was packed by the supplier.

When handling the product, please, remember that the module, its components and connectors require delicate care. Always keep in mind the ESD sensitivity of the product.

Three Year Warranty

Fastwel Co. Ltd. (Fastwel), warrants that its standard hardware products will be free from defects in materials and workmanship under normal use and service for the currently established warranty period. Fastwel's only responsibility under this warranty is, at its option, to replace or repair any defective component part of such products free of charge.

Fastwel neither assumes nor authorizes any other liability in connection with the sale, installation or use of its products. Fastwel shall have no liability for direct or consequential damages of any kind arising out of sale, delay in delivery, installation, or use of its products.

If a product should fail through Fastwel's fault during the warranty period, it will be repaired free of charge. For out of warranty repairs, the customer will be invoiced for repair charges at current standard labor and materials rates.

Warranty period for Fastwel products is 36 months since the date of purchase.

The warranty set forth above does not extend to and shall not apply to:

1. Products, including software, which have been repaired or altered by other than Fastwel personnel, unless Buyer has properly altered or repaired the products in accordance with procedures previously approved in writing by Fastwel.
2. Products, which have been subject to power supply reversal, misuse, neglect, accident, or improper installation.

Returning a product for repair

1. Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization.
2. Attach a failure inspection report with a product to be returned in the form, accepted by customer, with a description of the failure circumstances and symptoms.
3. Carefully package the product in the antistatic bag in which the product had been supplied. Failure to package in antistatic material will VOID all warranties. Then package the product in a safe container for shipping.
4. The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer.

1 Introduction

This document presents general information on CPC1301 processor module, the details of its proper and safe installation, configuration and operation.

1.1 Overview

CPC1301 is a COM Express Type II CPU module that fully complies with PICMG COM Express standard. It is based on Intel® Core™ 2 Duo/Core Duo/Celeron M CPUs operating at frequencies of up to 1.66 GHz with 533/667 MHz front side bus and on Intel chipset comprising 945GM GMCH and ICH7M DH. Memory interface supports dual or single channel DDR2 SDRAM through two SODIMM sockets with total capacity of up to 4 GB.

CPC1301 is intended for high performance embedded systems, terminals, industrial computers. The module is designed for use with carrier boards conforming to PICMG COM Express Module Base Specification rev.1.0 for CPU modules with pinout Type II, for example with Fastwel KIB1280 ATX-format development carrier board.

Multimedia functions are supported by interfaces for CRT monitor, flat panels with dual LVDS interface and AC'97/HD 5.1 audio. External graphic adapters can be connected through x16 PCI Express interface. S-Video interface is also available.

Gigabit Ethernet channel makes this board perfect for developing communication intensive applications CPC1301 storage subsystem supports two SATA and one IDE UltraATA/100 disk drives.

CPC1301 supports S3 (Suspend to RAM) mode. Additional reliability of CPC1301 is provided by hardware monitoring, watchdog timers, and a set of system monitoring features.

CPC1301 operates in industrial (–40°C to +85°C) or commercial (0°C to +70°C) temperature ranges depending on the version.

Supported operating systems – Microsoft DOS v. 3.30 – 6.22, Fastwel DOS (MS-DOS compatible); Windows 2000, XP, XP Embedded; QNX v. 4.20, 6.0; Linux 2.6.

1.2 CPC1301 Versions

The board is offered in flexible configuration. Options include different processors, the size of supplied system memory, and other options described in this section.

Customer can choose necessary configuration options using the following template:

1	–	2	–	3	–	4	\	5

1 Basic product name:

CPC1301

2 Integral part of the product code (configuration version):

01	ICH7M DH, five x1 PCIe or one x4 and one x1 PCIe

3 Processor:

CD1.66	Core Duo LV L2400, 1.66 GHz, 2 MB L2, 667 MHz FSB
C2D1.5	Core 2 Duo Mobile L7400, 1.5 GHz, 4 MB L2, 667 MHz FSB
CS1.06	Celeron M 423, 1.06 GHz, 1 MB L2, 533 MHz FSB

4 Operating temperature range:

I	Industrial range, -40…+85°C (with CS1.06 only)
C	Commercial range, 0…+70°C

5 Other options:

DDR2 SODIMM memory modules:

Code	Supplied Memory
\SC-SODIMM-DDR2 1024 C	One F-SODIMM-DDR2 1024, 0°C…+70°C
\SC-SODIMM-DDR2 1024 I	One F-SODIMM-DDR2 1024, -40°C…+85°C
\SC-SODIMM-DDR2 2048 C	One F-SODIMM-DDR2 2048, 0°C…+70°C
\SC-SODIMM-DDR2 2048 I	One F-SODIMM-DDR2 2048, -40°C…+85°C
\DC-SODIMM-DDR2 1024 C	Two F-SODIMM-DDR2 512, 0°C…+70°C
\DC-SODIMM-DDR2 1024 I	Two F-SODIMM-DDR2 512, -40°C…+85°C
\DC-SODIMM-DDR2 2048 C	Two F-SODIMM-DDR2 1024, 0°C…+70°C
\DC-SODIMM-DDR2 2048 I	Two F-SODIMM-DDR2 1024, -40°C…+85°C
\DC-SODIMM-DDR2 4096 C	Two F-SODIMM-DDR2 2048, 0°C…+70°C
\DC-SODIMM-DDR2 4096 I	Two F-SODIMM-DDR2 2048, -40°C…+85°C

Heatspreader, heatsink and fan (preliminary information):

Code	Description
\R	Heatspreader (with CS1.06 only)
\R3	Ribbed heatsink, no fan, ribs oriented lengthwise, OSX77
\R3F	Ribbed heatsink, with fan, ribs oriented lengthwise, OSX77
\R4	Ribbed heatsink, no fan, ribs oriented widthwise, OSX77
\R4F	Ribbed heatsink, with fan, ribs oriented widthwise, OSX77
\R5	Ribbed heatsink, no fan, ribs oriented lengthwise, OSX98
\R5F	Ribbed heatsink, with fan, ribs oriented lengthwise, OSX98
\R6	Ribbed heatsink, no fan, ribs oriented widthwise, OSX98
\R6F	Ribbed heatsink, with fan, ribs oriented widthwise, OSX98

Custom configurations are available upon request

Example:

CPC1301 – 01 – CD1.66 – C \SC-SODIMM-DDR2 1024 C \R1

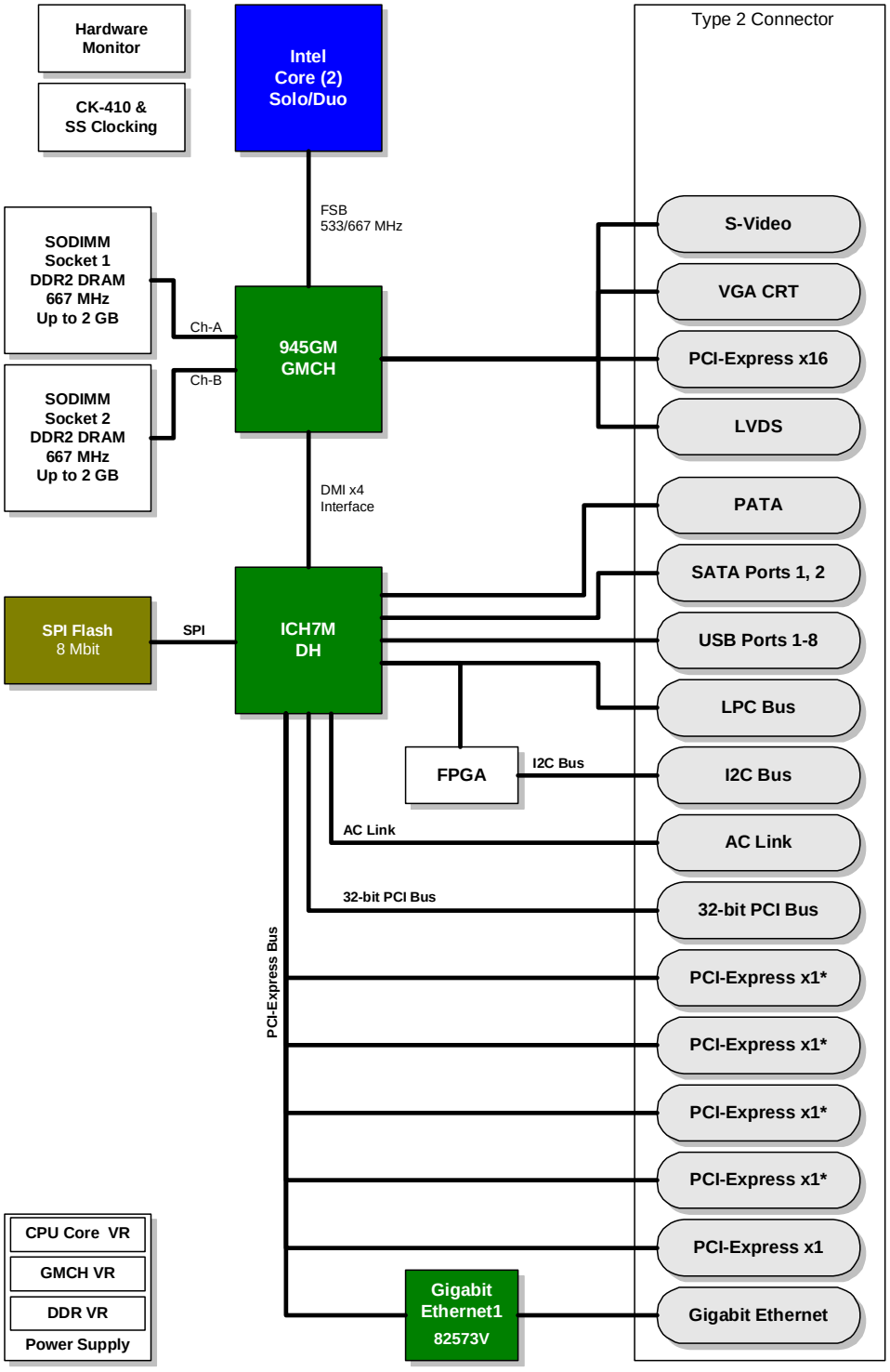
COM Express processor module, Intel® 945GM, SVGA, PCIe x16, LVDS, SATA, Gigabit Ethernet
Core Duo 1.66 GHz, 2 MB cache, 667 MHz FSB
Commercial temperature range, 0…+70°C
One DDR2 SODIMM memory module, 1024 MB, commercial range
Ribbed heatsink, no fan, ribs oriented lengthwise, ThermaFlo

1.3 CPC1301 Diagrams

The diagrams in this section give visual information about the CPC1301 board design, its appearance, connectors and components layout. The diagrams may not reflect insignificant differences between the CPC1301 versions and generations.

1.3.1 Block Diagram

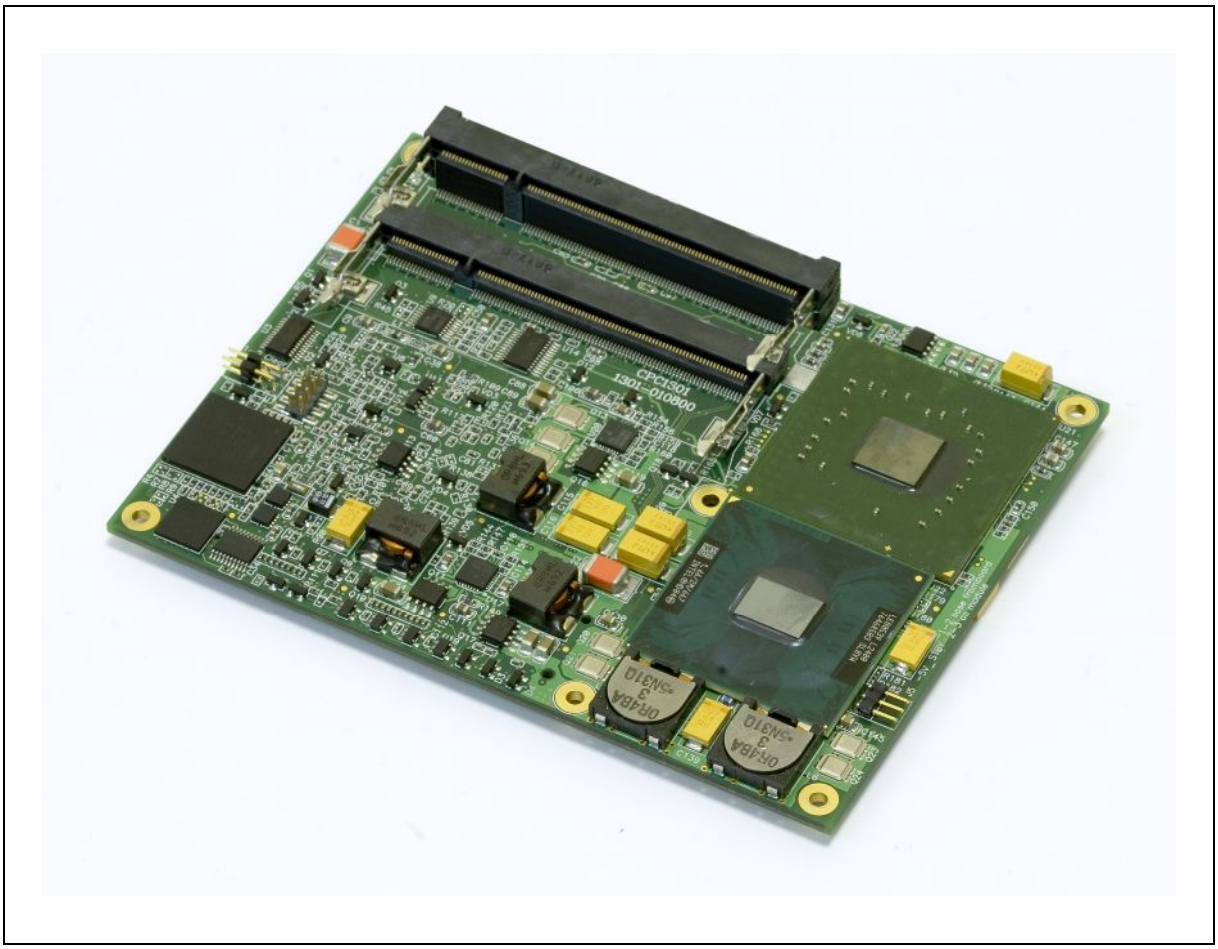
Figure 1-1: CPC1301 Block Diagram



(*) Four x1 PCI Express channels can be aggregated into one x4 channel.

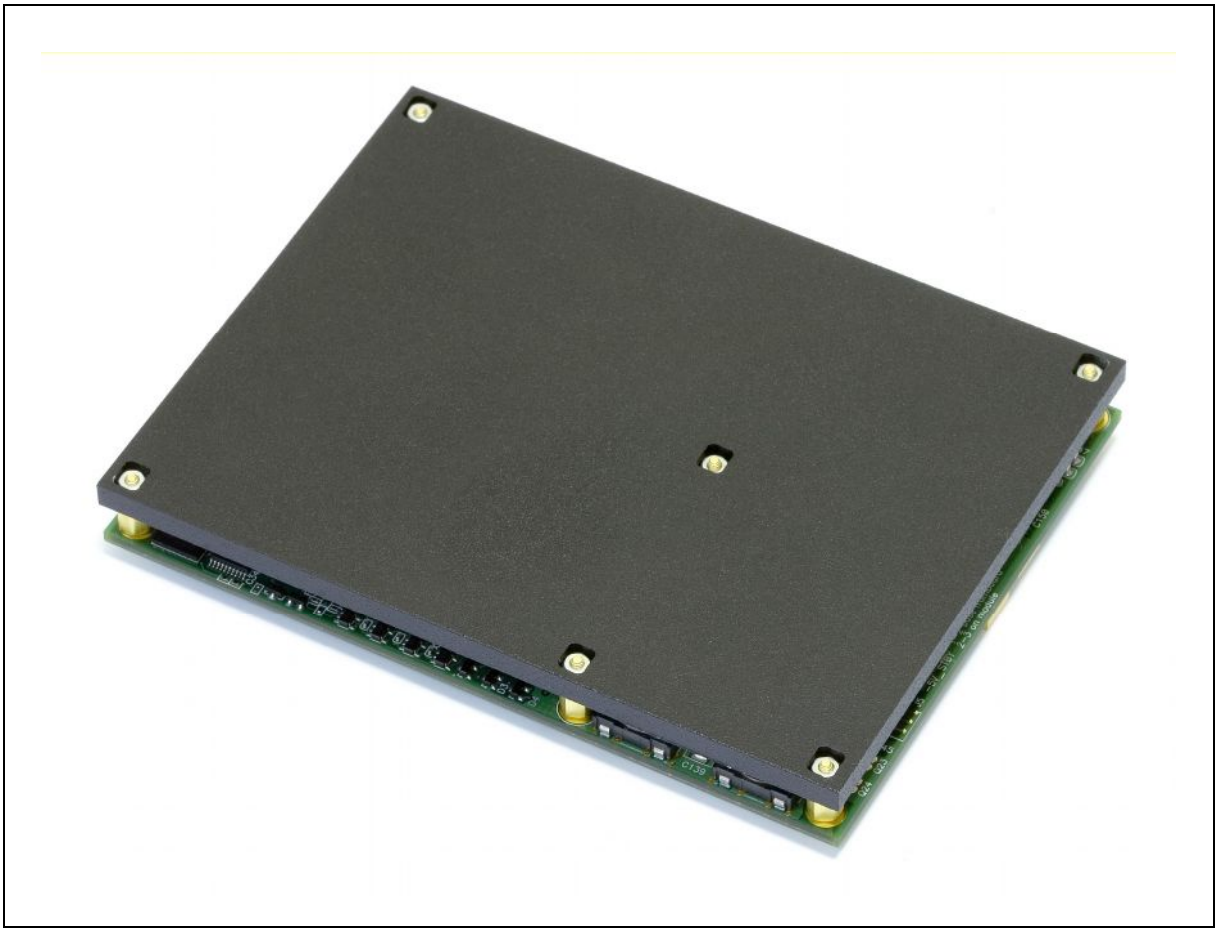
1.3.2 Module Appearance

Figure 1-2: CPC1301 Module Appearance



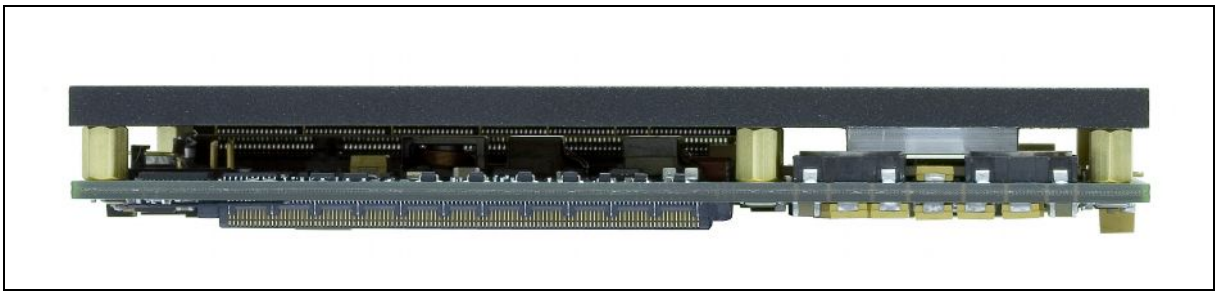
The appearance may vary for different versions of the module.
Heatspreader and memory modules are not shown.

Figure 1-3: CPC1301 Module Appearance with Heatspreader Intalled



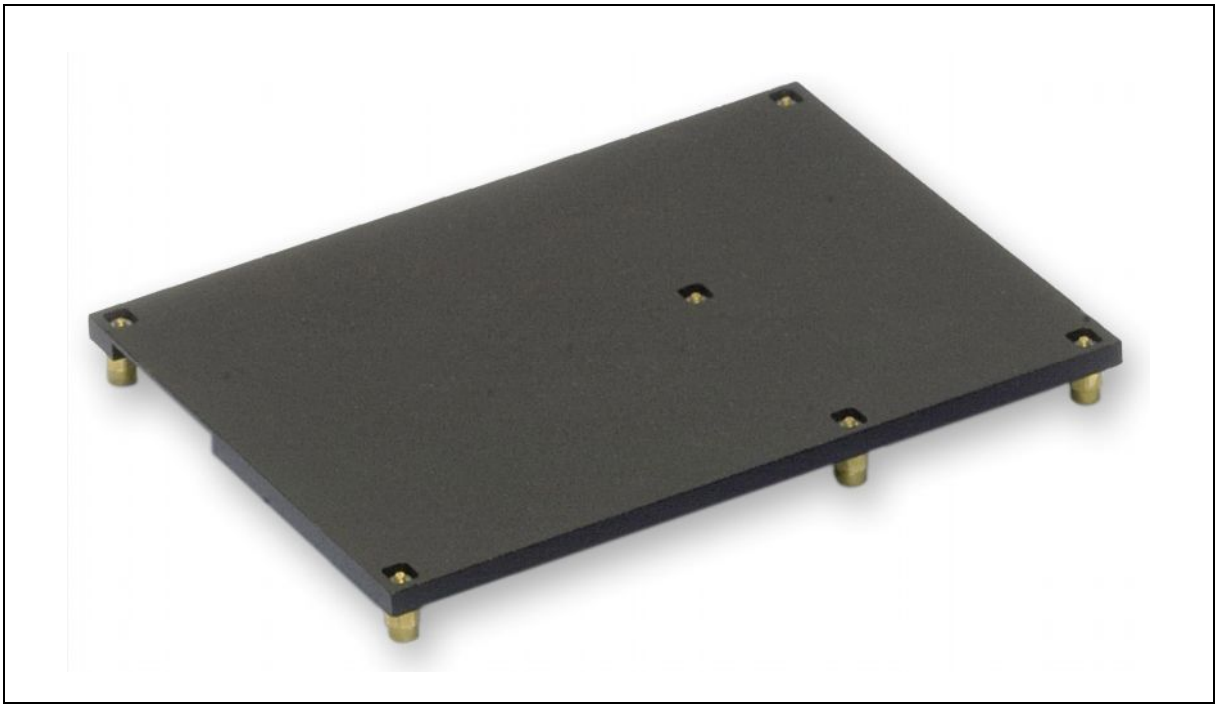
The appearance may vary for different versions of the module.

Figure 1-4: CPC1301 with Heatspreader Installed, Side View



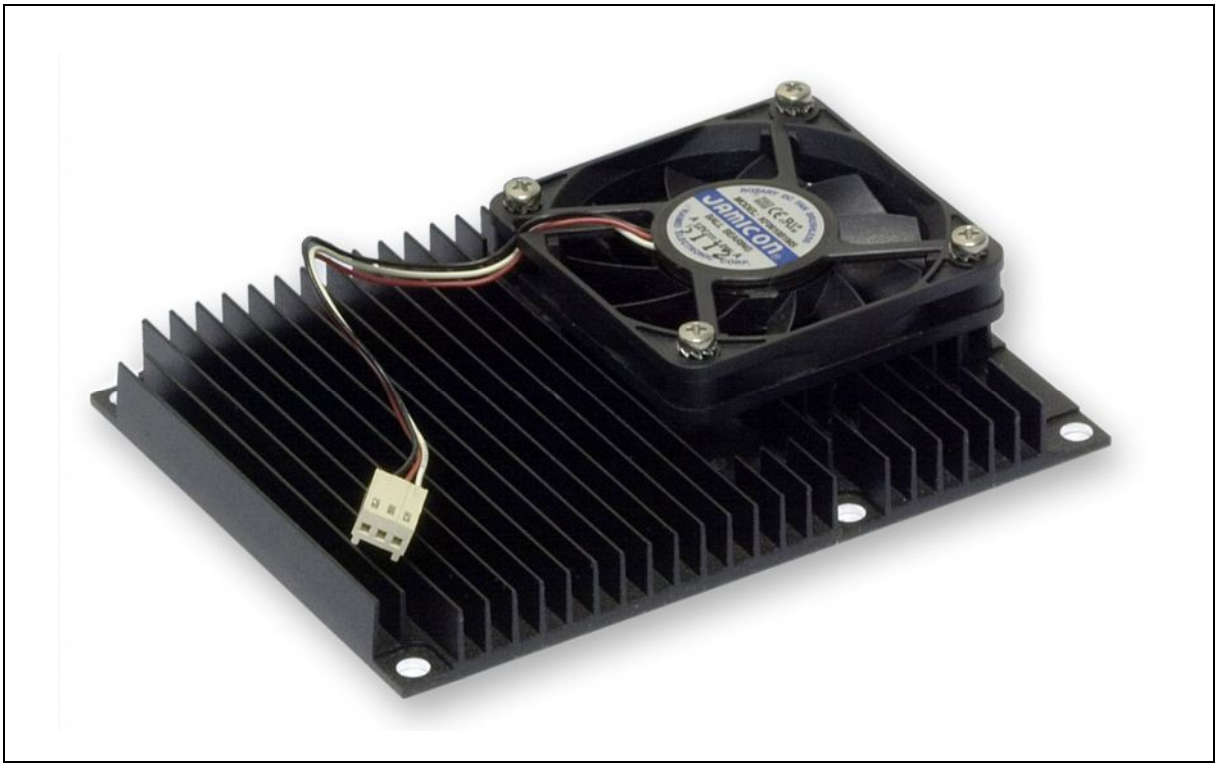
The appearance may vary for different versions of the module.

Figure 1-5: Heatspreader Plate



The appearance may vary for different versions of the plate.

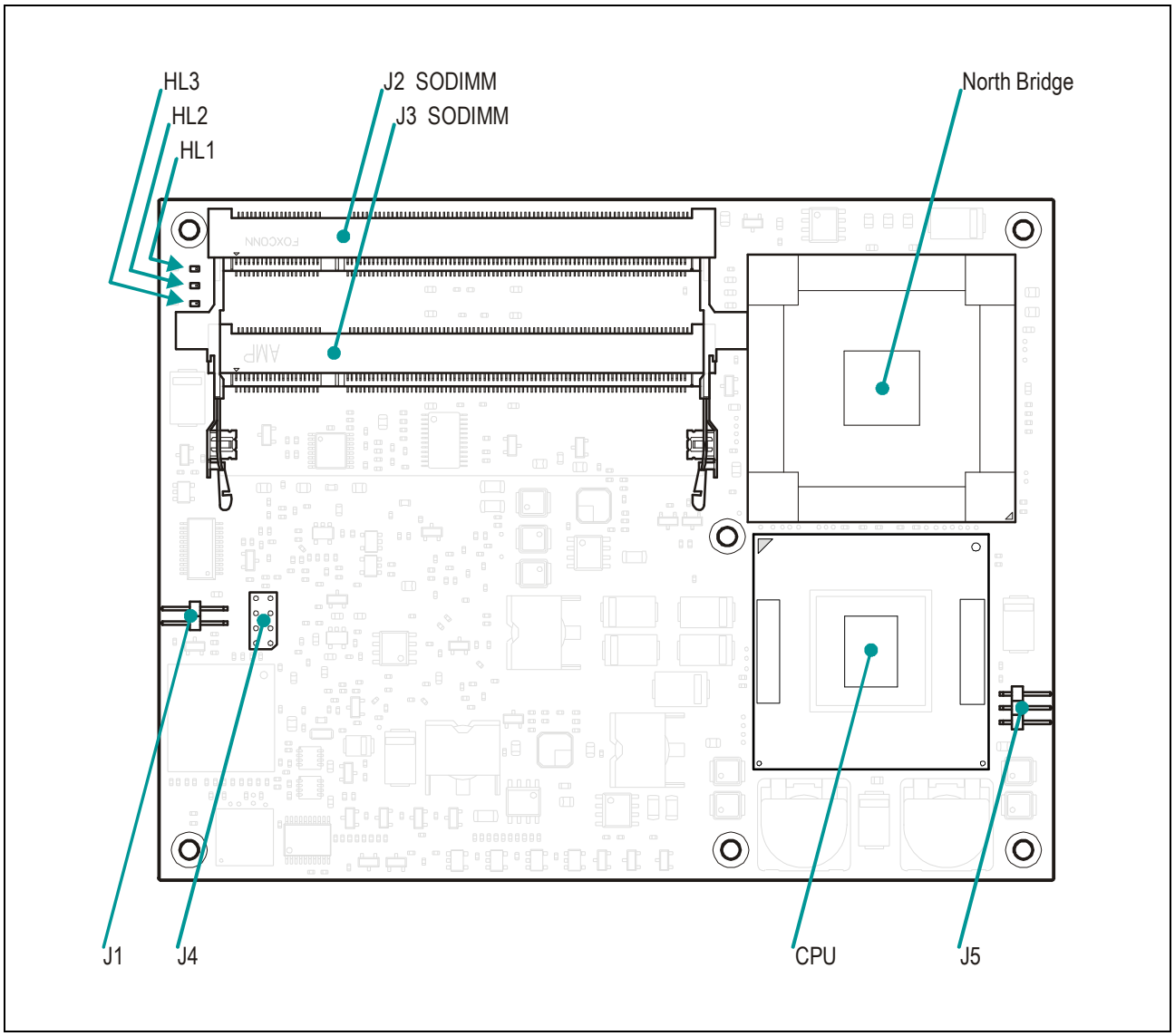
Figure 1-6: Ribbed Heatsink with Mounted Fan



The appearance may vary for different versions of the heatsink.

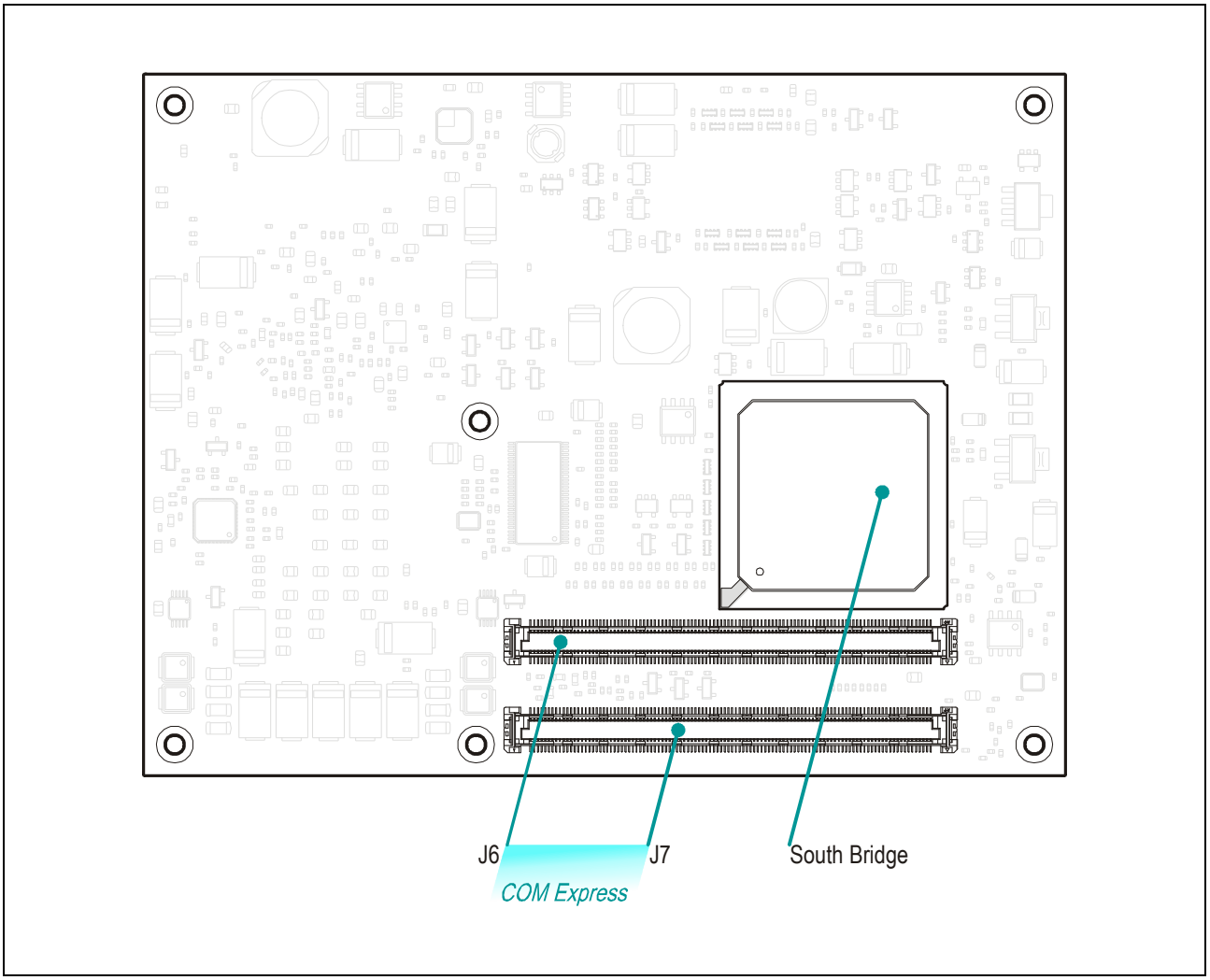
1.3.3 Module Layout

Figure 1-7: CPC1301 Top Side Layout



The layout may slightly differ for various versions of the module.

Figure 1-8: CPC1301 Bottom Side Layout



The layout may slightly differ for various versions of the module.

1.3.4 Dimensions Diagrams

Figure 1-9: CPC1301 Mounting Dimensions Diagram, Top View

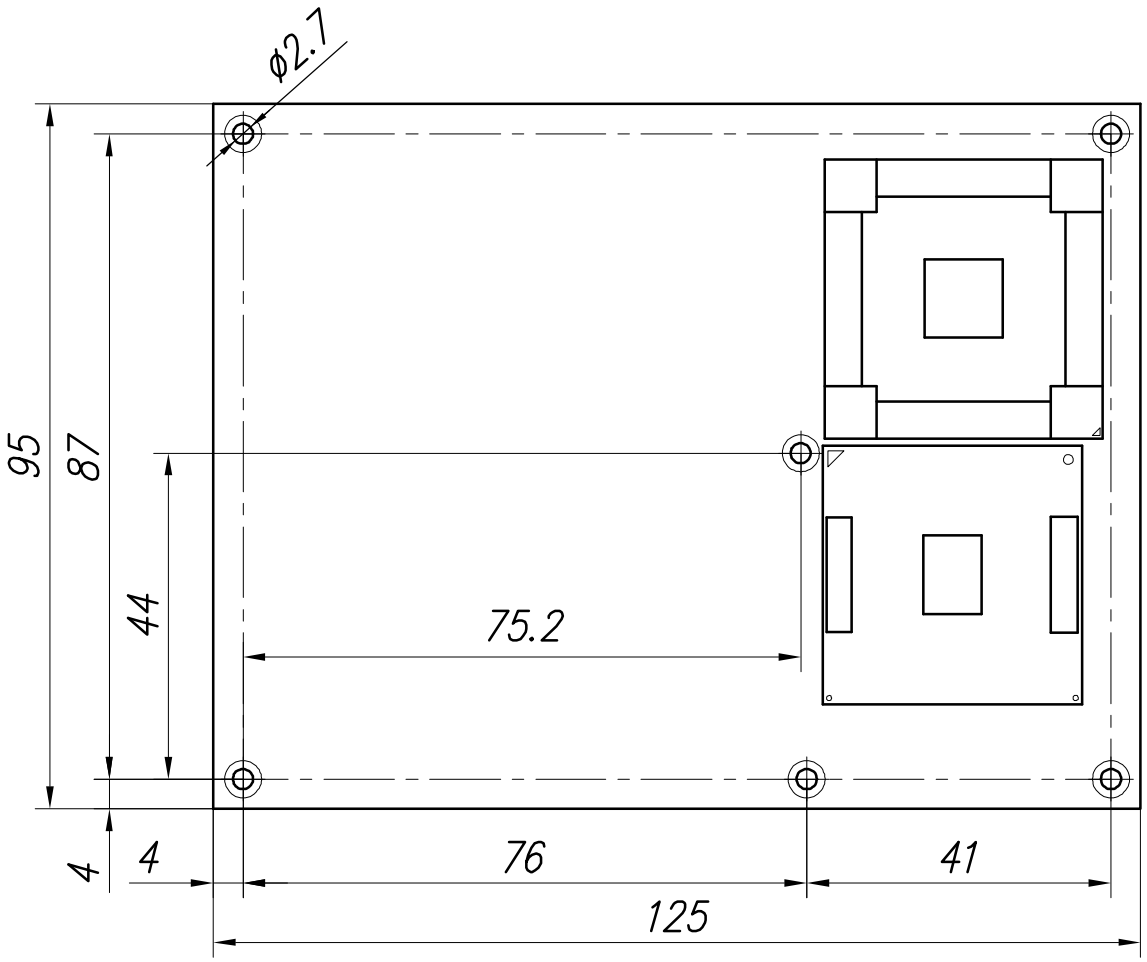


Figure 1-10: CPC1301 Mounting Dimensions Diagram, Bottom View

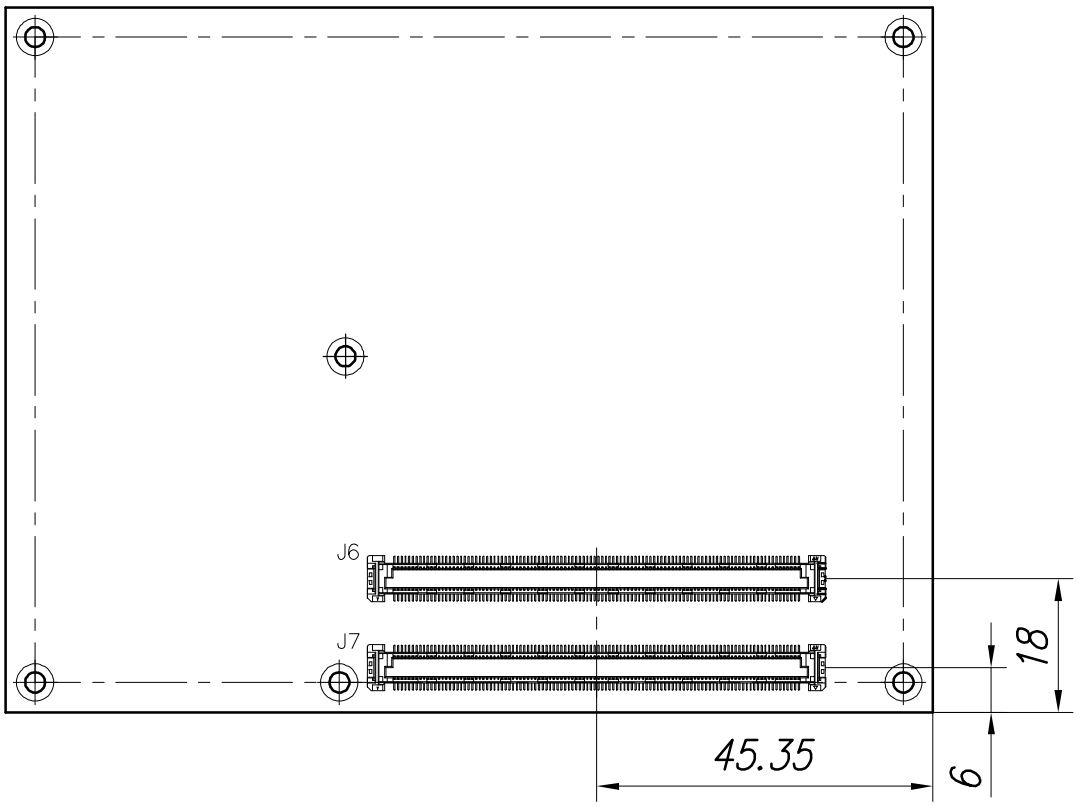
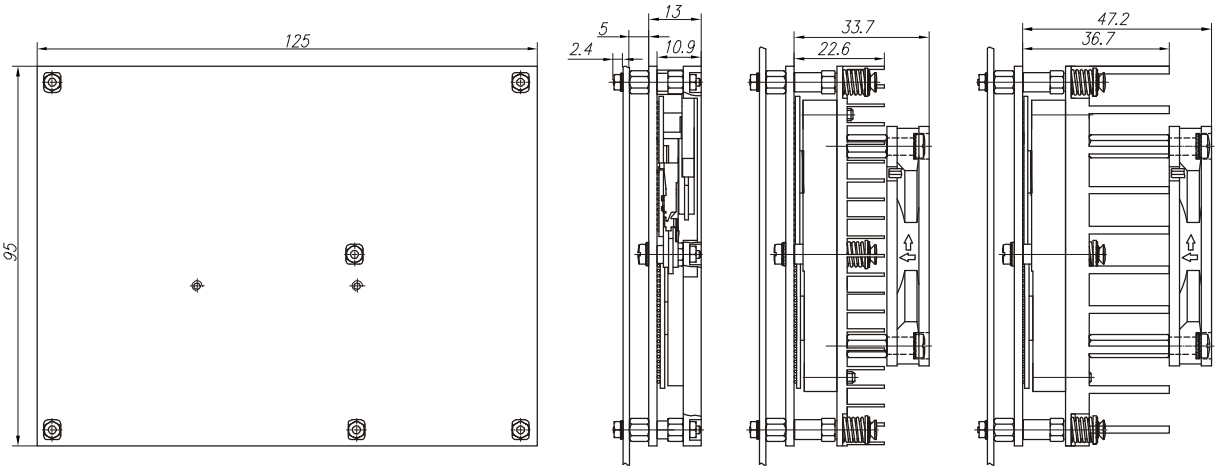


Figure 1-11: CPC1301 Dimensions Diagram, Heatsink Versions



Note: A – Heatspreader mounted, top view
B – Heatspreader mounted, side view
C – Low profile heatsink and a fan mounted, side view
D – High profile heatsink and a fan mounted, side view

Heatsinks design may differ from the shown above.

1.4 Technical Characteristics

1.4.1 Processor, Memory and Chipset

CPU

Intel® Core™ 2 Duo Processor (L7400)

- Up to 1.5 GHz
- Up to 4 MB L2 on-die cache
- 667 MHz PSB
- Enhanced SpeedStep

Intel® Core™ Duo Processor (L2400)

- Up to 1.66 GHz
- Up to 2 MB L2 on-die cache
- 667 MHz PSB
- Enhanced SpeedStep

Intel® Celeron M 423 Processor

- Up to 1.06 GHz
- Up to 2 MB L2 on-die cache
- 533 MHz PSB
- Enhanced SpeedStep

Memory

Main memory:

- Up to 4 GB of DDR2 SDRAM memory in two SODIMM sockets
- Memory frequency: 667/533 MHz (up to PC5300)
- Dual channel support
- PC SPD compatible

Flash memory:

- 8 Mbit SPI flash memory for BIOS storage

EEPROM memory:

- 64 Kbit of nonvolatile memory on SMBus

Chipset

Intel® 82945GM Graphics and Memory Controller Hub (GMCH)

- Optimized for Intel® Core™ processors
- 32-bit host bus addressing
- 64-bit AGTL+ based PSB interface at 533/667 MHz
- DMI interface
- 64-bit System Memory interface, optimized for dual channel DDR2 SDRAM memory symmetric and asymmetric modes
- Integrated 2D/3D Graphics and H/W Motion Compensation Engines
- Integrated DAC, 400 MHz
- Intel® Graphics Media Accelerator 950
- Intel® Stable Image Technology

Intel® I/O Controller Hub ICH7M DH

- PCI-Express base specification rev. 1.0a
- PCI Bus rev. 2.3 interface at 33 MHz
- Integrated Serial ATA host controller
- Integrated IDE controller Ultra ATA 33/66/100, BMIDE and PIO modes
- USB 2.0 host interface
- ACPI 3.0 compliant power management logic
- DMI interface
- Low Pin Count (LPC) interface
- SPI interface
- Intel HighDefinition Audio interface, AC'97 v. 2.3 support
- Additional timer
- Intel® Active Management Technology support
- Enhanced DMA controller
- High precision event timers
- Interrupt controller
- System Management Bus
- Firmware Hub (FWH) interface support via LPC bus

1.4.2 Interfaces

PCI Bus Interface

Compliant with 2.3 Specification at 33 MHz

- System master operation
- Up to 6 Bus Master devices
- Support for 32-bit addressing on PCI using DAC protocol
- Six available PCI REQ/GNT pairs
- 3.3/5.0 V compatible

PCI Express Interface

- Five x1 channels
- Four x1 channels can be aggregated into one x4 channel
- One x16 PCI Express interface for external graphics card connection.
  It is possible to connect x2, x4, x8 PCI Express devices along with integrated graphics controller with certain limitations. Please, apply to manufacturer for details.

SMBus Interface

- SMBus 2.0 Specification support
- Compatible with most two-wire components that are also I^2C compatible

USB Interface

- Up to eight USB 2.0 channels
- UHCI and EHCI support
- Data transfer rate up to 480 Mb/s

LAN Interface

- One 10/100/1000 Mb/s Gigabit Ethernet interface
- Intel 82573V PCI-E bus Ethernet controller
- Automatic mode recognition
- Automatic cabling configuration recognition
- Cabling requirement: Category 5, UTP, four (two)-pair cabling

Video Interfaces

- Built-in Intel 2D/3D high performance Intel® Graphics Media Accelerator 950
- Hardware Motion Compensation Engine for software MPEG2 and MPEG4 decoding
- Intel® Stable Image Technology
- Video memory up to 64 MB shared with system

VGA CRT

- Resolutions of up to 2048 x 1536, 16 bit at 75 Hz refresh rate
- Integrated RAMDAC, 400 MHz

LVDS TFT

- Dual/single channel interface
- Resolutions of up to 1600 x 1200, 18 bpp
- Spread spectrum clocking 25-112 MHz single/dual channel

S-video

- Three integrated 10-bit DACS
- NTSC/PAL
- HDTV support – 480p/720p/1080i/1080p

Audio

- AC97 audio rev. 2.3
- High Definition audio available

Low Pin Count (LPC) Interface

- Super I/O Winbond W83627HF interfaces supported:
  PS/2 Keyboard+Mouse, 1xLPT, 1xFDD, 2xRS-232

Mass Storage

EIDE Ultra ATA 100/66/33

- One channel

Serial ATA interface

- Two channels
- Data transfer rates up to 150 MB/s

GPIO Lines

- 4-bit I/O port
- GPI[3:0] and GPO[3:0] signals are used. Operation mode of GPO2 and GPO3 is selected in BIOS Setup utility (see details in Chapter 4, Configuration)

I^2C Interface

- Master mode at 100 kHz supported

1.4.3 Control and Monitoring

Thermal Management

The processor is protected from overheating by:

- Internal processor temperature control unit, which initiates CPU shut down
- Processor die temperature monitor
- Heat spreader or heatsink with fan

System Parameters Monitoring

LM87 hardware monitor is used for supervision of the critical system parameters:

- System parameters monitoring via I^2C or SMBus (switched in BIOS Setup)
- Main power voltages monitoring (V_{ccCore}, +3.3V, +5V, +12V)
- Processor die temperature monitoring
- Board temperature under SODIMM modules monitoring

LEDs

- Standby power LED (green)
- System status indicator (red)
- SATA activity LED (yellow)

Watchdog Timers

- Chipset watchdog timer
- FPGA based programmable timer

Additional Features

- Support for USB keyboard without Super I/O on carrier board

1.4.4 General

Mechanical

COM Express Basic form-factor

Dimensions:	95 × 125 mm (see Figure 1-7 for details)
Board weight:	less than 0.600 kg ~0.150 kg (without heatsink/heatspreader and fan) (to be amended)
Shock/Vibration:	50G / 2G

Power Supply

Power is supplied to the module through COM Express connectors

Max 3.2 A @ 12 V; 1.0 A @ 5V_SBY; 6.0 µA in off state (VCC_RTC)

See Chapter 6 for details on power supply requirements

Temperature Ranges

Operational:	0°C ... +70°C – commercial range -40°C ... +85°C – industrial range (with CS1.06 only)
Storage:	-55°C ... +95°C

Humidity

5% to 95% RH, non-condensing

Battery

External 3.0 V lithium battery for RTC on carrier board.
Use PANASONIC BR2032 or compatible

MTBF

Not less than 140000 hours

The value is calculated according to: Telcordia Issue 1 model, Method I Case 3, for continuous operation at a surface location, at normal environmental conditions (Russian State Standard GOST 15150-69, "UHL4" climatic parameters) and at ambient temperature 30°C.

1.4.5 Software

BIOS

Flash memory based enhanced Phoenix® BIOS

Operating Systems

Microsoft DOS v. 3.30 – 6.22

Fastwel DOS (MS-DOS compatible);

Windows 2000, XP, XP Embedded;

QNX v. 4.20, 6.0

Linux 2.6

1.5 Delivery Checklist

The CPC1301 supplied set includes:

1. CPC1301 module
2. Heatspreader / Ribbed heatsink (depending on version)
3. Optional cooling fan (depending on version)
4. Set of screws and standoffs (depending on version)
5. CD-ROM with documentation and service software
6. Antistatic bag
7. Consumer carton box

Note:

Keep the antistatic bag and the original package at least until the warranty period is over. It can be used for future storage or warranty shipments.

2 Detailed Description

2.1 Processor, Memory and Chipset

2.1.1 Processors

The CPC1301 module is based on the Intel® Core™ 2 Duo / Core™ Duo / Celeron M processors operating at frequencies of up to 1.66 GHz.

These processors combine high performance and low power consumption. Its enhanced performance characteristics are provided by a newly designed processor core with an integrated 64 KB L1 (32 KB instruction cache and 32 KB write-back data cache) and 2048 KB shared L2 cache (4 MB for Core™ 2 Duo).

These processors support Enhanced Intel SpeedStep® technology to control power consumption and processor die temperature by switching the processor core voltage and frequency between several modes without need to reset the system.

Important performance features of the Intel® Core Duo/Celeron M 423 processors also include

- Level 2 cache memory with Advanced Transfer architecture
- Intel® Architecture with Dynamic Execution
- Data Prefetch Logic
- Streaming SIMD (SSE2, SSE3) extensions
- 533/667 MHz FSB
- Execute Disable Bit technology support
- Intel® Virtualization technology support
- Dynamic Cache Sizing

Moreover, Intel® Core 2 Duo processors support:

- Intel® 64 Architecture
- 4 MB Level 2 cache shared between cores
- Supplemental Streaming SIMD Extensions 3 (SSSE3)

2.1.2 System Memory

The module has two 200-contact SODIMM sockets onboard for DDR2 SDRAM memory modules. Total capacity of PC5300 compliant memory can be up to 4 GB. Dual channel operation and PC SPD (Serial Presence Detect) Specification are supported.

2.1.3 Chipset

The CPC1301 chipset consists of the following devices:

- 82945GM Graphics and Memory Controller Hub (GMCH) with DMI (Direct Media Interface) bus support
- ICH7M DH I/O Controller Hub with DMI bus
- One 1 MB SPI-flash memory chip

North Bridge

The 82945GM Graphics and Memory Controller Hub (GMCH) in the 1466 µFCBGA package provides interfaces with the microprocessor, dual- or single-channel DDR2 SDRAM system memory and includes a high performance graphics accelerator (Intel® GMA 950) as well as a x16 PCI Express interface for connection of an external graphics card on carrier board, for connection of general purpose input/output devices(*), or for two SDVO channels of the integrated graphics controller. It also provides a DMI interface to the ICH.

Table 2-1: PCI Express x16 Interface: Available Configurations

Device	PCI Express Link Width	Integrated Graphics Controller	SDVO Interface
External graphics controller	x1, x16	Disabled	Disabled
General pupose IO device(*)	x1	Enabled	Enabled
General pupose IO device(*)	x2, x4, x8	Enabled	Disabled

(*) With limitations. Please, apply to manufacturer for details

The 945GM is optimized for the Intel® Core family of microprocessors. The chipset supports a PSB frequency of 533/667 MHz with AGTL+ signaling. It also supports 32-bit addressing for using up to 4 GB memory address space. The 945GM includes a system memory controller with a 64-bit interface. The chipset supports up to PC5300 dual or single channel DDR2 SDRAMs for use as system memory.

When running in internal graphics mode, high performance video capabilities of the 945GM are supported by a 2D/3D graphics accelerator and H/W Motion Compensation engines for software MPEG2 decoding. The internal graphics controller allows connection of a standard CRT display, a LVDS TFT panel, and digital displays with DVI interface.

South Bridge

The ICH7M DH is a multifunctional I/O Controller Hub that provides interfaces to the PCI-Express and PCI buses and to a number of PC interfaces, such as UltraDMA 100/66/33, SATA, USB 2.0 host interface, LPC interface, SPI interface, and AC'97 or HD digital audio. The ICH communicates with the host controller directly via a dedicated DMI interface.

I/O Controller Hub features are:

- PCI-Express Base Specification enhanced rev 1.0a
- PCI bus interface, rev. 2.3, up to 6 Bus Master devices
- ACPI Power Management logic support
- Bus Master EIDE controller UltraDMA 100/66/33
- SATA interface, two channels
- USB controller supporting eight USB 2.0 ports
- DMI interface with 945GM
- Intel® Active Management Technology
- LPC interface
- SPI interface
- AC'97 2.3 and High Definition audio interface
- RTC controller
- Additional timer

2.2 I^2C Controller Input/Output Ports

I^2C controller realized in FPGA as a LPC bus device supports Master mode and 100 kHz transmission frequency. Its activation and IRQ selection is performed in BIOS Setup. The device is operated via the registers within I/O ports area. Base address in I/O area is set by BIOS. It is indicated within the “Help” screen region to the right of “I2C Controller / GPIO Port” menu item of BIOS Setup program.

GPIO (BASE+3) register is used to read and write GPI[3:0], GPO[3:0] I/O signals, routed to COM Express connector.

Table 2-2: I^2C Controller Registers

I/O Port Address	Type	Hard Reset	Configuration Register
Base+0	R/W	00h	Status Register
Base+1	R/W	00h	Control Register
Base+2	R/W	00h	Data Register
Base+3	R/W	0xh	GPIO Register

2.2.1 I²C Controller Registers Description

Status Register (Base+0)

Bit	Name	Type	Function
7	MCF	R/W	Transaction state indicator: Completed / In process. It is set to “1” after acknowledgement (ACK) and stop phases of the transaction (STOP Condition). To start the next transaction it has to be cleared by writing “1” here.
6	–		Reserved
5	MBB	R	Bus Busy indicator. It is set to “1” on detection of START Condition and is reset to “0” on STOP Condition.
4	MAL	R/W	Bus Arbitration Lost indicator. It is set to “1”, if bus arbitration is lost during START/STOP/Transmit phases. It can be reset by writing “1” to this bit.
3	–		Reserved
2	–		Reserved
1	MIF	R/W	Interrupt indicator. It is set to “1”, if MCF=“1” or MAL=“1”. The interrupt is generated, if MIEN bit is set in Control Register. It should be reset by writing “1” to this bit position.
0	RXAK	R	Transaction acknowledgement indicator. It is set to “0” on ACK receipt; it is set to “1”, if ACK is not received. In the absence of the transmission transaction acknowledgement (RXAK=1), the MSTA bit is automatically reset to “0” and STOP Condition is enabled.

Control Register (Base+1)

Bit	Name	Type	Function
7	MEN	R/W	Controller enable/disable. Writing “1” here enables I²C controller. Writing “0” resets I²C controller and disables it.
6	MIEN	R/W	Interrupt enable. Writing “1” here enables interrupt generation. The interrupt is generated, if MIF bit is set in Status Register.
5	MSTA	R/W	Start transaction. Writing “1” here enables START Condition and transmit/receive phase depending on MTX bit value. Writing “0” here enables STOP Condition. In the absence of the transmit transaction acknowledgement (RXAK=1), this bit is automatically reset to “0” and STOP Condition is enabled.
4	MTX	R/W	Transaction mode selection. Writing “1” enables transmission mode, “0” – reception mode.
3	TXAK	R/W	Receive transaction acknowledgement bit. Writing “0” here enables acknowledgement (ACK), writing “1” disables acknowledgement (NAK).
2	RSTA	R/W	Restart. Writing “1” here enables Repeated Start Condition. It is reset to “0” automatically on completion of the restart phase.
1	–		Reserved
0	–		Reserved

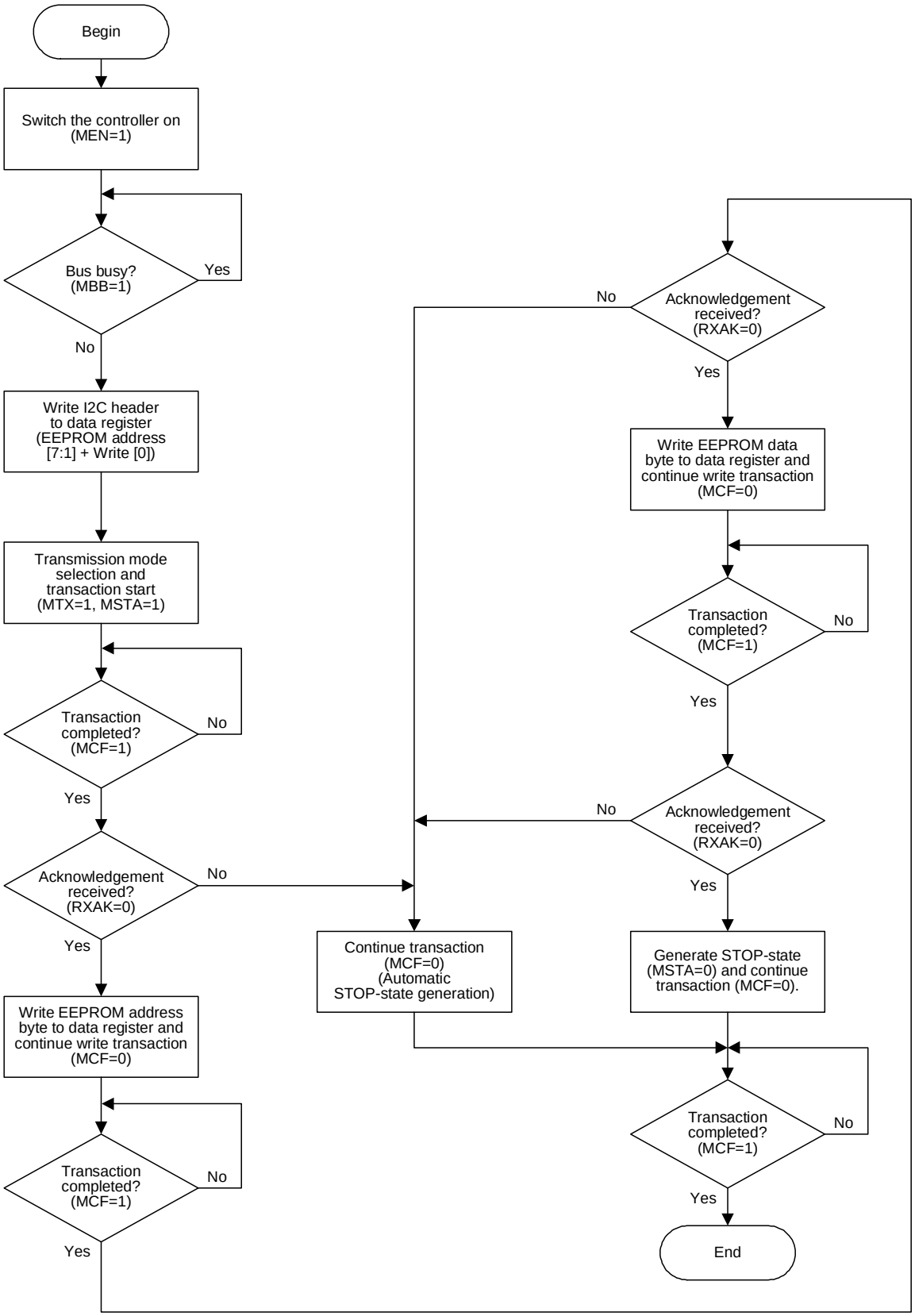
Data Register (Base+2)

Bit	Name	Type	Function
7-0		R/W	In transmit mode, data written into this register is transmitted to the I^2C bus; in receive mode, this register contains the data received from the I^2C bus.

GPIO Register (Base+3)

Bit	Name	Type	Function
7-4	GPO	R/W	GPO[3:0] output values. GPO2 and GPO3 signals have dual functionality. Operation modes are set in BIOS Setup. They are used either as output ports or as ALERT# and THERM# outlets of LM87 chip.
3-0	GPI	R	GPI[3:0] input values

Figure 2-1: I^2C Controller Operation Flowchart: Write Data Byte to EEPROM Atmel AT24C02



2.1 Watchdog Timer

The FPGA based watchdog timer operates as an LPC device. Its activation and IRQ selection is performed in BIOS Setup. The device is operated via the registers within I/O ports area. Base address in I/O area is set by BIOS. It is indicated within the “Help” screen region to the right of “Watchdog Timer (WDT)” menu item of BIOS Setup program.

Watchdog timer includes 24-bit Timer Current Value Register, which is decremented at frequency of 32.768 kHz, and Timer Initial Value Register. It is possible to set the timeout period from 0 to 512 seconds with increments of 30.52 μs by changing the value in this register. On the first expiry of the timeout period the watchdog timer can invoke an interrupt or Reset on second expiry.

By default, the watchdog timer is not active. The equation below can be used to calculate the timeout T_{WD} in μs as a function of the decimal value in the Timer Initial Value Register (K_{WD}):

$$T_{WD}\,[\mu s] = K_{WD} * 10^6 / 2^{15}$$

For example, decimal value "1" of K_{WD} (000001h) corresponds to the timeout of 30.52 μs, and K_{WD} = 16777215 (FFFFFFh) – 512 seconds.

It is possible to reset the counter to the initial value in one of the following ways:

1. Write any value to Timer Current Value Register
2. Write any value to 80h port. This mode is enabled in BIOS Setup and is available only if access cycles to 80h port are translated to LPC bus.

TMF flag is set on the first timeout expiry, STF flag is set on the second.

Procedure of the watchdog timer control via I/O registers:

1. Stop the watchdog countdown.
2. Write the timeout value to the Timer Initial Value Register.
3. Initialize the watchdog in one of the two possible ways, for example, by writing any value to the Timer Current Value Register. This leads to wrting of the value in Timer Initial Value Register to the Timer Current Value Register.
4. Start the countdown and, if needed, enable the automatic Reset of the module.
5. It is necessary to strobe the watchdog timer with the period less than the set timeout period (T_{WD}) in one of the ways described above. If the watchdog timer is not reset during the first timeout period, the TMF flag is set the interrupt is generated (if enabled). If the watchdog timer is not reset during the next timeout period, the STF flag is set and the second interrupt is generated (or the module will reboot, if Reset is enabled).

2.2.2 WDT Controller I/O Registers

Timer Current Value Register [23:0]

Base+0h		
Bit	**Name**	**Description**
7:0	Timer_Current_Value[7:0]	Write/Read: Bits 7:0 of the current timer value
Base+1h		
Bit	**Name**	**Description**
7:0	Timer_Current_Value[15:8]	Write/Read: Bits 15:8 of the current timer value
Base+2h		
Bit	**Name**	**Description**
7:0	Timer_Current_Value[23:16]	Write/Read: Bits 23:16 of the current timer value

Timer Initial Value Register [23:0]

Base+3h		
Bit	**Name**	**Description**
7:0	Timer_Initial_Value[7:0]	Write/Read: Bits 7:0 of the initial timer value
Base+4h		
Bit	**Name**	**Description**
7:0	Timer_Initial_Value[15:8]	Write/Read: Bits 15:8 of the initial timer value
Base+5h		
Bit	**Name**	**Description**
7:0	Timer_Initial_Value[23:16]	Write/Read: Bits 23:16 of the initial timer value

Status Register

Base+6h		
Bit	**Name**	**Description**
7:3	–	Reserved
2	STM	Write/Read: Second timeout flag. It is set to “1”, if TMF=1. This flag invokes interrupt. If RSTE=1 (Reset enabled), the module is rebooted. Cleared by writing “1” into this bit.
1	–	Reserved
0	TMF	Write/Read: Timeout flag. It is set to “1” on expiry of the timeout. This flag enables interrupt generation. Cleared by writing “1” into this bit or by writing to 80h port (if this mode is enabled).

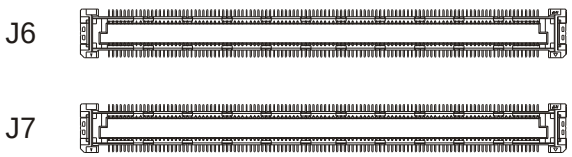
Control Register

Base+7h		
Bit	**Name**	**Description**
7:2	–	Reserved
1	CNTE	Write/Read: Writing “1” enables watchdog countdown.
0	RSTE	Write/Read: Writing “1” enables Reset on timeout.

2.3 CPC1301 Connectors

2.3.1 COM Express Connectors

Figure 2-2: COM Express Connectors



Standard COM Express connectors (J6 and J7) are used to route module's interfaces to carrier board connectors. The following table presents pin designation for these connectors.

Table 2-3: COM Express Connectors Pinout

	AB Connector (J7)			CD Connector (J6)		
##	Cont.	Signal	Note	Cont.	Signal	Note
1	A1	GND_(FIXED)		C1	GND_(FIXED)	
2	A2	GBE0_MDI3-		C2	IDE_D7	
3	A3	GBE0_MDI3+		C3	IDE_D6	
4	A4	GBE0_LINK100#		C4	IDE_D3	
5	A5	GBE0_LINK1000#		C5	IDE_D15	
6	A6	GBE0_MDI2-		C6	IDE_D8	
7	A7	GBE0_MDI2+		C7	IDE_D9	
8	A8	GBE0_LINK#		C8	IDE_D2	
9	A9	GBE0_MDI1-		C9	IDE_D13	
10	A10	GBE0_MDI1+		C10	IDE_D1	
11	A11	GND_(FIXED)		C11	GND_(FIXED)	
12	A12	GBE0_MDI0-		C12	IDE_D14	
13	A13	GBE0_MDI0+		C13	IDE_IORDY	Pull-up 10K to 3.3V STBY
14	A14	GBE0_CTREF		C14	IDE_IOR#	
15	A15	SUS_S3#		C15	PCI_PME#	Pull-up 10K to 3.3V STBY
16	A16	SATA0_TX+		C16	PCI_GNT2#	
17	A17	SATA0_TX-		C17	PCI_REQ2#	Pull-up 10K to 3.3V
18	A18	SUS_S4#		C18	PCI_GNT1#	
19	A19	SATA0_RX+		C19	PCI_REQ1#	Pull-up 10K to 3.3V
20	A20	SATA0_RX-		C20	PCI_GNT0#	
21	A21	GND_(FIXED)		C21	GND_(FIXED)	
22	A22	SATA2_TX+		C22	PCI_REQ0#	Pull-up 10K to 3.3V
23	A23	SATA2_TX-		C23	PCI_RESET#	
24	A24	SUS_S5#		C24	PCI_AD0	
25	A25	SATA2_RX+		C25	PCI_AD2	
26	A26	SATA2_RX-		C26	PCI_AD4	
27	A27	BATLOW#	Pull-up 10K to 3.3V STBY	C27	PCI_AD6	
28	A28	ATA_ACT#	Pull-up 10K to 3.3V	C28	PCI_AD8	
29	A29	AC_SYNC		C29	PCI_AD10	
30	A30	AC_RST#		C30	PCI_AD12	
31	A31	GND_(FIXED)		C31	GND_(FIXED)	
32	A32	AC_BITCLK		C32	PCI_AD14	
33	A33	AC_SDOUT		C33	PCI_C/BE1#	
34	A34	BIOS_DISABLE#	Pull-up 10K to 3.3V STBY	C34	PCI_PERR#	Pull-up 10K to 3.3V

##	AB Connector (J7)			CD Connector (J6)		
	Cont.	Signal	Note	Cont.	Signal	Note
35	A35	THRMTRIP#		C35	PCI_LOCK#	Pull-up 10K to 3.3V
36	A36	USB6-		C36	PCI_DEVSEL#	Pull-up 10K to 3.3V
37	A37	USB6+		C37	PCI__IRDY#	Pull-up 10K to 3.3V
38	A38	USB_6_7_OC#	Pull-up 10K to 3.3V STBY	C38	PCI_C/BE2#	
39	A39	USB4-		C39	PCI_AD17	
40	A40	USB4+		C40	PCI_AD19	
41	A41	GND_(FIXED)		C41	GND_(FIXED)	
42	A42	USB2-		C42	PCI_AD21	
43	A43	USB2+		C43	PCI_AD23	
44	A44	USB_2_3_OC#	Pull-up 10K to 3.3V STBY	C44	PCI_C/BE3#	
45	A45	USB0-		C45	PCI_AD25	
46	A46	USB0+		C46	PCI_AD27	
47	A47	VCC_RTC		C47	PCI_AD29	
48	A48	EXCD0_PERST#		C48	PCI_AD31	
49	A49	EXCD0_CPPE#		C49	PCI_IRQA#	Pull-up 10K to 3.3V
50	A50	LPC_SERIRQ	Pull-up 10K to 3.3V STBY	C50	PCI_IRQB#	Pull-up 10K to 3.3V
51	A51	GND_(FIXED)		C51	GND_(FIXED)	
52	A52	PCIE_TX5+	Not used	C52	PEG_RX0+	
53	A53	PCIE_TX5-	Not used	C53	PEG_RX0-_	
54	A54	GPI0	Pull-down 4K-34.5K to GND	C54	TYPE0#	Not connected
55	A55	PCIE_TX4+		C55	PEG_RX1+	
56	A56	PCIE_TX4-		C56	PEG_RX1-	
57	A57	GND		C57	TYPE1#	Not connected
58	A58	PCIE_TX3+		C58	PEG_RX2+	
59	A59	PCIE_TX3-		C59	PEG_RX2-	
60	A60	GND_(FIXED)		C60	GND_(FIXED)	
61	A61	PCIE_TX2+		C61	PEG_RX3+	
62	A62	PCIE_TX2-		C62	PEG_RX3-	
63	A63	GPI1	Pull-down 4K-34.5K to GND	C63	RSVD	
64	A64	PCIE_TX1+		C64	RSVD	
65	A65	PCIE_TX1-		C65	PEG_RX4+	
66	A66	GND		C66	PEG_RX4-	
67	A67	GPI2	Pull-down 4K-34.5K to GND	C67	RSVD	
68	A68	PCIE_TX0+		C68	PEG_RX5+	
69	A69	PCIE_TX0-		C69	PEG_RX5-	
70	A70	GND_(FIXED)		C70	GND_(FIXED)	
71	A71	LVDS_A0+		C71	PEG_RX6+	
72	A72	LVDS_A0-		C72	PEG_RX6-	
73	A73	LVDS_A1+		C73	SDVO_DATA	
74	A74	LVDS_A1-		C74	PEG_RX7+	
75	A75	LVDS_A2+		C75	PEG_RX7-	
76	A76	LVDS_A2-		C76	GND	
77	A77	VDS_VDD_EN		C77	RSVD	
78	A78	LVDS_A3+	Not used	C78	PEG_RX8+	
79	A79	LVDS_A3-	Not used	C79	PEG_RX8-	
80	A80	GND_(FIXED)		C80	GND_(FIXED)	
81	A81	LVDS_A_CK+		C81	PEG_RX9+	
82	A82	LVDS_A_CK-		C82	PEG_RX9-	
83	A83	LVDS_I2C_CK	Pull-up 10K to 3.3V	C83	RSVD	
84	A84	LVDS_I2C_DAT	Pull-up 10K to 3.3V	C84	GND	
85	A85	GPI3	Pull-down 4K-34.5K to GND	C85	PEG_RX10+	
86	A86	KBD_RST#	Pull-up 10K to 3.3V STBY	C86	PEG_RX10-	
87	A87	KBD_A20GATE	Pull-up 10K to 3.3V STBY	C87	GND	
88	A88	PCIE0_CK_REF+		C88	PEG_RX11+	
89	A89	PCIE0_CK_REF-		C89	PEG_RX11-	
90	A90	GND_(FIXED)		C90	GND_(FIXED)	
91	A91	RSVD		C91	PEG_RX12+	

##	AB Connector (J7)			CD Connector (J6)		
	Cont.	Signal	Note	Cont.	Signal	Note
92	A92	RSVD		C92	PEG_RX12-	
93	A93	GPO0		C93	GND	
94	A94	RSVD		C94	PEG_RX13+	
95	A95	RSVD		C95	PEG_RX13-	
96	A96	GND		C96	GND	
97	A97	VCC_12V		C97	RSVD	
98	A98	VCC_12V		C98	PEG_RX14+	
99	A99	VCC_12V		C99	PEG_RX14-	
100	A100	GND_(FIXED)		C100	GND_(FIXED)	
101	A101	VCC_12V		C101	PEG_RX15+	
102	A102	VCC_12V		C102	PEG_RX15-	
103	A103	VCC_12V		C103	GND	
104	A104	VCC_12V		C104	VCC_12V	
105	A105	VCC_12V		C105	VCC_12V	
106	A106	VCC_12V		C106	VCC_12V	
107	A107	VCC_12V		C107	VCC_12V	
108	A108	VCC_12V		C108	VCC_12V	
109	A109	VCC_12V		C109	VCC_12V	
110	A110	GND_(FIXED)		C110	GND_(FIXED)	
111	B1	GND_(FIXED)		D1	GND_(FIXED)	
112	B2	GBE0_ACT#		D2	IDE_D5	
113	B3	LPC_FRAME		D3	IDE_D10	
114	B4	LPC_AD0		D4	IDE_D11	
115	B5	LPC_AD1		D5	IDE_D12	
116	B6	LPC_AD2		D6	DE_D4	
117	B7	LPC_AD3		D7	IDE_D0	
118	B8	LPC_DRQ0#		D8	IDE_REQ	
119	B9	LPC_DRQ1#		D9	IDE_IOW#	
120	B10	LPC_CLK		D10	IDE_ACK#	
121	B11	GND_(FIXED)		D11	GND_(FIXED)	
122	B12	PWRBTN#		D12	IDE_IRQ	Pull-up 10K to 3.3V STBY
123	B13	SMB_CK	Pull-up 2.2K to 3.3V STBY	D13	IDE_A0	
124	B14	SMB_DAT	Pull-up 2.2K to 3.3V STBY	D14	IDE_A1	
125	B15	SMB_ALERT#		D15	IDE_A2	
126	B16	SATA1_TX+	Not used	D16	IDE_CS1#	
127	B17	SATA1_TX-	Not used	D17	IDE_CS3#	
128	B18	SUS_STAT#		D18	IDE_RESET#	Pull-down 100K
129	B19	SATA1_RX+	Not used	D19	PCI_GNT3#	
130	B20	SATA1_RX-	Not used	D20	PCI_REQ3#	Pull-up 10K to 3.3V
131	B21	GND_(FIXED)		D21	GND_(FIXED)	
132	B22	SATA3_TX+	Not used	D22	PCI_AD1	
133	B23	SATA3_TX-	Not used	D23	PCI_AD3	
134	B24	PWR_OK		D24	PCI_AD5	
135	B25	SATA3_RX+	Not used	D25	PCI_AD7	
136	B26	SATA3_RX-	Not used	D26	PCI_C/BE0#	
137	B27	WDT		D27	PCI_AD9	
138	B28	AC_SDIN2		D28	PCI_AD11	
139	B29	AC_SDIN1		D29	PCI_AD13	
140	B30	AC_SDIN0		D30	PCI_AD15	
141	B31	GND_(FIXED)		D31	GND_(FIXED)	
142	B32	SPKR		D32	PCI_PAR	
143	B33	I2C_CK	Pull-up 2.2K to 3.3V STBY	D33	PCI_SERR#	Pull-up 10K to 3.3V
144	B34	I2C_DAT	Pull-up 2.2K to 3.3V STBY	D34	PCI_STOP#	Pull-up 10K to 3.3V
145	B35	THRM#	Pull-up 10K to 3.3V	D35	PCI_TRDY#	Pull-up 10K to 3.3V
146	B36	USB7-		D36	PCI_FRAME#	Pull-up 10K to 3.3V
147	B37	USB7+		D37	PCI_AD16	
148	B38	USB_4_5_OC#	Pull-up 10K to 3.3V STBY	D38	PCI_AD18	

##	AB Connector (J7)			CD Connector (J6)		
	Cont.	Signal	Note	Cont.	Signal	Note
149	B39	USB5-		D39	PCI_AD20	
150	B40	USB5+		D40	PCI_AD22	
151	B41	GND_(FIXED)		D41	GND_(FIXED)	
152	B42	USB3-		D42	PCI_AD24	
153	B43	USB3+		D43	PCI_AD26	
154	B44	USB_0_1_OC#	Pull-up 10K to 3.3V STBY	D44	PCI_AD28	
155	B45	USB1-		D45	PCI_AD30	
156	B46	USB1+		D46	PCI_IRQC#	Pull-up 10K to 3.3V
157	B47	EXCD1_PERST#		D47	PCI_IRQD#	Pull-up 10K to 3.3V
158	B48	EXCD1_CPPE#		D48	PCI_CLKRUN#	Pull-up 10K to 3.3V STBY
159	B49	SYS_RESET#	Pull-up 10K to 3.3V	D49	PCI_M66EN	Not connected
160	B50	CB_RESET#	Pull-up 4.7K to 3.3V	D50	PCI_CLK	
161	B51	GND_(FIXED)		D51	GND_(FIXED)	
162	B52	PCIE_RX5+	Not used	D52	PEG_TX0+	
163	B53	PCIE_RX5-	Not used	D53	PEG_TX0-	
164	B54	GPO1		D54	PEG_LANE_RV#	Pull-up 4.7K to 3.3V STBY
165	B55	PCIE_RX4+		D55	PE3_TX1+	
166	B56	PCIE_RX4-		D56	PEG_TX1-	
167	B57	GPO2(*)	Or INT# / ALERT# (LM87)	D57	TYPE2#	Not connected
168	B58	PCIE_RX3+		D58	PEG_TX2+	
169	B59	PCIE_RX3-		D59	PEG_TX2-	
170	B60	GND_(FIXED)		D60	GND_(FIXED)	
171	B61	PCIE_RX2+		D61	PEG_TX3+	
172	B62	PCIE_RX2-		D62	PEG_TX3-	
173	B63	GPO3(*)	Or THERM# (LM87)	D63	RSVD	
174	B64	PCIE_RX1_+		D64	RSVD	
175	B65	PCIE_RX1-		D65	PEG_TX4+	
176	B66	WAKE0#	Pull-up 10K to 3.3V STBY	D66	PEG_TX4-	
177	B67	WAKE1#	Pull-up 10K to 3.3V STBY	D67	GND	
178	B68	PCIE_RX0+		D68	PEG_TX5+	
179	B69	PCIE_RX0-		D69	PEG_TX5-	
180	B70	GND_(FIXED)		D70	GND_(FIXED)	
181	B71	LVDS_B0+		D71	PEG_TX6+	
182	B72	LVDS_B0-		D72	PEG_TX6-	
183	B73	LVDS_B1+		D73	SDVO_CLK	
184	B74	LVDS_B1-		D74	PEG_TX7+	
185	B75	LVDS_B2+		D75	PEG_TX7-	
186	B76	LVDS_B2-		D76	GND	
187	B77	LVDS_B3+	Not used	D77	IDE_CBLID#	Pull-down 10K
188	B78	LVDS_B3-	Not used	D78	PEG_TX8+	
189	B79	LVDS_BKLT_EN		D79	PEG_TX8-	
190	B80	GND_(FIXED)		D80	GND_(FIXED)	
191	B81	LVDS_B_CK+		D81	PEG_TX9+	
192	B82	LVDS_B_CK-		D82	PEG_TX9-	
193	B83	LVDS_BKLT_CTRL		D83	RSVD	
194	B84	VCC_5V_SBY		D84	GND	
195	B85	VCC_5V_SBY		D85	PEG_TX10+	
196	B86	VCC_5V_SBY		D86	PEG_TX10-	
197	B87	VCC_5V_SBY		D87	GND	
198	B88	RSVD		D88	PEG_TX11+	
199	B89	VGA_RED		D89	PEG_TX11-	
200	B90	GND_(FIXED)		D90	GND_(FIXED)	
201	B91	VGA_GRN		D91	PEG_TX12+	
202	B92	VGA_BLU		D92	PEG_TX12-	
203	B93	VGA_HSYNC		D93	GND	
204	B94	VGA_VSYNC		D94	PEG_TX13+	
205	B95	VGA_I2C_CK	Pull-up 2.7K to 5V	D95	PEG_TX13-	

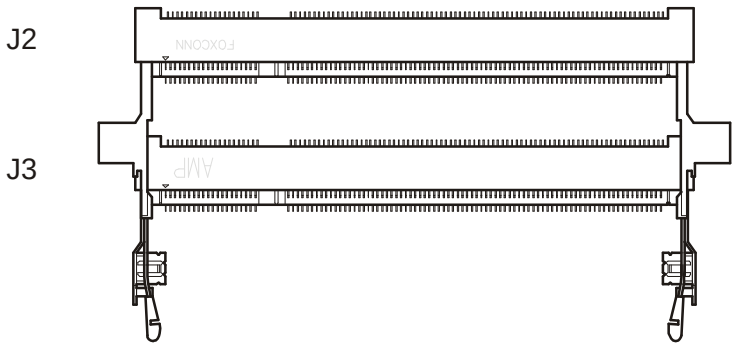
##	AB Connector (J7)			CD Connector (J6)		
	Cont.	Signal	Note	Cont.	Signal	Note
206	B96	VGA_I2C_DAT	Pull-up 2.7K to 5V	D96	GND	
207	B97	TV_DAC_A		D97	PEG_ENABLE#	
208	B98	TV_DAC_B		D98	PEG_TX14+	
209	B99	TV_DAC_C		D99	PEG_TX14-	
210	B100	GND_(FIXED)		D100	GND_(FIXED)	
211	B101	VCC_12V		D101	PEG_TX15+	
212	B102	VCC_12V		D102	PEG_TX15-	
213	B103	VCC_12V		D103	GND	
214	B104	VCC_12V		D104	VCC_12V	
215	B105	VCC_12V		D105	VCC_12V	
216	B106	VCC_12V		D106	VCC_12V	
217	B107	VCC_12V		D107	VCC_12V	
218	B108	VCC_12V		D108	VCC_12V	
219	B109	VCC_12V		D109	VCC_12V	
220	B110	GND_(FIXED)		D110	GND_(FIXED)	

(*) GPO2 and GPO3 mode is set in BIOS Setup.

2.4.1 SODIMM Connectors

Memory modules are installed in standard 200-contact SODIMM sockets – J2 (h = 9.2 mm) and J3 (h = 5.2 mm).

Figure 2-3: SODIMM Connectors



Single memory module can be intalled into any socket. To achieve maximum performance in sinchronous dual channel mode, two memory modules should be of the same capacity.

2.4.2 Other Connectors and Jumpers

J1 and J5 jumpers are used to control system settings. Please refer to Chapter 4 (Configuration) in this document. J4 connector is used for system programming by the manufacturer.

2.4 Local SMBus Devices

CPC1301 incorporates a System Management Bus to access several system monitoring and control devices via a two-wire I^{2}C™ bus interface. The following table presents functions and addresses of onboard SMBus devices.

Table 2-4: SMBus Devices

Address	Device
D2h	CY28411 clock oscillator
A0h	J3 DDR2 SODIMM memory module
A2h	J2 DDR2 SODIMM memory module
ACh	AT24C64 SPD EEPROM chip
5Ch	LM87 hardware monitor

2.5 Serial EEPROM

SPD serial 64 Kbit EEPROM chip is installed on CPC1301 and connected to SMBus.

2.6 LED Indicators

Three LED indicators are located on the top side of the module.

Table 2-5: LED Indicators

Name	Function
HL1	Standby power LED (green). It is on when standby power is supplied to the module.
HL2	System status indicator (red). After power-up this LED blinks rapidly (~8 Hz), after BIOS is started it blinks slowly (~1 Hz) until INT 19h BIOS procedure is finished then is constantly on. This LED is used for system startup troubleshooting.
HL3	SATA activity (yellow). It is on while SATA device is active.

3 Installation

The CPC1301 is easy to install. However, it is necessary to follow the procedures and safety regulations below to install the module correctly without damage to the hardware, or harm to personnel.

For details on installation of an operating system, please refer to the relevant software documentation.

3.1 Safety Regulations

The following safety regulations must be observed when installing or operating the CPC1301. Fastwel assumes no responsibility for any damage resulting from infringement of these rules.

Warning!

When handling or operating the module, special attention should be paid to heatspreader or heatsink, because they can get very hot during operation. Do not touch heatspreader or heatsink when installing or removing the module immediately after the operation.

Moreover, the module should not be placed on any surface or in any kind of package until the module and its hot parts have cooled down to ambient temperature.

Caution!

Switch off the system power before installing the module. Failure to follow this requirement can damage the module or entire system.

ESD Sensitive Equipment!

This product comprises electrostatically sensitive components. Please follow the ESD safety instructions to ensure module's operability and reliability:

- Use grounding equipment, if working at an anti-static workbench. Otherwise, discharge yourself and the tools in use before touching the sensitive equipment.
- Try to avoid touching contacts, leads and components.

Extra caution should be taken in cold and dry weather.

3.2 System Design Variants

CPC1301 is supplied with one of the optional heat sinking devices: heat-conducting plate (heatspreader), ribbed heatsinks, and combinations of ribbed heatsinks with cooling fan.

The heatsink or the heat-conducting plate is installed on the processor side of CPC1301 using six screws and thermal compound. The heatspreader is used in system designs with conductive heat sinking, for example to a metal outer housing. Ribbed heatsinks are used in a system case, where centralized forced air cooling is available. An optional cooling fan can be installed on the ribbed heatsink to further intensify heat dissipation. Power is supplied to the fan from the system power supply unit (fan connector on a carrier board).

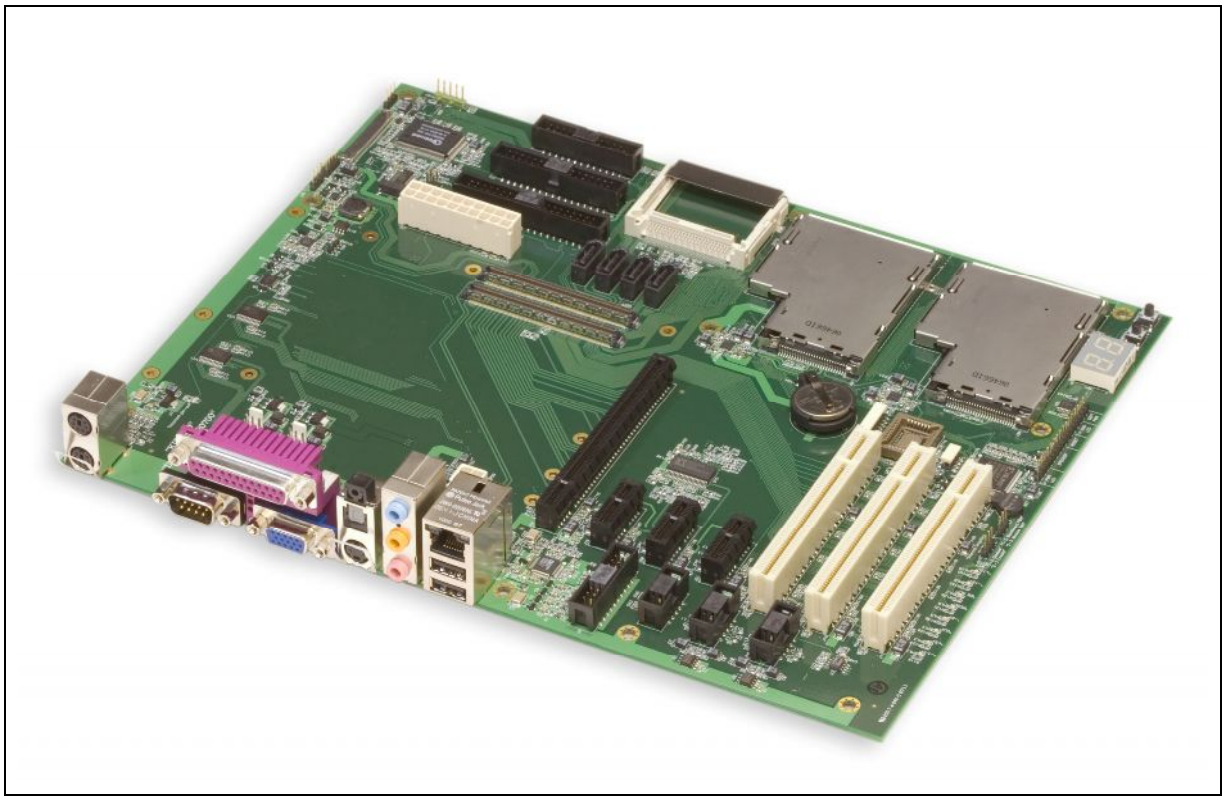
CPC1301 is installed on a carrier board using six stanoffs. Mounting the module on a carrier board, observe correct orientation of the module and ensure the complete engagement of the connectors.

TBA

3.3 Connection of Peripheral Devices: KIB1280

External devices are connected to CPC1301 via a carrier board for COM Express Type II pinout processor modules. Fastwel offers KIB1280, which can serve as an ATX development carrier board for CPC1301.

Figure 3-1: KIB1280 Carrier Board Appearance



The appearance may vary for different versions of the board.

KIB1280 carrier board provides access to the following interfaces and connectors:
VGA (RP D-Sub connector), S-Video (RP), LVDS, Gigabit Ethernet 10/100/1000-BaseT (one RJ45 RP connector), one x16 PCI Express, three x1 PCI Express connectors, three PCI headers, six USB 2.0 (two Type A RP connectors, four channels via onboard IDC headers), IDE UltraATA, four standard SATA connectors (two of them reserved), CF Type I/II socket with IDE interface, two RS232 COM ports (RP COM1 and onboard COM2), LPT (RP D-Sub) and FDD (IDC) standard connectors, two PS/2 RP connectors, two ExpressCard™ slots, Audio line in/out, MIC (RP), HD (5+1 out) Audio Connector, IrDA, LPC interface, SMBus, PLCC, two fan connectors, control&signalling interfaces and LEDs, ATX power supply header.

Please, the KIB1280 User Manual for details.

RP = Rear Panel connector

3.4 Installation of the Module

To install CPC1301, follow the instructions below.

1. Keep to the safety regulations of the Section 3.1 when performing the following operations.

Warning!

Failure to accomplish the following instruction may damage the module or result in incorrect system operation.

2. Ensure that the module configuration corresponds to the application requirements before installing. For information regarding the configuration of the CPC1301, refer to Chapter 4. For the installation of CPC1301 specific peripheral devices, and I/O devices refer to the appropriate sections in Chapter 3.
3. To install the CPC1301:
    1. Make sure that no power is connected to the system.
    2. Mount the module on a carrier board using all supplied screws.
    3. For CPC1301 versions with a ribbed heatsink with cooling fan - Connect the fan power cable to a carrier board connector. Provide conditions for sufficient cooling air flow. The fan air flow should be directed towards the heatsink.
    3. Connect the required external interfacing cables to the carrier board's connectors and make sure that the module and all connected cables are properly fixed.

The CPC1301 is now ready for operation. Please, refer to appropriate software, application, and system manuals to get further instructions.

3.5 Dismounting

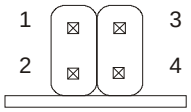
To unmount the module from the carrier board do the following:

1. When performing the next actions, keep to safety regulations of the Section 3.1. Pay special attention to the temperature of the heatsink or heatspreader!
2. Ensure that the system power is switched off before proceeding.
3. Disconnect the fan power cable (for version with a fan).
4. Unscrew the retaining screws. Do not touch the heatsink, since it can get very hot during operation.
5. Dispose of the module at your discretion. The module should not be placed on any surface or in any form of package until the board and the heatsink have cooled down to room temperature.

4 Configuration

The module has J1 and J5 jumper switches used to configure the system.

Figure 4-1: J1 Jumper Switch



Pins 1 and 2 closed – CMOS Reset.

Pins 3 and 4 open – five x1 PCI-E channels,
pins 3 and 4 closed – one x4 and one x1 PCI-E channel.

Figure 4-2: J5 Jumper Switch

Pins 1 and 2 closed – +5V_STBY voltage supplied via COM Express connector is used by the module. Pins 2 and 3 closed – +5V_STBY voltage is not used by the module.

With BIOS Setup utility it is possible to adjust the watchdog timer timeout and set parameters for I^2C controller. See sections 2.3 and 2.2 respectively for instructions. In BIOS Setup it is also possible to switch between SMBus and I^2C buses to be used for system parameters monitoring. The same utility is used to set operation mode for GPO2 and GPO3 signals, which are used either as output ports or as ALERT# and THERM# outlets of LM87 chip.

Warning!

All actions should be performed when the power is disconnected. Failure to follow this requirement can damage the module!

ESD Sensitive Equipment!

This product comprises electrostatically sensitive components. Please follow the ESD safety instructions to ensure module's operability and reliability:

- Use grounding equipment, if working at an anti-static workbench. Otherwise, discharge yourself and the tools in use before touching the sensitive equipment.
- Try to avoid touching contacts, leads and components.

5 Phoenix® BIOS Setup

The Phoenix® BIOS in your COM Express module is an adapted version of a standard BIOS for IBM PC AT-compatible personal computers equipped with Intel®x86 and compatible processors. The BIOS provides low-level support for the central processing, memory, and I/O system units.

With the help of BIOS Setup program, you can modify the BIOS configuration parameters and control the special features of your module. The Setup program is started by pressing the F2 key and offers a convenient menu interface to modify basic system configuration settings and switching between the subsystems operation modes. These settings are stored in a dedicated battery-backed memory, CMOS RAM, which keeps the information when the power is switched off.

To get the on-line help about the details of BIOS Setup program operation, please apply to the screen tips and the integrated help system.

6 Power Requirements

Absolute maximum input voltages presented in the table below must not be exceeded to guarantee that the CPC1301 is not damaged. The ranges for the input power voltages, within which the module is functional, are also presented.

Table 6-1: DC Input Voltage Ranges and Limits

Name	Power Voltage, V	Maximum Permitted Value, V	Absolute Limits, V	Recommended Range, V
Vcc_12V	+12	14.0	11.4 to 12.6	12.0 to 12.6
Vcc_5V_SBY	+5	5.25	4.75 to 5.25	5.0 to 5.25
Vcc_RTC	+3	3.3	2.0 to 3.3	3.0 to 3.3

Table 6-2: CPC1301 Maximum Consumption Current

Processor	Vcc_12V, A	Vcc_5V_SBY, A	Vcc_RTC in Power-off State, µA
Core 2 Duo 1.5 GHz, 667 MHz FSB	3.2	1.0	6.0
Core Duo 1.66 GHz, 667 MHz FSB	3.0	1.0	6.0
Celeron 1.06 GHz, 533 MHz FSB	2.1	1.0	6.0

Power supplies to be used with the CPC1301 should comply with these requirements.

7 Appendices

7.1 Supplementary Information

7.1.1 Related Standards and Specifications

The Fastwel's CPC1301 module comply with the requirements of the following standards:

Table 7-1: Related Standards

Type	Standard	Test Parameters
Temperature change	IEC 68-2-14-84	-40°C to 80°C (industrial range) 0°C to 70°C (commercial range) at RH=80%, non-condencing
CE: Emission	EN50081-1 (*TBA*)	–
CE: Immission	EN61000-6-2:2001	–
CE: Electrical safety	EN60950	–
Mechanical dimensions	IEEE 1101.10	–
Vibration (sinusoidal)	IEC60068-2-6-82; Fc	2 g / 10-500 Hz / 10 (acceleration / frequency range / test cycles per axis)
Single shock	IEC60068-2-27-87; Ea	50 g / 9 ms / 18 / 3 s (peak acceleration / shock duration / number of shocks / recovery time in seconds)
Multiple shock	IEC60068-2-29-87; Eb	25 g / 11 ms / 1000±10 / 1 s (peak acceleration / shock duration half sine / number of shocks / recovery time)

Important...

Some versions of the module may have the test results differing from the ones presented in the above table. For more information, please contact Fastwel's official representatives.

Information related to this product and its components can be found in the following specifications:

Table 7-2: Related Specifications

Product	Specification
COM Express module	PICMG COM.0. COM Express Module Base Specification
TBA	

7.1.2 Troubleshooting

In case the module does not start read this section carefully before calling to service center; the reason is not necessarily in hardware problem. Please, refer also to LED Indicators section in this document.

Table 7-3: Troubleshooting

Symptoms	Reason	Actions
The module does not start, HL1 LED is off.	+5 V standby voltage is not supplied to the module.	Check if J5 jumper switch is set correctly: • Set to the correct position, if it is not set at all. • If it is set to position 1-2, check presence of +5VSTBY voltage supplied from the carrier board. • If it is set to position 2-3, check presence of +12 V voltage supplied from the carrier board and PWR_OK signal at contact B24 of J7 connector.
The module does not start, HL1 LED is on, HL2 LED is off.	① +12 V power voltage is absent ② Onboard power sources are defective ③ Missing or broken FPGA firmware ④ PCIRST# signal is active	① Check presence of +12 V power voltage supplied from the carrier board, and PWR_OK signal at contact B24 of J7 connector. ② ③ ④ Apply to service center.
The module does not start, HL1 LED is on, HL2 LED is rapidly blinking (~8 Hz)	① BIOS is missing or damaged ② The module is damaged	① Check the correctness of BIOS selection at the carrier board (if there is choice). Check BIOS_DISABLE# signal at contact A34 of J7 connector. If this signal is active, the BIOS is loaded from LPC FWH installed at the carrier board. Start the module with the reserve BIOS, if this option is provided at the carrier board, and restore BIOS at the module. ② Apply to service center.
The module does not start, HL1 LED is on, HL2 LED is slowly blinking (~1 Hz), and the module beeps.	① BIOS execution did not reach OS loading via INT19h. ② BIOS is corrupt	① Diagnose BIOS loading process using POST using POST codes and beeps. If diagnostics and repair is not possible, apply to service center. ② Start the module with the reserve BIOS, if this option is provided at the carrier board, and restore BIOS at the module.

7.2 Useful Abbreviations, Acronyms and Short-cuts

Abbreviation	Meaning
BMC	Baseboard Management Controller
PM	Peripheral Management Controller
IPMI	Intelligent Platform Management Interface
IPMB	Intelligent Platform Management Bus
I^2C™	Inter Integrated Circuit Two-thread serial protocol, used in SMB and IPMI
KCS interface	Keyboard Controller Style interface Interface for communication between control software and BMC, similar to a keyboard controller interface
BT interface	Block Transfer interface Block transfer interface for communication between control software and BMC
DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory
SODIMM	Small Outline Dual In-Line Memory Module
ECC	Error Correction Code Data error correction technology used in memory modules
FWH	Firmware Hub Nonvolatile memory chip, part of Intel chipset, used for main and reserve BIOS copies in CPC1301
GMCH	Graphics and Memory Controller Hub
USB	Universal Serial Bus
LPC	Low Pin Count External devices communication interface
SMB	System Management Bus
UART	Universal Asynchronous Receiver-Transmitter
UHCI	Universal Host Controller Interface USB Host Controller Interface
EHCI	Enhanced Host Controller Interface (Universal Serial Bus specification)
UTP	Unshielded Twisted Pair
CRT-display	Cathode Ray Tube Display
PMC	PCI (Peripheral Component Interconnect) Mezzanine Card
CMC	Common Mezzanine Card
LVDS	Low Voltage Differential Signal Digital monitors communication specification
RTC	Real Time Clock
BIOS	Basic Input-Output System
PC	Personal Computer
PICMG	PCI Industrial Computer Manufacturers Group
AHA	Accelerated Hub Architecture GMCH and ICH communication bus specification
AGP	Accelerated Graphics Port
AGTL	Advanced Gunning Transceiver Logic PSB (Processor Side Bus) signal exchange specification
SMBus	System Management Bus
EEPROM	Electrically Erasable Programmable Read-Only Memory
NAND Flash	Not And (electronic logic gate) Flash memory specification
SSD	Solid State Disk
PLCC	Plastic Leaded Chip Carrier
RAMDAC	Random Access Memory Digital-to-Analog Converter

Abbreviation	Meaning
DAC	Digital-to-Analog Converter
DVMT	Dynamic Video Memory Technology
TTL	Transistor-Transistor Logic
ECP/EPP	Extended Capabilities Port / Enhanced Parallel Port Parallel port specifications
FDD	Floppy Disk Drive
EIDE	Enhanced Integrated Drive Electronics Mass storage devices interface
DMA	Direct Memory Access
PIO	Programmed Input/Output EIDE: Directly processor controlled data exchange
Rear I/O Board	Rear Input-Output Board Auxiliary interface board, which is connected to the cPCI backplane rear connectors
PWM output	Pulse-Width Modulation Cooling fan control technique
ESD	Electrostatically Sensitive Device Electrostatic Discharge
ACPI	Advanced Configuration and Power Interface
POST	Power On Self Test
cPCI	CompactPCI Industrial automation systems standard
EOS	Electrical Overstress
MDI	Media Dependent Interface Interface with connection type automatical detection