CPC801-01

EPIC
Intel Pentium M Based
Processor Module

Board Layout and Connectors

Rev. 001c E

April 2009

The product described in this manual is compliant to all related CE standards.

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Document name: CPC801-BLC-E
Document version: 001c E
Ref.doc.ver: –

Revision History

Rev. Index	Brief Description of Changes	Board Index	Date of Issue
001	Initial version	CPC801-01	June 2008
001a	Corrected audio connector	CPC801-01	March 2009
001b	Connectors table amended	CPC801-01	April 2009
001c	Delivery checklist and dimensions diagram added	CPC801-01	April 2009

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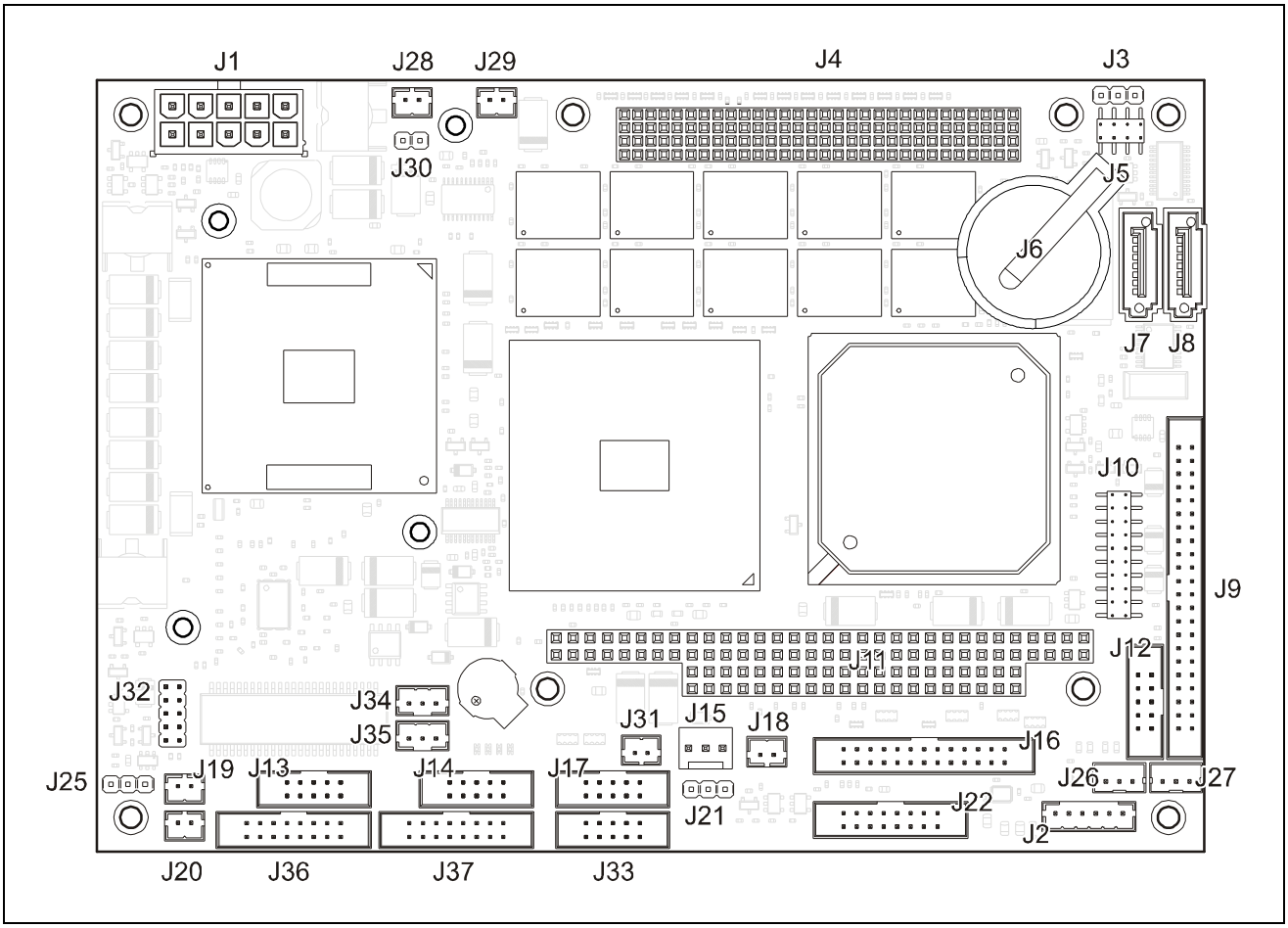
Table of Contents

1 Introduction

This document presents information on board layout, connectors description and pinouts of CPC801-01 EPIC processor module.

2 Board Layout

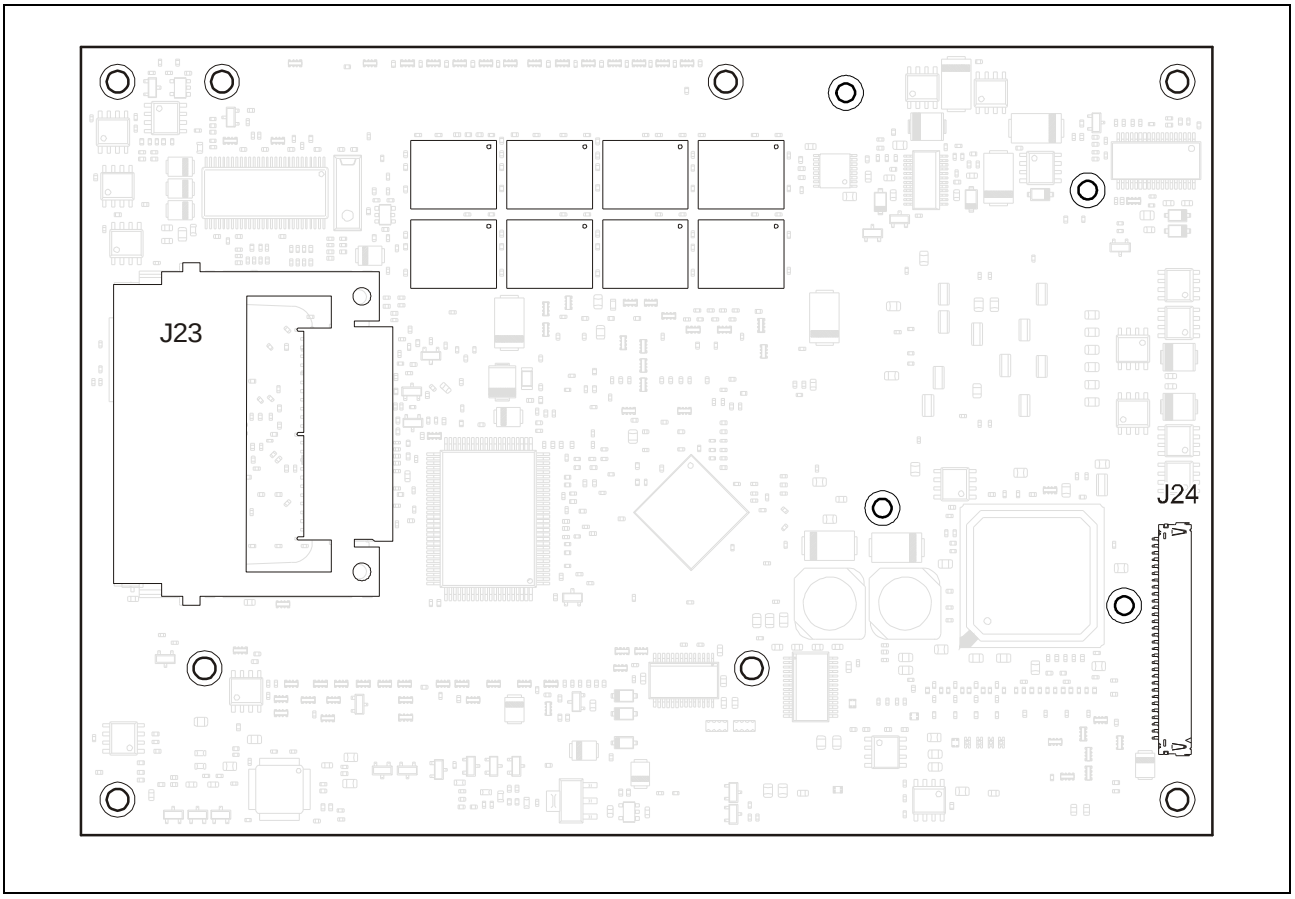
Figure 2-1: CPC801-01 Module Layout (Top View)



The layout may slightly vary for different versions of the module.

Heatsinks are not shown.

Figure 2-2: CPC801-01 Module Layout (Bottom View)



The layout may slightly vary for different versions of the module.

3 Delivery Checklist

CPC801-01 is basically supplied with the following accessories and cables:

1. CPC801-01 processor module with a heat spreader plate
2. 44-thread ribbon cable for 2.5" HDD connection
3. Header adapter from 44-contact 2 mm pitch to 40-contact 2.54 mm pitch (*)
4. One SATA angle data cable
5. One SATA power cable
6. AT and ATX adapter power cable
7. PS/2 adapter
8. PS/2 keyboard/mouse Y-cable
9. PC/104 module mounting kit:
   - Eight brass hexagon stud spacers 15 mm
   - Four screws, M3x8 DIN7985
   - Four hexagon nuts, M3 DIN934
   - Four serrated lock washers, Ø3 DIN6798 A
   - Four washers, Ø3 DIN125
10. PCI intermediate connector AMP 1375799-1
11. ISA intermediate connector AMP 1375795-2
12. One LVDS mating connector DF19G-30S-1C
13. 30 contacts for LVDS connector DF19A-3032SCFA
14. Three jumpers MJ-6
15. CD-ROM with documentation and service software
16. Antistatic bag
17. Consumer carton box

The list above can be expanded by ordering additional accessories as a ACS1 set:

1. Two RS232/RS485 adapter cables
2. Two USB adapter cables
3. LPT adapter
4. Two RS232 adapters
5. Two Ethernet cables
6. VGA adapter

Fan, heatsink and mounting accessories are included in ACS2 set:

1. Fan
2. Four stud spacers
3. Heatsink
4. The fan and heatsink mounting kit:
   - Four M2.5x8 screws DIN7985
   - Four M3x14 screws DIN7985
   - Four serrated lock washers, Ø2.5 DIN6798 A
   - Four serrated lock washers, Ø3 DIN6798 A
   - Four reduced washers Ø3 DIN433
   - Four washers Ø2.5 DIN125
   -

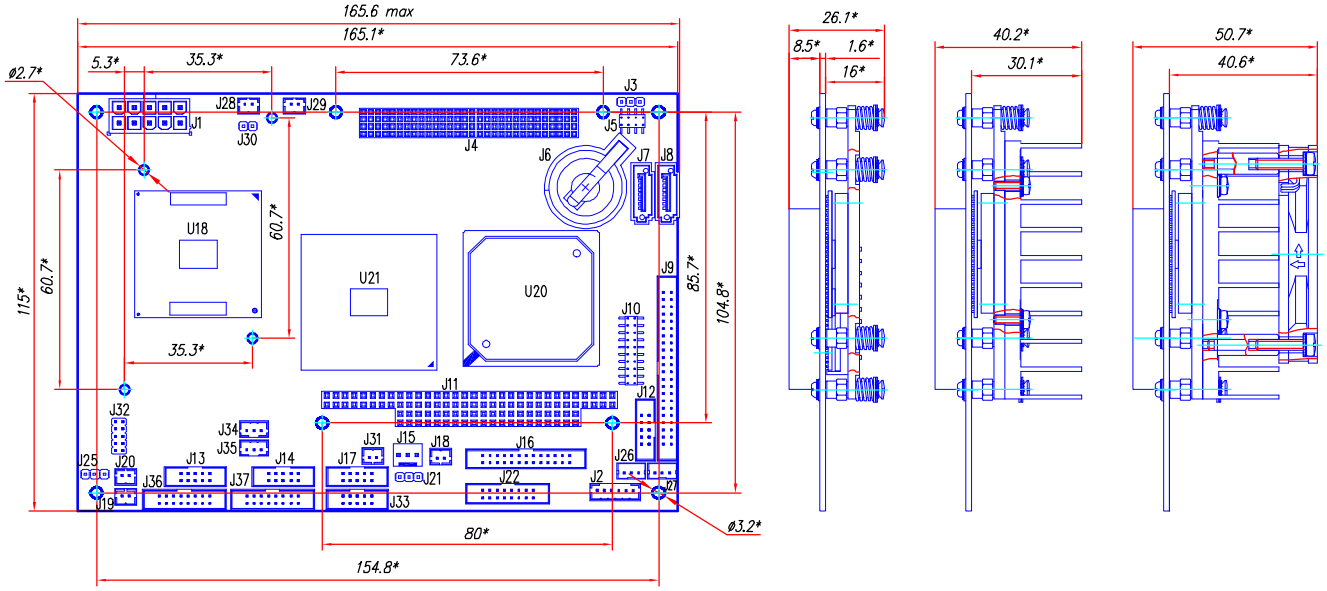
(*) Subject to change

Note:

Keep the antistatic bag and the original package at least until the warranty period is over. It can be used for future storage or warranty shipments.

4 Dimensions Diagram

Figure 4-1: CPC801-01 Dimensions Diagram



On the figure above:

A – Top view, heatspreader, heatsinks, and fan are not shown

B – Side view, basic configuration

C – Side view, heatsink installed

D – Side view, heatsink and fan installed

5 Connectors Description and Pinouts

5.1 Connectors List

Name	Pins	Type	Counterpart	Short Description
J1	10	–	–	Power
J2	6	MW-6M	MU-6F	PS/2
J3	3	3	3	PC/104-Plus VIO selector
J4	120	–	–	PC/104-Plus PCI
J5	8	IDC2-8	IDC2-8	JTAG
J6	2	–	–	Battery holder
J7	7	–	–	SATA1
J8	7	–	–	SATA2
J9	44	IDC2-44M	IDC2-44F	IDE
J10	20	IDC2-20	–	LPC
J11	104	–	–	PC/104 (ISA)
J12	10	PLD2-10	IDC2-10	COM3, COM4
J13	10	PLD2-10	BLD2-10	USB 1, 2
J14	10	PLD2-10	BLD2-10	USB 3, 4
J15	3	5045-03A	HU-3	Fan (Molex 5045-03A)
J16	26	PLD2-26	IDC2-26	LPT
J17	10	PLD2-10	IDC2-10	COM1
J18	2	MW-2M	MU-2F	SIO programmable LED
J19	2	MW-2M	MU-2F	SIO programmable LED
J20	2	MW-2M	MU-2F	FPGA LED
J21	3	PLS-3	–	Fan Voltage Selector
J22	16	PLD2-16	BLD2-16	VGA
J23	50	Type I/II	–	CompactFlash (*)
J24	30	–	–	LVDS (*)
J25	3	PLS-3	–	TFT Voltage Selector
J26	3	B3B-PH-K-S	MU-3F	Line Out
J27	3	B3B-PH-K-S	MU-3F	Line In / Mic In
J28	2	MW-2M	MU-2F	Soft Power
J29	2	MW-2M	MU-2F	Reset
J30	2	PLS-2	–	No SBY Switch
J31	2	MW-2M	MU-2F	IDE activity LED
J32	10	IDC2-10M	IDC2-10F	TFT Backlight Control
J33	10	PLD2-10	IDC2-10	COM2
J34	3	MW-3M	MU-3F	Gigabit Ethernet 1 LEDs
J35	3	MW-3M	MU-3F	Gigabit Ethernet 2 LEDs
J36	16	PLD2-16	BLD2-16	Gigabit Ethernet 2
J37	16	PLD2-16	BLD2-16	Gigabit Ethernet 1

(*) Located on the bottom side

5.2 PC/104 and PC/104-Plus Connectors

Figure 5-1: PC/104 J11 Connector Contacts Layout

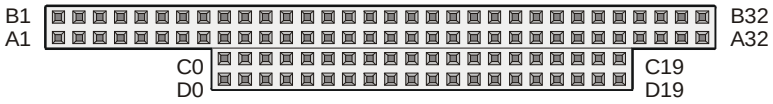


Table 5-1: PC/104 J11 (Rows A and B) Connector Contacts Designation

Pin #	Signal	In/Out	Pin #	Signal	In/Out
A1	/IOCHK	–	B1	GND	Ground
A2	SD7	In/Out	B2	RESETDRV	Out
A3	SD6	In/Out	B3	+5V	Power
A4	SD5	In/Out	B4	IRQ9	In
A5	SD4	In/Out	B5	-5V	–
A6	SD3	In/Out	B6	DRQ2	In
A7	SD2	In/Out	B7	-12V	Power
A8	SD1	In/Out	B8	/ENDXFR	In
A9	SD0	In/Out	B9	+12V	Power
A10	IOCHRDY	In	B10	KEY	–
A11	AEN	Out	B11	/SMEMW	Out
A12	SA19	Out	B12	/SMEMR	Out
A13	SA18	Out	B13	/IOW	Out
A14	SA17	Out	B14	/IOR	Out
A15	SA16	Out	B15	/DACK3	Out
A16	SA15	Out	B16	DRQ3	In
A17	SA14	Out	B17	/DACK1	Out
A18	SA13	Out	B18	DRQ1	In
A19	SA12	Out	B19	/REFRESH	Out
A20	SA11	Out	B20	SYSCLK	Out
A21	SA10	Out	B21	IRQ7	In
A22	SA9	Out	B22	IRQ6	In
A23	SA8	Out	B23	IRQ5	In
A24	SA7	Out	B24	IRQ4	In
A25	SA6	Out	B25	IRQ3	In
A26	SA5	Out	B26	/DACK2	Out
A27	SA4	Out	B27	TC	Out
A28	SA3	Out	B28	BALE	Out
A29	SA2	Out	B29	+5V	Power
A30	SA1	Out	B30	OSC	Out
A31	SA0	Out	B31	GND	Ground
A32	GND	Ground	B32	GND	Ground

Table 5-2: PC/104 J11 (Rows C and D) Connector Contacts Designation

Pin #	Signal	In/Out	Pin #	Signal	In/Out
C0	GND	Ground	D0	GND	Ground
C1	/SBHE	Out	D1	/MEMCS16	In
C2	LA23	Out	D2	/IOCS16	In
C3	LA22	Out	D3	IRQ10	In
C4	LA21	Out	D4	IRQ11	In
C5	LA20	Out	D5	IRQ12	In
C6	LA19	Out	D6	IRQ13	In
C7	LA18	Out	D7	IRQ14	In
C8	LA17	Out	D8	/DACK0	Out
C9	/MEMR	Out	D9	DRQ0	In
C10	/MEMW	Out	D10	/DACK5	Out
C11	SD8	In/Out	D11	DRQ5	In
C12	SD9	In/Out	D12	/DACK6	Out
C13	SD10	In/Out	D13	DRQ6	In
C14	SD11	In/Out	D14	/DACK7	Out
C15	SD12	In/Out	D15	DRQ7	In
C16	SD13	In/Out	D16	+5V	Power
C17	SD14	In/Out	D17	/MASTER	In
C18	SD15	In/Out	D18	GND	Ground
C19	KEY	–	D19	GND	Ground

Note:

In tables above:

"–" - Not used;
"Power" - The power is supplied to the module installed into a crate
In/Out column shows the data transfer direction for a processor module being the bus master.

Figure 5-2: PC/104-Plus J4 Connector Contacts Layout

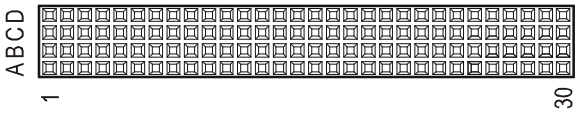
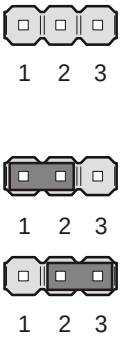


Table 5-3: PC/104-Plus J4 Connector Contacts Designation

Pin	A	B	C	D
1	GND/5.0V_KEY2	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	/C/BE0	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	/C/BE1	AD15	+3.3V
9	/SERR	GND	Reserved	PAR
10	GND	/PERR	+3.3V	Reserved
11	/STOP	+3.3V	/LOCK	GND
12	+3.3V	/TRDY	GND	/DEVSEL
13	/FRAME	GND	/IRDY	+3.3V
14	GND	AD16	+3.3V	/C/BE2
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	/C/BE3	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	/REQ0	GND	/REQ1	VI/O
24	GND	/REQ2	+5V	/GNT0
25	/GNT1	VI/O	/GNT2	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	/INTD	+5V	/RST
29	+12V	/INTA	/INTB	/INTC
30	-12V	Reserved	Reserved	GND/3.3V_KEY

Figure 5-3: J3 PC/104-Plus VIO Selector Positions



The jumper should be removed only if the module is powered via J4 connector from a PC/104-Plus power supply module. In case the processor module receives power through J1 connector, the jumper must be installed in one of the two positions, described below.

Contacts 1-2 closed, +5 V power is supplied to PCI interface I/O buffers

Contacts 2-3 closed, +3.3 V is supplied.

5.3 VGA CRT Connector

Figure 5-4: VGA-CRT J22 Connector

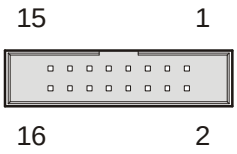


Table 5-4: SVGA J22 Connector Pinout

Pin Number	Signal	Pin Number	Signal
1	RED	9	GND
2	+5V FUSE	10	HSYNC
3	GREEN	11	GND
4	GND	12	VSYNC
5	BLUE	13	GND
6	NC	14	DDC CLOCK
7	NC	15	GND
8	DDC DATA	16	NC

5.4 LVDS Connector

Figure 5-5: J24 LVDS Connector

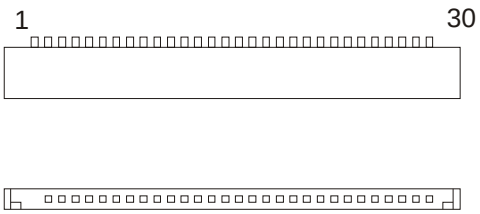
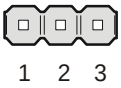


Table 5-5: J24 LVDS Connector Pinout

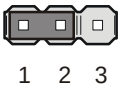
Contact #	Signal	Description	In/Out
27	LA_DATA_P0	Differential Signal Positive	–
28	LA_DATA_N0	Differential Signal Negative	–
25	LA_DATA_P1	Differential Signal Positive	–
26	LA_DATA_N1	Differential Signal Negative	–
23	LA_DATA_P2	Differential Signal Positive	–
24	LA_DATA_N2	Differential Signal Negative	–
19	LA_DATA_P3	Differential Signal Positive	–
20	LA_DATA_N3	Differential Signal Negative	–
21	LA_CLK_P	Differential Clock Positive	–
22	LA_CLK_N	Differential Clock Negative	–
15	LB_DATA_P0	Differential Signal Positive	–
16	LB_DATA_N0	Differential Signal Negative	–
13	LB_DATA_P1	Differential Signal Positive	–
14	LB_DATA_N1	Differential Signal Negative	–
11	LB_DATA_P2	Differential Signal Positive	–
12	LB_DATA_N2	Differential Signal Negative	–
7	LB_DATA_P3	Differential Signal Positive	–
8	LB_DATA_N3	Differential Signal Negative	–
9	LB_CLK_P	Differential Clock Positive	–
10	LB_CLK_N	Differential Clock Negative	–
1, 2, 3, 4	VDD	Panel Power 5V or 12V	–
5, 6, 17, 18, 29, 30	GND	Signal ground	–

5.5 TFT Panel Power Voltage Selection

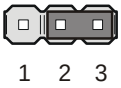
Figure 5-6: J25 TFT Panel Power Voltage Selector



J25 is a standard 3-pin header (PLS-3) used for TFT power voltage (V_{DD}) selection. It is located on the top side of the module. Figures below presents explanation of its jumper positions.



Pins 1-2 closed: +5 V power is supplied to a panel



Contacts 2-3 closed: +12 V is supplied

Attention!

Take due care selecting TFT panel power voltage!

Wrong setting can result in a damage to the panel. Please, apply to specifications of a panel for correct voltage level.

5.6 Digital Panel Backlight Control

Figure 5-7: J32 TFT Backlight Control Connector

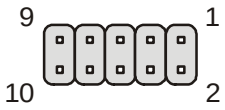


Table 5-6: J32 Backlight Control Connector Pinout

Pin #	Signal	Description	In/Out
1	+12V	+12V for voltage selector	–
2	Backlight Control Voltage Selector	Connecting this pin with pin #1 or pin #4 allows to select voltage for pin#6	–
3	GND	Signal ground	–
4	+5V	+5V for voltage selector	–
5	Backlight Enable	Backlight On/Off function, 5V-level	Out
6	Backlight Control Out	Backlight brightness control output. Voltage defined by input level on pin #2	Out
7	NC	–	–
8	NC	–	–
9	LVDS DDC CLK	DDC clock signal	Out
10	LVDS DDC DATA	DDC data signal	In/Out

5.7 Audio Connectors

Figure 5-8: Onboard CRIMP Audio Connectors: J26 and J27

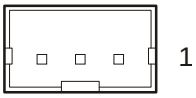


Table 5-7: J26 LineOut Connector Pinout

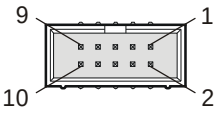
Pin #	Signal	Description	In/Out
1	Right	Right channel output	Out
2	GND	Analog ground	–
3	Left	Left channel output	Out

Table 5-8: J27 Line Input or Microphone Input Connector Pinout

Pin #	Signal	Description	In/Out
1	Right	Right channel input / microphone bias	In/Out
2	GND	Analog ground	–
3	Left	Left channel input / microphone Input	In

5.8 Serial Interfaces

Figure 5-9: IDC2-10 Serial Connectors J17, J12, and J33



According to "Intel 6300ESB I/O Controller HUB (ICH) Specification update", COM1 and COM2 interfaces have limited functionality due to unexpected behavior of serial port interrupt enable register.

Below is an abstract from this document:

2. Behavior of Serial Port Interrupt Enable Register

Problem: The Serial Port Interrupt Enable Register (IER) bit 1 [3f9h] (Transmit Data request Interrupt Enable) will not change status if the bit has been set previously.

Implication: Will not cause an interrupt if the register bit has been set already. This hinders the serial ports from being fully 100 percent 16550 compatible.

Workaround: Customers may be able to implement a BIOS workaround to clear out the bit IER bit 1 to '0' before programing the bit to '1'.

Status: No fix.

Thus serial ports integrated in South bridge are compatible with standard UART 16550, except the following registers:

1. Changed designation of bits 4 and 5 of IER (Interrupt Enable Register)
2. Changed designation of bits 6 and 7 of FCR (FIFO Control Register)

For details see "IntelR 6300ESB I/O Controller Hub Datasheet. February 2004", pages 667-671.

Table 5-9: Serial Port Connectors J17 (COM1) and J33 (COM2) Pinout

Pin	RS232	Pin	RS232
1	DCD#	6	DSR#
2	RXD	7	RTS#
3	TXD	8	CTS#
4	DTR#	9	RI#
5	GND	10	GND

Table 5-10: Serial Ports Connector J12 (COM3 and COM4) Pinout

Pin	Signal	Pin	Signal
1	RS485_PORT1_D	6	RS485_PORT2_D#
2	RS485_PORT1_D#	7	TTL_PORT1_RXD
3	GND	8	TTL_PORT1_TXD
4	+5V	9	TTL_PORT2_RXD
5	RS485_PORT2_D	10	TTL_PORT2_TXD

Note:

The RS485 interfaces (COM3 and COM4) provide for support of up to 256 network segments. In case the module is supposed to serve as a terminal network device, it is necessary to mention this fact when ordering the module. The required SMT 120 ohm terminal resistors will be installed at the factory.

5.9 USB Connectors

Figure 5-10: USB1 to USB4 IDC2-10 Connectors J13 and J14

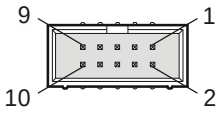


Table 5-11: USB1 to USB4 (J13 and J14) Pinouts

J13 USB Ports 1&2

Pin Number	Signal
1	+5V
2	+5V
3	DATA1-
4	DATA2-
5	DATA1+
6	DATA2+
7	GND
8	GND
9	NC
10	NC

J14 USB Ports 3&4

Pin Number	Signal
1	+5V
2	+5V
3	DATA3-
4	DATA4-
5	DATA3+
6	DATA4+
7	GND
8	GND
9	NC
10	NC

5.10 Parallel Port Interface

Figure 5-11: LPT Connector J16

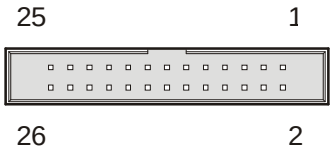


Table 5-12: LPT Connector J16 Pinout

Pin #	LPT1 Signals	Pin #	LPT1 Signals
1	STROBE#	14	GND
2	AFD#	15	DATA6
3	DATA0	16	GND
4	ERR#	17	DATA7
5	DATA1	18	GND
6	INIT#	19	ACK#
7	DATA2	20	GND
8	SELECT_IN#	21	BUSY
9	DATA3	22	GND
10	GND	23	PE
11	DATA4	24	GND
12	GND	25	SELECT
13	DATA5	26	NC

5.11 Gigabit Ethernet

Figure 5-12: Gigabit Ethernet Connectors J36, J37

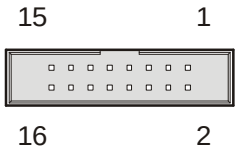


Table 5-13: Gigabit Ethernet Connectors J36, J37 Pinouts

J37 LAN1		J36 LAN2	
Pin	**Signal**	**Pin**	**Signal**
1	TRXD0+	1	TRXD0+
2	TRXD0-	2	TRXD0-
3	AGND	3	AGND
4	AGND	4	AGND
5	TRXD1+	5	TRXD1+
6	TRXD1-	6	TRXD1-
7	AGND	7	AGND
8	AGND	8	AGND
9	TRXD2+	9	TRXD2+
10	TRXD2-	10	TRXD2-
11	AGND	11	AGND
12	AGND	12	AGND
13	TRXD3+	13	TRXD3+
14	TRXD3-	14	TRXD3-
15	AGND	15	AGND
16	AGND	16	AGND

Figure 5-13: Gigabit Ethernet LEDs Connectors J34, J35

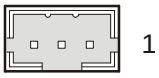


Table 5-14: Gigabit Ethernet LEDs Connectors J34, J35 Pinouts

Pin #	Function
1	ACTIVITY#
2	+3.3V
3	LINK#

5.12 IDE Connector

Figure 5-14: J9 IDE HDD Connector

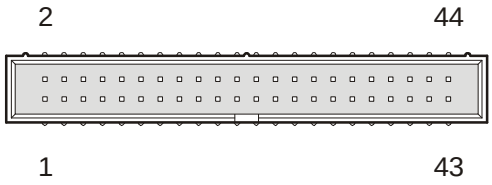


Table 5-15: Standard EIDE HDD Connector J9 Pinout

Pin Number	Signal	Function	In/Out
1	/RESET	Reset HD	Out
2	GND	Ground signal	–
3	DD7	HD data 7	In/Out
4	DD8	HD data 8	In/Out
5	DD6	HD data 6	In/Out
6	DD9	HD data 9	In/Out
7	DD5	HD data 5	In/Out
8	DD10	HD data 10	In/Out
9	DD4	HD data 4	In/Out
10	DD11	HD data 11	In/Out
11	DD3	HD data 3	In/Out
12	DD12	HD data 12	In/Out
13	DD2	HD data 2	In/Out
14	DD13	HD data 13	In/Out
15	DD1	HD data 1	In/Out
16	DD14	HD data 14	In/Out
17	DD0	HD data 0	In/Out
18	DD15	HD data 15	In/Out
19	GND	Ground signal	–
20	–	–	–
21	DRQ	DMA request	In
22	GND	Ground signal	–
23	/IOW	I/O write	Out
24	GND	Ground signal	–
25	/IOR	I/O read	Out
26	GND	Ground signal	–
27	/IOCHRDY	I/O channel ready	In
28	GND	Ground signal	–
29	/DACK	DMA Ack	Out
30	GND	Ground signal	–
31	IRQ	Interrupt request	In
32	/CS16	–	–
33	DA1	Address 1	Out
34	–	ATA66/100 Detect	–
35	DA0	Address 0	Out
36	DA2	Address 2	Out
37	/CS1	Select Register #1	Out
38	/CS3	Select Register #3	Out
39	DASP	IDE Activity	Out
40	GND	Ground signal	–
41	+5V	+5V	–
42	+5V	+5V	–
43	GND	Ground signal	–
44	–	–	–

Figure 5-15: J31 IDE Activity LED Connector

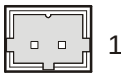


Table 5-16: J31 IDE Activity LED Connector Pinout

Pin Number	Function
1	LED Anode
2	LED Cathode

5.13 SerialATA Connectors

Figure 5-16: SATA Connectors J7, J8

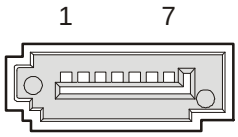


Table 5-17: SATA Connectors (J7, J8) Pinout

Contact Number	Function
1	GND
2	TXP
3	TXN
4	GND
5	RXN
6	RXP
7	GND

5.14 CompactFlash Socket

Figure 5-17: CompactFlash Type I/II Socket J23

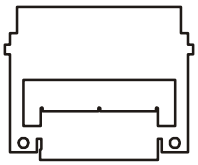


Table 5-18: CompactFlash Socket J23 Pinout

Pin Number	Signal	Function	In/Out
1	GND	Ground signal	–
2	D03	Data 3	In/Out
3	D04	Data 4	In/Out
4	D05	Data 5	In/Out
5	D06	Data 6	In/Out
6	D07	Data 7	In/Out
7	IDE_CS0	Chip select 0	Out
8	GND	–	–
9	GND	–	–
10	GND	–	–
11	GND	–	–
12	GND	–	–
13	3.3 V	3.3 V power	–
14	GND	–	–
15	GND	–	–
16	GND	–	–
17	GND	–	–
18	A02	Address 2	Out
19	A01	Address 1	Out
20	A00	Address 0	Out
21	D00	Data 0	In/Out
22	D01	Data 1	In/Out
23	D02	Data 2	In/Out
24	IOCS16	–	–
25	CD2	–	–
26	CD1	–	–
27	D11	Data 11	In/Out
28	D12	Data 12	In/Out
29	D13	Data 13	In/Out
30	D14	Data 14	In/Out
31	D15	Data 15	In/Out
32	IDE_CS1	Chip select 1	Out
33	VS1	–	–
34	IORD	I/O read	Out
35	IOWR	I/O write	Out
36	3.3 V	3.3 V power	–
37	INTRQ	Interrupt	In
38	3.3 V	3.3 V power	–
39	CSEL	Master/Slave	Out
40	VS2	–	–
41	Reset	Reset	Out
42	IORDY	I/O ready	In
43	INPACK	DMA Request	Out
44	REG	DMA Acknowledge	–
45	ACTIVE	IDE Activity	–
46	PDIAG	DMA Mode Detect	–
47	D08	Data 08	In/Out
48	D09	Data 09	In/Out
49	D10	Data 10	In/Out
50	GND	–	–

5.15 PS/2 Keyboard/Mouse Interface

Figure 5-18: PS/2 Connector J2

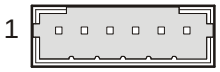


Table 5-19: PS/2 Connector J2 Pinout

Pin Number	Signal	Pin Number	Signal
1	VCC 5 V	4	MDAT
2	KBDDAT	5	MCLK
3	KBDCLK	6	GND

5.16 Power Supply

Figure 5-19: External Power Supply Connector J1

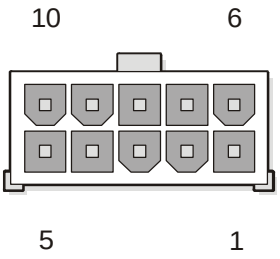


Table 5-20: EPIC Power Supply Connector J1 Pinout

Pin Number	Signal	Pin Number	Signal
1	PS_ON	6	+5VSB
2	GND	7	+5V
3	GND	8	+5V
4	+12V	9	–12V
5	+3.3V	10	GND

Figure 5-20: J30 Power Supply Type Selector Positions

If an external power supply does not support control functions, contacts 1-2 should be closed.

Open position of the jumper (default) corresponds to an ATX external power supply with control functions support.

Note:

If an external power supply without control functions support is used, it is allowed to leave contact 6 of J1 power connector not connected.

5.17 Fan Connector

Figure 5-21: Fan Connector J15

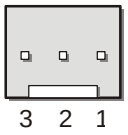
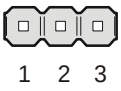


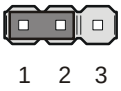
Table 5-21: J15 Fan Connector Pinout

Pin Number	Function
1	FANTACH
2	FANCTL (+5 V / +12 V)
3	GND

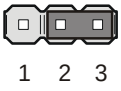
Figure 5-22: Fan Voltage Selector J21 Positions



Off



Contacts 1-2 closed,
+12 V is supplied to the pin "2" of the fan connector.



Contacts 2-3 closed,
+5 V is supplied to the pin "2" of the fan connector.

5.18 Soft Power and Reset Connectors

Figure 5-23: Soft Power (J28) and Reset (J29) Connectors

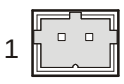


Table 5-22: SoftPower (J28) Connector Pinout

Pin Number	Signal
1	PWR Button
2	GND

Table 5-23: Reset (J29) Connector Pinout

Pin Number	Signal
1	–
2	In/Out

5.19 JTAG and LPC Connectors

Figure 5-24: JTAG Header J5

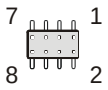


Table 5-24: JTAG J5 Connector Pinout

Pin Number	Signal	Pin Number	Signal
1	M_RESET#	5	GND
2	TDI	6	TCK
3	GND	7	VCC
4	TDO	8	TMS

Figure 5-25: LPC Header J10

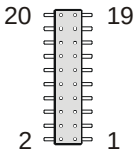


Table 5-25: LPC J10 Connector Pinout

Pin Number	Signal	Pin Number	Signal
1	LAD0	11	LDRQ#
2	PCIRST#	12	PME#
3	LAD1	13	LPD#
4	GND	14	GND
5	LAD2	15	+3_3V
6	PCICLK	16	FWH_INIT#
7	LAD3	17	BOOT
8	GND	18	+5V
9	LFRAME#	19	WRITE_EN
10	SERIRQ	20	GND

5.20 LED Indicators

Figure 5-26: LED Connectors (J18, J19, J20, and J31)

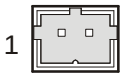


Table 5-26: LEDs Connectors by Function

Name	Function
J18	General purpose LED controlled by Super I/O
J19	General purpose LED controlled by Super I/O
J20	General purpose LED controlled by FPGA Xilinx XC3S200
J31	IDE activity

Table 5-27: LEDs Connectors Pinouts

J18 SIO LED2

Pin	Function
1	LED Anode
2	LED Cathode

J19 SIO LED1

Pin	Function
1	LED Anode
2	LED Cathode

J20 FPGA LED

Pin	Function
1	LED Anode
2	LED Cathode

J31 IDE Activity LED

Pin	Function
1	LED Anode
2	LED Cathode