Fastwel

CPC501

6U CompactPCI Intel Pentium M CPU Board

User Manual

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CPC501

6U CompactPCI
Intel Pentium M Based
Processor Module

User Manual

Rev. 0.03a E

June 2006

The product described in this manual is compliant to all related CE standards.

Product Title: CPC501
Document name: CPC501 User Manual
Manual version: 0.03a E

Revision Record

Rev. Index	Short Description	Product Index	Date
0.01	Initial version	CPC501	June 2004
0.02c	Appendix A "Rear I/O module" added Chapter 5 changed Information on versions of the CPC501 and RIO581 added Minor corrections made	CPC50101 CPC50102	June 2005
0.02e	Changes in Gigabit/Fast Ethernet functionality added Information on RIO585 added	CPC501## RIO581 RIO585	November 2005
0.03	Total text reassertion	Same	February 2006
0.03a	Watchdog timer section reworked, multiple text corrections	Same	June 2006

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Notation Conventions

Warning, ESD Sensitive Device!

This symbol draws your attention to the information related to electro static sensitivity of your product and its components. To keep product safety and operability it is necessary to handle it with care and follow the ESD safety directions.

Warning!

This sign marks warnings about hot surfaces. The surface of the heatsink and some components can get very hot during operation. Take due care when handling, avoid touching hot surfaces!

Caution: Electric Shock!

This symbol warns about danger of electrical shock (> 60 V) when touching products or parts of them. Failure to observe the indicated precautions and directions may expose your life to danger and may lead to damage to your product.

Warning!

Information marked by this symbol is essential for human and equipment safety.
Read this information attentively, be watchful.

Note...

This symbol and title marks important information to be read attentively for your own benefit.

General Safety Precautions

This product was developed for fault-free operation. Its design provides conformance to all related safety requirements. However, the life of this product can be seriously shortened by improper handling and incorrect operation. That is why it is necessary to follow general safety and operational instructions below.

Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.

Warning!

When handling this product, special care must be taken not to hit the heatsink (if installed) against another rigid object. Also, be careful not to drop the product, since this may cause damage to the heatsink, CPU or other sensitive components as well.

Please, keep in mind that any physical damage to this product is not covered under warranty.

Note:

This product is guaranteed to operate within the published temperature ranges and relevant conditions. However, prolonged operation near the maximum temperature is not recommended by Fastwel or by electronic chip manufacturers due to thermal stress related failure mechanisms. These mechanisms are common to all silicon devices, they can reduce the MTBF of the product by increasing the failure probability. Prolonged operation at the lower limits of the temperature ranges has no limitations.

Caution, Electric Shock!

Before installing this product into a system and before installing other devices on it, always ensure that your mains power is switched off.

Always disconnect external power supply cables during all handling and maintenance operations with this module to avoid serious danger of electrical shock.

Unpacking, Inspection and Handling

Please read the manual carefully before unpacking the module or mounting the device into your system. Keep in mind the following:

ESD Sensitive Device!

Electronic modules and their components are sensitive to static electricity. Even a non-perceptible by human being static discharge can be sufficient to destroy or degrade a component's operation! Therefore, all handling operations and inspections of this product must be performed with due care, in order to keep product integrity and operability:

- Preferably, unpack or pack this product only at EOS/ESD safe workplaces. Otherwise, it is important to be electrically discharged before touching the product. This can be done by touching a metal part of your system case with your hand or tool. It is particularly important to observe anti-static precautions when setting jumpers or replacing components.
- If the product contains batteries for RTC or memory back-up, ensure that the module is not placed on conductive surfaces, including anti-static mats or sponges. This can cause short-circuit and result in damage to the battery and other components.
- Store this product in its protective packaging while it is not used for operational purposes.

Unpacking

The product is carefully packed in an antistatic bag and in a carton box to protect it against possible damage and harmful influence during shipping. Unpack the product indoors only at a temperature not less than +15°C and relative humidity not more than 70%. Please note, that if the product was exposed to the temperatures below 0°C for a long time, it is necessary to keep it at normal conditions for at least 24 hours before unpacking. Do not keep the product close to a heat source.

Following ESD precautions, carefully take the product out of the shipping carton box. Proper handling of the product is critical to ensure correct operation and long-term reliability. When unpacking the product, and whenever handling it thereafter, be sure to hold the module preferably by the front panel, card edges or ejector handles. Avoid touching the components and connectors.

Retain all original packaging at least until the warranty period is over. You may need it for shipments or for storage of the product.

Initial Inspection

Although the product is carefully packaged, it is still possible that shipping damages may occur. Careful inspection of the shipping carton can reveal evidence of damage or rough handling. Should you notice that the package is damaged, please notify the shipping service and the manufacturer as soon as possible. Retain the damaged packing material for inspection.

After unpacking the product, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socketed components), contact Fastwel's official distributor from which you have purchased the product for additional instructions. Depending on the severity of the damage, the product may even need to be returned to the factory for repair. DO NOT apply power to the product if it has visible damage. Doing so may cause further, possibly irreparable damage, as well as result in a fire or electric shock hazard.

If the product contains socketed components, they should be inspected to make sure they are seated fully in their sockets.

Handling

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

In order to keep Fastwel's warranty, you must not change or modify this product in any way, other than specifically approved by Fastwel or described in this manual.

Technical characteristics of the systems in which this product is installed, such as operating temperature ranges and power supply parameters, should conform to the requirements stated by this document.

Retain all the original packaging, you will need it to pack the product for shipping in warranty cases or for safe storage. Please, pack the product for transportation in the way it was packed by the supplier.

When handling the product, please, remember that the module, its components and connectors require delicate care. Always keep in mind the ESD sensitivity of the product.

Three Year Warranty

Fastwel Co. Ltd. (Fastwel), warrants that its standard hardware products will be free from defects in materials and workmanship under normal use and service for the currently established warranty period. Fastwel's only responsibility under this warranty is, at its option, to replace or repair any defective component part of such products free of charge.

Fastwel neither assumes nor authorizes any other liability in connection with the sale, installation or use of its products. Fastwel shall have no liability for direct or consequential damages of any kind arising out of sale, delay in delivery, installation, or use of its products.

If a product should fail through Fastwel's fault during the warranty period, it will be repaired free of charge. For out of warranty repairs, the customer will be invoiced for repair charges at current standard labor and materials rates.

Warranty period for Fastwel products is 36 months since the date of purchase.

The warranty set forth above does not extend to and shall not apply to:

1. Products, including software, which have been repaired or altered by other than Fastwel personnel, unless Buyer has properly altered or repaired the products in accordance with procedures previously approved in writing by Fastwel.
2. Products which have been subject to power supply reversal, misuse, neglect, accident, or improper installation.

Returning a product for repair

1. Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization.
2. Attach a failure inspection report with a product to be returned in the form, accepted by customer, with a description of the failure circumstances and symptoms.
3. Carefully package the product in the antistatic bag, in which the product had been supplied. Failure to package in antistatic material will VOID all warranties. Then package the product in a safe container for shipping.
4. The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer.

Chapter 1

Introduction

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1 Introduction

1.1 Overview

The CPC501 is an advanced 64-bit / 33 MHz 6U CompactPCI system controller module. To get the details about the CompactPCI, a wide spread industrial standard, please refer to PCI and CompactPCI specifications. The Internet site of the PCI Industrial Computer Manufacturers Group (PICMG) provides information related to these standards (http://www.picmg.org/).

The CPC501 processor module is specially developed for use in highly integrated systems for performance-demanding industrial applications. This is one of the main reasons to employ Intel® Pentium® M processors family. The CPC501 basic configuration utilizes the processor in the μFCPGA478M package operating at the processor speed of up to 2 GHz and a Processor Side Bus (PSB) running at 400 MHz. The chipset of the CPC501 includes the Intel 82855GME GMCH and ICH4 I/O Controller Hub.

The module includes up to 1 GB of Double Data Rate (DDR) memory. It is installed in one 200-pin SODIMM socket and is operated at 333 MHz.

System features include two Gigabit Ethernet ports, one Fast Ethernet port (82559-style), and one PMC slot to support mezzanine PCI devices (option). The module also includes a built-in Intel 2D/3D Graphics accelerator with up to 64 MB memory shared with system for enhanced graphics performance with a VGA CRT-display interface and with TFT LVDS interface.

The CPC501 is equipped with the following PC interfaces including: five USB 2.0 ports, four COM ports, two EIDE ATA100 interfaces, one CompactFlash Type I socket, one Floppy port, one parallel port, and, besides, rear I/O CompactPCI bus connectors J3, J4, and J5.

The module supports one configurable 64-bit, 33 MHz, hotswap CompactPCI interface. In the system master slot the bridge is enabled, and if installed in a peripheral slot, the CPC501 is isolated from the CompactPCI-bus.

One of the most important features of the CPC501 is its support of the PICMG CompactPCI Packet Switching Backplane Specification 2.16. When installed in a backplane which supports packet switching, the CPC501 can communicate via both of its Gigabit Ethernet interfaces with other peripherals or a system master which also support packet switching.

CPC501 employs the thoroughly selected components for embedded industrial systems to ensure their long term availability.

The module is compatible with the Microsoft® DOS v.3.30 – 6.22, Microsoft® Windows® CE, 2000, Windows® XP, QNX v.4.20, 6.0, and Linux® operating systems.

Some of the CPC501's main features are:

- Intel® Pentium® M processor up to 2.0 GHz in µFCPGA package
- Up to 2 MB L2 on-die cache running at CPU speed
- 82855GME GMCH and 82801DB ICH4 chipset
- 400 MHz processor system bus
- Up to 1 GB of DDR SDRAM memory running at 333 MHz (PC2700) with ECC
- PCI local bus: 32-bit / 33 MHz
- CompactPCI-bus interface: 64-bit / 33 MHz
- Integrated 3D high performance VGA controller
  - 64 MB memory shared with system
  - CRT-display support with resolutions of up to 2048 x 1536 pixels at 16 bits and 75 Hz
  - LVDS interface support via Rear I/O
- Four serial ports
- Five USB 2.0 ports
- PS/2 keyboard and mouse interface
- Floppy disk interface
- Parallel port
- Two Gigabit Ethernet interfaces
  - 10Base-T, 100Base-TX, and 1000Base-T
  - Independently software configurable for cPCI backplane packet switching (PICMG® 2.16, R1.0), for CPC501 front panel or for RIO58x front panel interfacing.
- One integrated Fast Ethernet interface (82559-style), 82562ET, 10Base-T, 100Base-TX
- PMC interface (32-bit) with rear I/O support and opening on front panel.
  Standard PMC modules can be installed on CPC50102 version only.
- Two EIDE Ultra ATA/100 interfaces
- Onboard CompactFlash Type I socket
- Optional socket for 2.5" hard disk or flash-disk on board (CPC50101 only)
- Hardware Monitor (LM82)
- Watchdog timer
- Additional counters and timers integrated in the ICH4
- Real-time clock with battery backup
- Two 512 KB on-board FWHs
- 4HP, 6U CompactPCI form-factor
- Hotswap capability: as system controller or as peripheral device
- Supports PICMG® Packet Switching Backplane Specification v.2.16
- Rear I/O on J3, J4 and J5
- Passive heatsink solution
- Phoenix® BIOS

1.2 CPC501 Versions

At the present time, the module is manufactured in two basic versions:

Version	On-board 2.5" HDD or flash-disk capability	Standard PMC modules capability
CPC50101	+	–
CPC50102	–	+

Moreover, the CPC501 configuration is flexible. The customer can choose necessary configuration options using the following template:

1	–	2	–	3	–	4	–	5

1 Basic product name:

CPC501

2 Basic configurations:

01 On-board 2.5" HDD or flash-disk capability

02 Standard PMC modules capability

3 Processor:

P1.6 Pentium M 1.6 GHz, 400 MHz FSB

P1.8 Pentium M 1.8 GHz, 400 MHz FSB

4 Operating temperature range:

I Industrial, -40°C to +85°C

C Commercial, 0°C to 70°C

5 Other options:

SODIMM Memory Module

\SODIMM512 512 MB DDR SDRAM SODIMM, Industrial Range

\SODIMM512C 512 MB DDR SDRAM SODIMM, Commercial Range

\SODIMM1024 1024 MB DDR SDRAM SODIMM, Industrial Range

\SODIMM1024C 1024 MB DDR SDRAM SODIMM, Commercial Range

CompactFlash Module

\CF128 128 MB CompactFlash card, industrial

\CF256 256 MB CompactFlash card, industrial

\CF512 512 MB CompactFlash card, industrial

\CF1024 1024 MB CompactFlash card, industrial

Installed 2.5" Disk Drive (for CPC50101 only)

\HDD20 2.5" Hard Disk Drive, 20 GB

\FFD2048 2.5" Flash Disk, 2048 MB

Coating

\COATED Protective Coating

Examples:

CPC501 – 01 – P1.8 – I \SODIMM1024

6U CompactPCI Pentium M SBC, FFD 32 MB, VGA, 2x Gigabit Ethernet
2.5" HDD Site
Pentium M 1.8 GHz, 400 MHz FSB
Industrial operating temperature range, -40°C to +85°C
1024 MB DDR SDRAM SODIMM, industrial range

CPC501 – 01 – P1.6 – C \SODIMM512C \CF128 \HDD20 \COATED

6U CompactPCI Pentium M SBC, FFD 32 MB, VGA, 2x Gigabit Ethernet
Pentium M 1.6 GHz, 400 MHz FSB
Commercial operating temperature range, 0°C … +70°C
512 MB DDR SDRAM SODIMM, commercial range
128 MB CompactFlash card
HDD 2.5'' 20 GB
Protective coating

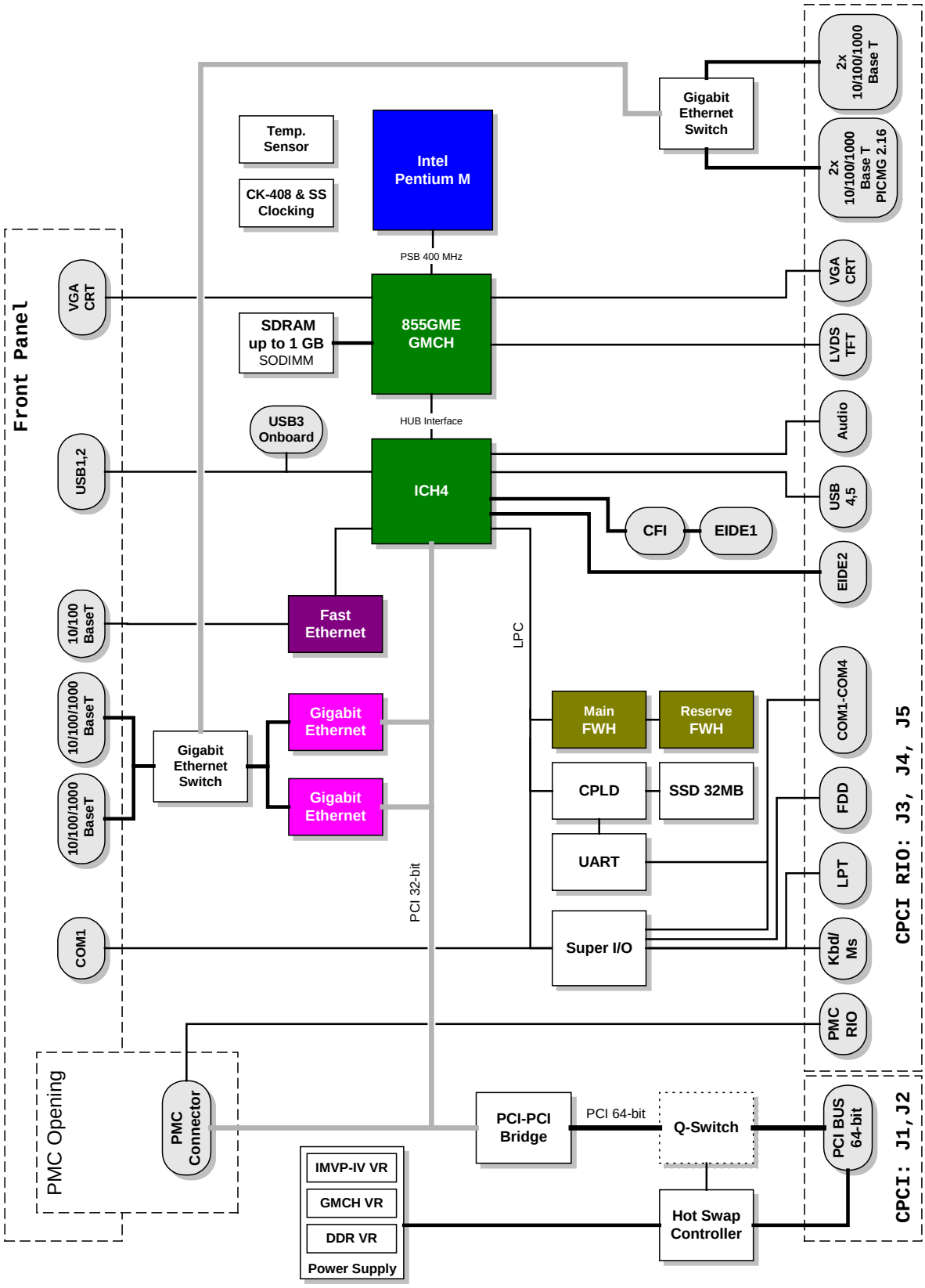
Other configuration options are available upon request.

1.3 CPC501 Diagrams

The diagrams in this section give visual information about the CPC501 module design, its appearance, connectors and components layout. The diagrams may not reflect insignificant differences between the CPC501 versions.

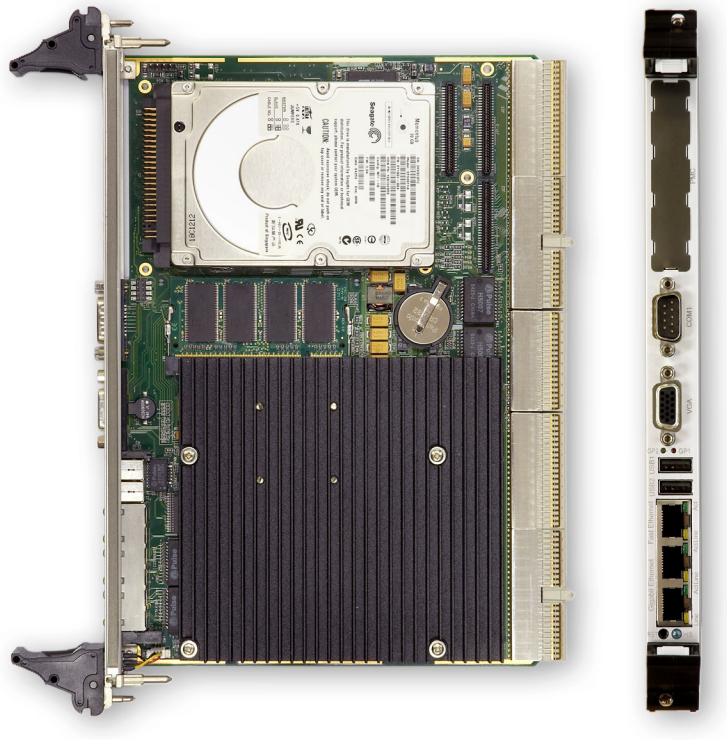
1.3.1 Block Diagram

Figure 1-1: CPC501 Block Diagram



1.3.2 Module Appearance

Figure 1-2: CPC501 Module Appearance: Top, Front Views

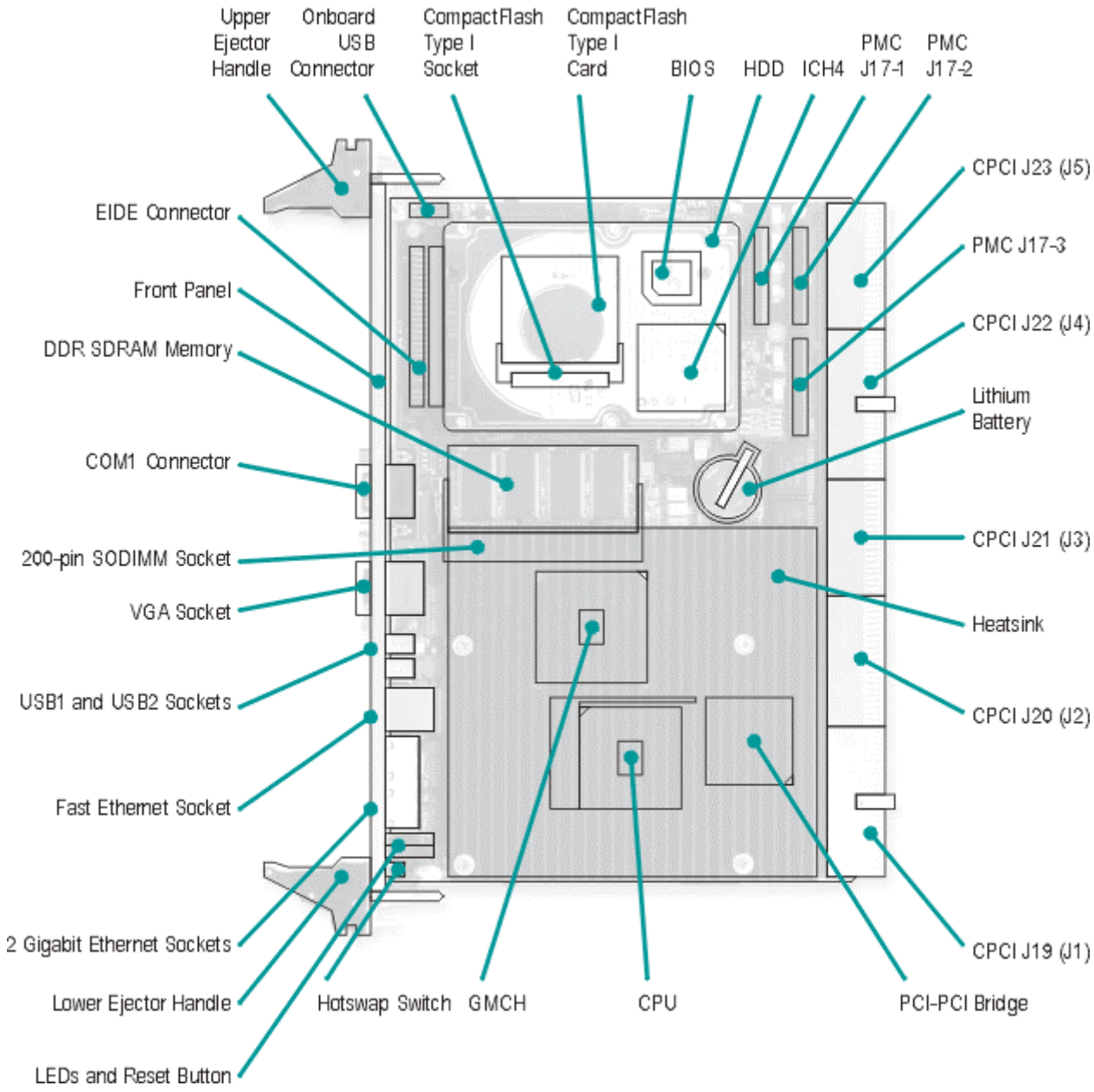


The appearance may slightly differ for various versions of the module.

This figure shows CPC50101 with a 2.5" HDD installed on-board.

1.3.3 Components and Connectors Layout

Figure 1-3: CPC501 Module Layout (Top View)

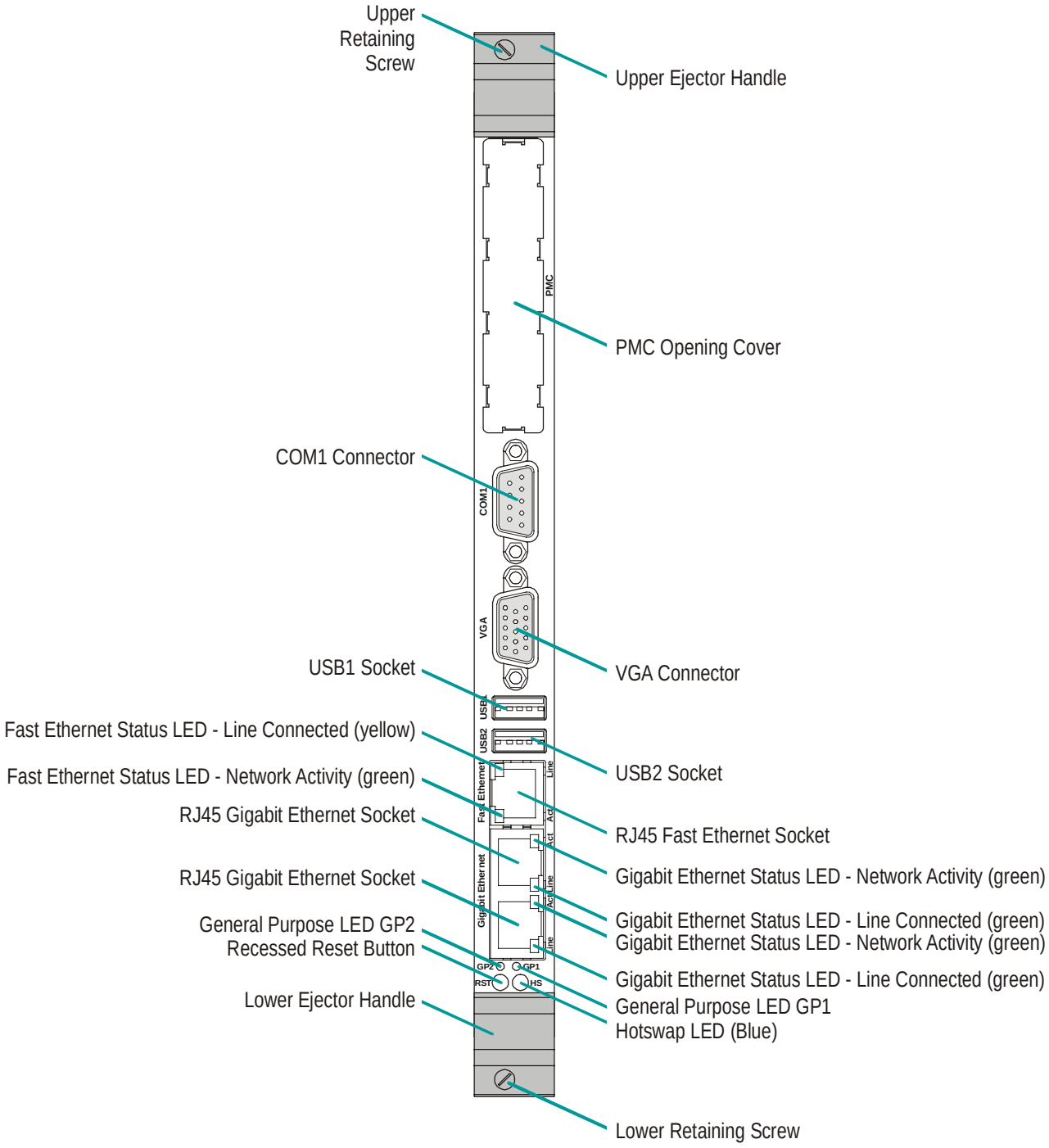


The layout may differ for various versions of the module:

CPC50101 – has J5 connector, does not have J17-3 PMC connector;
CPC50102 – does not have J5 EIDE connector, has J17-1, J17-2 u J17-3

1.3.4 Front Panel

Figure 1-4: CPC501 Front Panel (4HP)



The layout may slightly differ for various versions of the module.

1.4 Technical Characteristics

1.4.1 Processor, Memory and Chipset

CPU

Pentium® M Processor

- Up to 2.0 GHz
- Up to 2 MB L2 on-die cache
- 400 MHz PSB
- Supports SpeedStep® III for low power mode
- 478-pin μFCPGA package

Memory

Main memory:

- Up to 1 GB of DDR SDRAM memory in a 200-pin SODIMM socket, ECC support
- Memory frequency: 333 MHz (PC2700)

Flash memory:

- Two flash memory Firmware Hubs (part of the CPC501 chipset) used for BIOS storage
- One 256 byte EEPROM for storing CMOS data when operating without battery
- Up to 32 MB solid-state disk (NAND flash memory) with Fastwel file system

Chipset

Intel® 82855GME Graphics Memory Controller Hub (GMCH)

- Support for a single Pentium M family microprocessors
- 64-bit AGTL/AGTL+ based System Bus interface at 400 MHz
- 64-bit System Memory interface, optimized for DDR SDRAM memory at 333 MHz with additional 8-bits for ECC
- Integrated 2D/3D Graphics and H/W Motion Compensation Engines
- Integrated DAC, 350 MHz

Intel® 82801DB I/O Controller Hub (ICH4)

- PCI Rev. 2.2 compliant with support for 33 MHz/32-bit PCI bus
- Enhanced DMA controller, interrupt controller, and timer
- Integrated Ultra ATA100 IDE controller
- USB 2.0 host interface
- One integrated 82559-type LAN controller
- System Management Bus
- Power management logic support
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Additional timers

1.4.2 Interfaces

CompactPCI Bus Interface

Compliant with CompactPCI Specification PICMG® 2.0 R3.0

- System master operation
- 64-bit / 33 MHz master interface
- 3.3V / 5.0V compatible (default configuration is 5.0V)
- When the CPC501 is operated in a peripheral slot, the CPCI-bus is electrically isolated from the CPC501

Serial Ports

COM1 and COM2:

- COM1 – RS-232, 9-pin D-sub connector on the CPC501 front panel
- COM2 – TTL level signals, available at the Rear I/O only
- Dual UART, 16C550 compatible

COM3 and COM4:

- 16C550 compatible UARTs
- Rear I/O availability only
- TTL level signals

USB Interface

Five USB 2.0 ports supporting UHCI and EHCI:

- Two USB type A connectors on the front panel
- Two rear I/O interfaces
- One onboard port connector

Parallel Port

Multi-Mode™ parallel port, SPP/ECP/EPP compatible

- Standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bidirectional parallel port
- Rear I/O interfacing only

Gigabit Ethernet

Two 10/100/1000 Mb/s Gigabit Ethernet interfaces based on the Intel 82541EI Ethernet PCI bus controller.

- Two RJ45 connectors on the front panel
- Support for two Gigabit Ethernet channels independently software configurable for cPCI backplane packet switching (PICMG® 2.16, R1.0), for CPC501 front panel or for RIO58x front panel interfacing.
- Automatic mode recognition
- Automatic cabling configuration recognition
- Cabling requirement: Category 5, UTP, four-pair cabling

Fast Ethernet

One 10Base-T/100Base-TX Fast Ethernet port integrated within the ICH4 controller (82559-type):

- One RJ45 connector on the CPC501 front panel
- Automatic mode recognition
- Cabling requirement: Category 5, UTP, two-pair cabling.

VGA interface

Built-in Intel 2D/3D high performance graphics accelerator

- Supports resolutions of up to 2048 x 1536, 16 bit at 75 Hz refresh rate
- Hardware motion compensation for software MPEG2 and MPEG4 decoding
- Video memory up to 64 MB shared with system
- 15-pin D-sub VGA CRT-display connectors available at CPC501 and at RIO58x front panels

Keyboard and Mouse

Super I/O support for a keyboard and a mouse:

- Rear I/O interfacing for both keyboard and mouse
- Standard PS/2 keyboard connector (6-pin), requires adaptor (Y-cable) to connect regular mouse and a keyboard simultaneously

Mass Storage

EIDE Ultra ATA/100/66/33

- Two channels
- Up to four devices (hard disks or CD-ROMs)
- Optional 50-pin, 2.0 mm, female connector for mounting a 2.5" disk drive onboard (CPC50101 only)

CompactFlash:

- CompactFlash type I on-board socket (true IDE mode), supports type I CompactFlash cards

Floppy Disk:

- Rear I/O interfacing only
- Supports 5.25 or 3.5 inch floppy drives
- 1.44 or 2.88 MB, 3.5 inch floppy disks

PMC

CMC / PMC P1386 / Draft 2.4a compliant mezzanine interface:

- J17-1 (Jn1), J17-2 (Jn2), and J17-3 (Jn4) PCI mezzanine connectors for standard PMC modules (CPC50102 only)
- 32-bit / 33 MHz master interface
- 3.3 V compatible
- Rear I/O supported through CompactPCI connector J23 (J5)

Rear I/O

To optimize cabling rear I/O interface is available via the J21 (J3), J22 (J4), and J23 (J5) connectors in combination with the rear I/O modules RIO58x.

- J21 (J3): floppy, COM3, keyboard, mouse, USB4, secondary EIDE port and PICMG 2.16 support.
- J23 (J5): VGA-CRT, two Ethernet channels without LEDs, USB5, COM1, COM2, COM4, control signals, PMC rear I/O connectivity
- J22 (J4): parallel port, AC-link, LVDS (RIO58101)

1.4.3 Control and Monitoring

Thermal Management

Processor is protected from overheating by the following means:

- The processor frequency and core voltage are automatically reduced when processor die temperature reaches the limit specified in BIOS Setup
- Internal processor temperature control unit initiates CPU shut down when the processor die is overheated
- Processor die temperature monitor helps to keep the processor temperature within prescribed limits
- Custom designed heatsinks provide efficient heat energy dissipation

Temperature Monitor

LM82 hardware monitor is used for supervision of the on-die CPU temperature and the board surface temperature

Hotswap Compatibility

The CPC501 supports System Master hotswap and application dependent hotswap when used in a peripheral slot.

When used as a System Master the CPC501 supports individual clocks for each slot and ENUM signal handling in accordance with the PICMG 2.1 R2.0 Hotswap specification.

LEDs

System status:

- GP1 (red): Programmable
- GP2 (green): Programmable
- HS: blue: Hotswap control

Gigabit Ethernet status (1 and 2):

- Line (green): Line connected
- Act (green): Network activity

Fast Ethernet status:

- Line (yellow): Line connected
- Act (green): Network activity

Switches

Reset switch (RST):

- Initiates cold restart of CPC501
- The button is recessed to prevent accidental activation (can be activated using long thin object)

Hotswap switch:

- When activated initiates safe power off
- Integrated as part of the lower ejector handle

1.4.4 General

Mechanical

6U, 4HP, CompactPCI compliant form factor

Dimensions: 233.35 mm × 160 × 20.32 mm

Module Weight: 835 g with 2.5” hard disk and without mezzanine boards, 725 g without HDD

Power Supply

2 A @ +3.3 V; 6 A @ +5 V; 0.1 A @ +12 V (without external devices)

See Chapter 6 for details on supply voltages and power supply requirements

Temperature Ranges

Operational:	CPC501-01-xxx-I, CPC501-02- xxx-I	-40°C ... +85°C
	CPC501-01- xxx-C, CPC501-02- xxx-C	0°C ... +70°C
Storage:		-55°C ... +85°C

Humidity

5% to 95% RH, non-condensing

Battery

3.0 V lithium battery for RTC in a battery holder. Use PANASONIC BR2032 or compatible

1.4.5 Software

Software BIOS

Flash memory based enhanced Phoenix® BIOS has the following features:

- BIOS boot support for USB keyboards
- Software enable/disable function for the Rear I/O, Ethernet, and COM ports configuration
- Plug&Play capability

Operating Systems

Supported operating systems:

- Microsoft® Windows® 2000, XP, CE
- Microsoft® DOS v. 3.x – 6.x
- Linux®
- QNX®

1.5 Information for Application Developers

Please, consider the following information when developing applications using the CPC501.

Hotswap Compatibility

When operated as a system master, the CPC501 supports individual clocks for each slot and ENUM signal handling is in compliance with the CompactPCI Hot Swap Specification PICMG 2.1 R2.0. When operated in a peripheral slot the CPC501 supports basic Hotswap.

System Slot / System Master Functionality

The CPC501 is designed to for use as a system master board whereby it can support up to 7 peripheral boards with 64-bit and 33 MHz. It may, however, be operated in a peripheral slot. In this case it does not support the CompactPCI-bus interface.

Peripheral Slot Functionality

When installed in a peripheral slot, the CPC501 is electrically isolated for the CompactPCI-bus. It receives power from the backplane and supports rear I/O and, if the system supports it, packet switching (in this case up to two channels of Gigabit Ethernet).

1.6 Delivery Checklist

The CPC501 supplied set includes:

1. CPC501 processor module
2. 2.5" HDD mounting kit (for installation of a 2.5” HDD, for CPC50101 only):
   - HDD mounting adapter with connectors
   - Four screws (M3)
3. CD-ROM with documentation and service software
4. Antistatic bag
5. Consumer package

Note:

Keep the antistatic bag and the original package at least until the warranty period is over. It can be used for future storage or warranty shipments.

1.7 System Expansion

1.7.1 PMC Modules

The CPC501 has one PMC interface. This 32-bit, 33 MHz interface supports a wide range of available standard PMC modules and provides a convenient way to adapt the CPC501 for various applications. PMC modules can be installed only on CPC50102, which has three PMC connectors and no J5 EIDE connector.

1.7.2 Rear I/O Modules: RIO581 and RIO585

Rear I/O modules expand the I/O capability of the CPC501. They are installed from the back of the system crate in line with the processor module. For detailed information concerning RIO581 and RIO585 modules, please, refer to Appendix A or to http://www.fastwel.com/

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Chapter 2

Detailed Description

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2 Detailed Description

2.1 Processor, Memory and Chipset

2.1.1 Processor

The CPC501 module is based on the Intel® Pentium® M processor in the μFCPGA478M package. It combines high performance and low power consumption. Its enhanced performance characteristics are provided by a newly designed processor core with an integrated 64 KB L1 and 2048 KB L2 cache.

The Intel® Pentium® M processor supports the Intel SpeedStep® enhanced technology to control power consumption and processor die temperature by switching the processor core voltage and frequency between several modes without resetting the system. This allows the system to maintain maximum performance rate at different temperature conditions.

Important performance features of the Intel Pentium M Processor also include Intel NetBurst™ Micro-Architecture, consisting of a 400 MHz processor system bus, Hyper Pipelined Technology, new Execution Trace Cache, Rapid Execution Engine, and 144 new Streaming SIMD instruction extensions.

2.1.2 System Memory

The CPC501 has one on-board 200-pin DDR SODIMM socket. The module supports a maximum of 1 GB. There is no need to make any additional settings, since the installed memory is automatically detected by the system. The SODIMM memory modules to be used with this module must conform to PC2700, and PC SPD (Serial Presence Detect) DDR SDRAM memory specifications.

The memory module is not included in the basic configuration.

2.1.3 Chipset

The Intel® 855GME chipset consists of the following devices:

- 82855GME Graphics and Memory Controller Hub (GMCH) with Accelerated Hub Architecture (AHA) bus
- 82801DB I/O Controller Hub 4 (ICH4) with AHA bus
- Two 82802AB Firmware Hubs (FWH)

The GMCH provides the interfaces for the Pentium® M microprocessor, the memory bus, the AGP 4x bus in the case of an external graphics controller installed. It includes a high performance 2D/3D built-in graphics accelerator. The ICH4 serves as a central controller for I/O peripherals, such as the PCI, EIDE, USB 2.0, LAN and Audio ports. The Firmware Hubs (FWH) provide the non-volatile storage of BIOS.

North Bridge

The 855GME Graphics Memory Controller Hub (GMCH) provides interfaces with the central processor, with the DDR SDRAM system memory, and interface to high performance internal graphics or AGP interface for an external VGA controller. It also provides a hub link interface to the ICH4.

The 855GME is optimized for the Intel® Pentium® M family of microprocessors. The chipset supports a PSB frequency of 400 MHz with AGTL+ signaling. For single processor systems the single ended AGTL termination is supported. It supports 32-bit addressing for using up to 4 GB memory address space. The 855GME includes a system memory controller with a 64-bit interface with ECC. The chipset supports up to PC2700 DDR SDRAMs for use as system memory.

When running in internal graphics mode, high performance video capabilities of the 855GME are supported by a 2D/3D graphics accelerator and H/W Motion Compensation engines for software MPEG2 decoding. The internal graphics controller allows connection of a standard CRT display.

South Bridge

The ICH4 is a multifunctional I/O Controller Hub that provides the interface to the PCI Bus and such PC interfaces, as UltraDMA 100/66/33, USB 2.0 host interface, LPC interface, FWH Flash BIOS interface, LAN interface and an AC'97 digital audio. The ICH4 communicates with the host controller directly via a dedicated hub link interface.

I/O Controller Hub features are:

- PCI 2.2 interface with eight IRQ inputs
- UltraDMA 100 EIDE controller with Bus Master capability
- Three USB controllers, up to six USB 2.0 ports
- Hub interface for 855GME
- LPC interface
- Integrated 82559-type LAN controller
- AC'97 2.1 audio interface
- RTC controller
- Additional timers

2.2 Internal Peripherals

The following internal peripherals are available on the CPC501 module:

2.2.1 Flash Memory

There are four flash devices available - one is used for the BIOS storage, one is reserved (not used in current version), one is a NAND flash memory (SSD) device and one is a CompactFlash card in the socket.

2.2.1.1 Flash Disk

The CPC501 has an on-board solid-state disk (up to 32 MB of NAND flash-memory) with Fastwel file system for storing user programs and data.

2.2.1.2 Compact Flash

The CPC501 has a standard Compact Flash type I socket, which can accept CompactFlash memory card for use as a disk drive.

2.2.2 Hot-Swap Controller

The purpose of the hot-swap controller is to provide safe disconnection of power when the module is removed from the system and to ensure correct power-up when the module is installed into the system crate.

As a part of the hot-swap controller, a precision voltage monitoring circuit automatically shuts down CPC501 when it detects a drop in voltage below the acceptable operating limit of 4.725 V for the 5 V line and below 3.0 V for the 3.3 V line, or in the event of a power failure of the processor DC/DC converter.

2.2.3 Timers

The CPC501 is equipped with the following timers:

- **Real-Time Clock**

The ICH4 contains a real-time clock compatible with MC146818A with 256 bytes of CMOS RAM. The RTC features include timekeeping with alarm function and 100-year calendar, as well as programmable periodic interrupt. A coin-cell battery powers the real-time clock and CMOS memory.

- **Counters/Timers**

Three PC/AT 8254-style counters/timers are available on the CPC501.

Watchdog Timer

The ICH4 includes an additional programmable timer (TCO timer), which prevents system hang-ups during the start-up process (for example, in case of mistakes in BIOS) and during normal operation. After the first time-out period is over, it generates the SMI# signal, which may start the software hang-up recovery subroutine. After the second timeout comes to an end, the "Reset" signal is issued to recover the system from the hardware hang-up state.

The timeout period is set in BIOS Setup program or by the user program.

2.2.3.1 Watchdog Timer Operation Details

The watchdog timer is switched on by setting the TCO_TMR_HLT bit of the TCO1_CNT register to 0 and is stopped by setting this bit to 1.

The timer is initially loaded with the value from the TCO1_TMR register and begins countdown. After the first timeout is over, the SECOND_TO_STS bit is set and if the TCO_EN bit of the SMI_EN register is set, SMI interrupt is issued. Along with it, the timer is again loaded with the value from the TCO1_TMR register and begins countdown for the second time.To prevent system reset, the SMI handler, if it is enabled in BIOS Setup, clears the SECOND_TO_STS bit. After the second timeout period is over and the SECOND_TO_STS bit is still set, the PCI_RESET signal is issued and the system is rebooted.

In case the TCO_TMR_HLT bit is cleared and either the SMI Handler is disabled or the TCO_EN bit is cleared, then to prevent system reset the user program should either reload the watchdog timer by writing any value to the TCO_RLD register within the first timeout period, or clear the SECOND_TO_STS bit by writing 1 to it before the second timeout period is over.

Please refer to Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet for the complete description of registers. The description of TCO timer operation related registers is quoted below.

TCO Timer Registers Description

TCO1_RLD – *TCO Timer Reload and Current Value Register*

I/O Address:	1060h	Attribute:	R/W
Default Value:	0000h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout. Bits 7:6 will always be 0.

TCO1_TMR – *TCO Timer Initial Value Register*

I/O Address:	1061h	Attribute:	R/W
Default Value:	0004h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7:6	Reserved
5:0	Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0h–3h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and this allows timeouts ranging from 2.4 seconds to 38 seconds.

TCO2_STS – *TCO2 Status Register*

I/O Address:	1066h	Attribute:	R/WC
Default Value:	0000h	Size:	16 bit
Lockable:	No	Power Well:	Resume

Bit	Description
15:2	Reserved
1	SECOND_TO_STS – R/WC. 0 = This bit is cleared by writing a 1 to the bit position or by a RSMRST#. 1 = The ICH4 sets this bit to a 1 to indicate that the TCO timer timed out a second time (probably due to system lock). If this bit is set, then the ICH4 will reboot the system after the second timeout. The reboot is done by asserting PCIRST#. NOTE: BIOS should always clear this bit before executing SMBus reads and writes.
0	Reserved

TCO1_CNT – *TCO1 Control Register*

I/O Address:	1068h	Attribute:	R/W, R/WC, R/W-Special
Default Value:	0000h	Size:	16 bit
Lockable:	No	Power Well:	Core

Bit	Description
15:12	Reserved
11	TCO Timer Halt (TCO_TMR_HLT) – R/W. 0 = The TCO Timer is enabled to count. 1 = The TCO Timer will halt. It will not count, and thus cannot reach a value that will cause an SMI# or set the SECOND_TO_STS bit. When set, this bit will prevent rebooting.
10:0	Reserved

SMI_EN – *SMI Control and Enable Register*

I/O Address:	1030h	Attribute:	R/W, WO, R/W-Special
Default Value:	0000h	Size:	32 bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

Bit	Description
31:14	Reserved
13	TCO_EN – R/W. 0 = Disables TCO logic generating an SMI#. 1 = Enables the TCO logic to generate SMI#.
12:0	Reserved

2.2.4 Local SMBus Devices

The CPC501 incorporates a System Management Bus to access several system monitoring and control devices via a two-wire I^2C™ bus interface. The following table presents functions and addresses of onboard SMBus devices.

Table 2-1: SMBus Devices

№	SMB Address	Device
1	0D2H	ICS950201 System clock generator
2	0D4H	TFT Suspend Generator ICS91718
3	0A0H	SPD EEPROM Module
4	9CH	LM82 Temperature Sensor
5	0ACH, 0AEH	2×256 Bytes User EEPROM

2.2.4.1 Temperatures Monitoring

The integrated LM82 temperature sensor monitors the processor and board surface temperatures to make sure that the system is operating at a safe temperature. On request, LM82 can report the current processor and board temperatures to the software responsible for the module operation mode.

2.2.4.2 Serial EEPROM

A serial EEPROM is implemented into the hot-swap controller (SMH4042). This nonvolatile memory is used for storage of CMOS data and some of the service parameters for emergency recovery.

2.2.5 Reset

Reset sources include the front panel and Rear I/O push-button switches, and CompactPCI backplane reset input (PRST). The CPC501 responds to any of these sources' signal by initializing local peripherals.

2.2.6 Battery

The CPC501 utilizes a 3.0 V lithium battery for the RTC and CMOS memory backup. Use PANASONIC BR2032 or compatible.

2.3 Interfaces

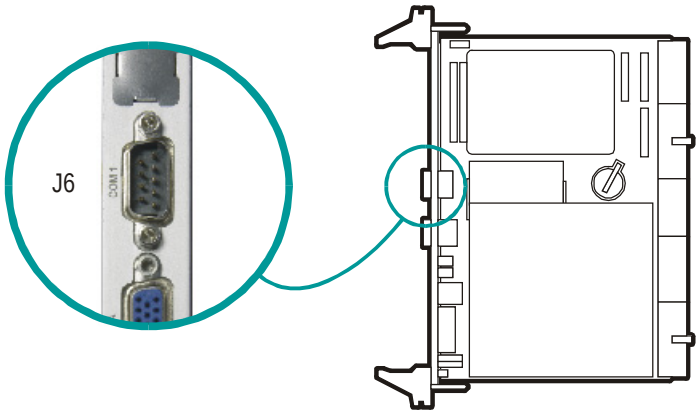
2.3.1 Keyboard/Mouse Interface

The onboard keyboard controller is 8042 software compatible.

The keyboard and mouse port is routed to the CompactPCI rear I/O interface. There is no front I/O connector available at CPC501. To connect a keyboard and/or a mouse a 6-pin MiniDIN connector CON14 is available at the front panel of RIO581 and RIO585 Rear I/O modules. Keyboard and mouse simultaneous connection requires Y-cable.

2.3.2 Serial Interfaces COM1 and COM2

Figure 2-1: PC-Compatible D-Sub Connector J6 (COM1)



One PC-compatible serial 9-pin D-sub connector (COM1) is available on the front panel as a RS-232 port. COM2 is available at the Rear I/O only. Both COM ports are fully compatible with the 16550 controller and include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer rate of up to 460.8 Kb/s.

Serial port COM1 can be switched to front panel or to the Rear I/O from inside the BIOS Setup program. The standard configuration is front I/O.

The two COM interfaces may be used at the Rear I/O as either RS-232, RS-422 or RS-485 ports via suitable adapter.

Table 2-2: Serial Port Connector J6 (COM1) Pinout

Pin Number	Function	Pin Number	Function
1	DCD	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RIN
5	GND		

2.3.3 Serial Interfaces COM3 and COM4

Additionally, two PC-compatible serial ports with TTL signal level are available. These two COM ports, which are fully compatible with the 16550 controller, include a complete set of handshaking and modem control signals, and maskable interrupt generation. **The COM3 and COM4 ports are available on the CompactPCI Rear I/O interface only.**

2.3.4 USB Interfaces

The CPC501 supports five USB 2.0 ports (two front I/O, one onboard interface and two on the Rear I/O module). All five ports support high-speed, full-speed, and low-speed operation. Hi-speed USB 2.0 supports data transfer rate of up to 480 Mb/s.

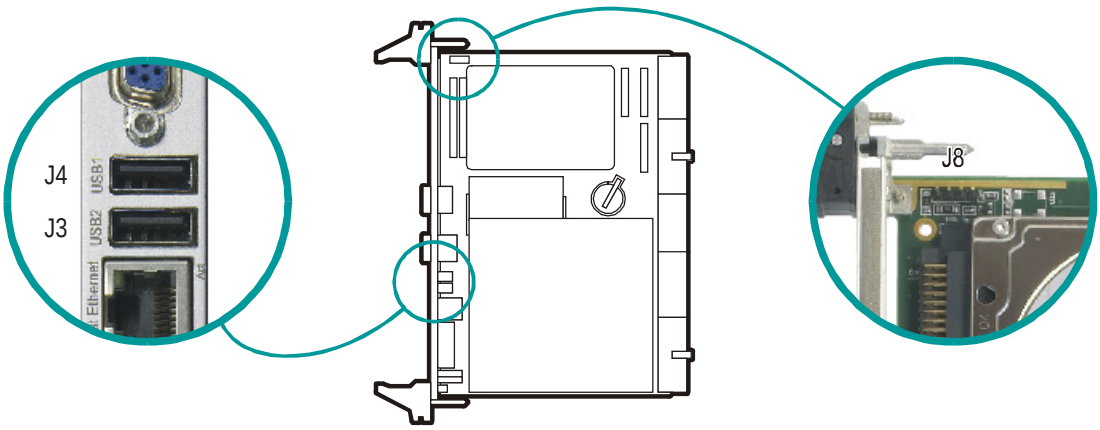
Note:

Some USB devices connected to the Rear I/O sockets may work in USB 1.1 mode only.

Only one USB device may be connected to each port. To connect more than five USB devices use an external hub.

The USB power supply is protected by a self-resettable 500 mA fuse.

Figure 2-2: USB Connectors J3, J4 and J8



The pinouts of the USB connectors appear on the following page.

2.3.4.1 USB Connectors J3 and J4 (front panel sockets) and J8 (onboard connector) Pinouts

The CPC501 has three USB interfaces (two more available via rear I/O) implemented on 4-pin connectors with the following pinouts:

Table 2-3: USB Connectors J3 and J4 Pinouts

Pin Number	Signal	Function	In/Out
1	VCC	VCC signal	–
2	UV0-	Differential USB-	–
3	UV0+	Differential USB+	–
4	GND	GND signal	–

Table 2-4: USB Connector J8 Pinout

Pin Number	Signal	Function	In/Out
1	VCC	VCC signal	–
2	UV0-	Differential USB-	–
3	UV0+	Differential USB+	–
4	GND	GND signal	–

2.3.5 Graphics Controller

A highly integrated 2D/3D graphics accelerator is included in the 855GME chipset. The internal graphics controller provides interfaces to a standard analog monitor or/and to a digital TFT panel with LVDS interface. The LVDS socket is available at Fastwel's RIO581 front panel.

Main features of an integrated 2D/3D graphics controller are:

- Resolutions up to 1600×1200 at 100 Hz, 1920×1440 at 85 Hz and 2048×1536 at 75 Hz
- 3D Setup and Render Engine
- High Quality Texture Engine
- 3D Graphics Rasterization Enhancements
- Full 2D hardware acceleration
- Intel® 855GME D.V.M. Technology
- Intelligent Memory Management
- Integrated 350 MHz DAC

2.3.5.1 DVM Technology

The 855GME chipset supports the Dynamic Video Memory Technology (DVMT). This technology provides use of all available memory in the most efficient way for maximum graphics performance. DVMT dynamically responds to requests from applications allocating the required amount of video memory. The Intel® 855GME graphics driver is allowed to request up to 64 MB of system memory. When not needed by the graphics subsystem, the memory is freed up for other applications. Thus, memory usage is balanced for optimal graphics and system memory performance.

To support legacy VGA devices the internal video-controller needs at least 1 MB of system memory. Thus, the reported system memory size is always 1 MB less than available amount of physical memory.

2.3.5.2 Supported Resolutions

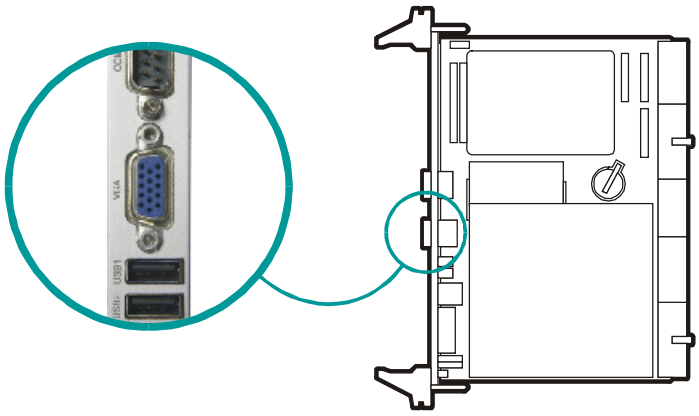
The integrated 350 MHz RAMDAC of the 855GME chipset allows direct connection of a progressive scan analog monitor with a resolution of up to 2048 × 1536 at 75 Hz. The supported resolution depends on the color depth and on the vertical scanning frequency, as illustrated in the table below.

Table 2-5: Supported Display Modes

Display Mode	Color Resolution vs. Vertical Frequency											
	8-bit Indexed				16-bit				32-bit			
	60	75	85	100	60	75	85	100	60	75	85	100
640 × 480	×	×	×	×	×	×	×	×	×	×	×	×
800 × 600	×	×	×	×	×	×	×	×	×	×	×	×
1024 × 768	×	×	×	×	×	×	×	×	×	×	×	×
1280 × 1024	×	×	×	×	×	×	×	×	×	×	×	×
1600 × 1200	×	×	×	×	×	×	×	×	×	×	×	×
1920 × 1440	×	×	×		×	×	×		×	×	×	
2048 × 1536	×	×			×	×			×	×		

2.3.5.3 CRT Interface and Connector J7

Figure 2-3: CRT Connector J7



The 15-contact D-sub female connector J7 is used to connect a CRT monitor to the CPC501 module.

Table 2-6: CRT Connector J7 Pinout

Pin Number	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
9	VCC	Power +5V 200 mA	Out
12	DDCdata	I^2C™ data	In/Out
13	Hsync	Horizontal sync.	TTL out
14	Vsync	Vertical sync.	TTL out
15	DDCclk	I^2C™ clock	Out
5, 6, 7, 8	GND	Signal ground	–
4, 10, 11	Free	–	–

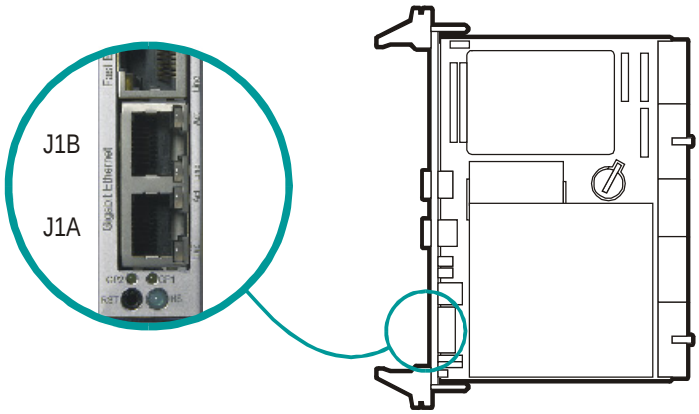
2.3.6 Parallel Port Interface

The CPC501 is provided with an IEEE1284-compatible Multi-Mode™ (SPP, ECP, EPP) parallel port/printer interface. **The parallel port is available on the RIO58x Rear I/O modules only.**

2.3.7 Gigabit Ethernet

The CPC501 module includes two 10Base-T/100Base-TX/1000Base-T Ethernet ports based on the Intel® 82541EI Gigabit Ethernet PCI Bus Controller. The Intel 82541EI Gigabit Ethernet Controller architecture combines high performance and low power consumption. The controller's architecture includes independent transmit and receive queues to minimize PCI bus traffic, and a PCI interface providing efficient bus utilization by increased use of bursts.

Figure 2-4: Gigabit Ethernet Connectors J1A and J1B



The design of the front panel may slightly differ for various versions of the module.

The Ethernet connectors are realized as RJ45 sockets J1A and J1B on the CPC501 front panel. The interfaces provide auto-detection and switching between 10Base-T, 100Base-TX and 1000Base-T operation modes. Each of the two Ethernet channels may be independently configured for the backplane (PICMG 2.16), for front I/O or for rear I/O module (see Appendix A) via the BIOS Setup or user software utility.

Note...

If the Gigabit Ethernet channel is configured for PICMG 2.16, both corresponding front panel (CPC501 and RIO58x) Gigabit connectors will have no functionality.

Table 2-7: Pinouts of Gigabit Ethernet Connectors J1A and J1B

Pin	10Base-T		100Base-TX		1000Base-T	
	I/O	Signal	I/O	Signal	I/O	Signal
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX–	O	TX–	I/O	BI_DA–
3	I	RX+	I	RX+	I/O	BI_DB+
4	–	–	–	–	I/O	BI_DC+
5	–	–	–	–	I/O	BI_DC–
6	I	RX–	I	RX–	I/O	BI_DB–
7	–	–	–	–	I/O	BI_DD+
8	–	–	–	–	I/O	BI_DD–

MDI / Standard Ethernet Cable

Integrated Ethernet LEDs

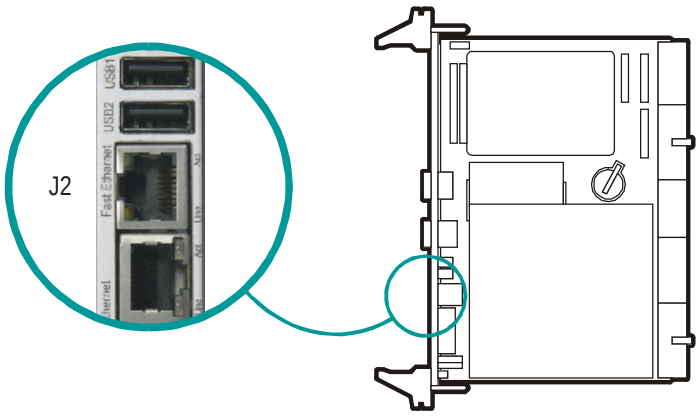
Green: Line: This LED indicates network connection. The LED lights up when the line is connected.

Green: Act: This LED monitors network activity. The LED lights up when network packets are sent or received through the RJ45 port. When this LED is not lit it means that the computer is not sending or receiving network data.

2.3.8 Fast Ethernet

The CPC501 module includes one 10Base-T/100Base-TX Ethernet 82559-type port as part the ICH4 chipset.

Figure 2-5: Fast Ethernet Connector J2



The design of the front panel may slightly differ for various versions of the module.

The Fast Ethernet interface is available via an RJ45 connector J2 on the CPC501 front panel. The interface provides automatic detection and switching between 10Base-T and 100Base-TX operation modes.

Note...

For some previous versions of RIO585 Rear I/O module two more Fast Ethernet connectors may be available as a function of the two Gigabit Ethernet controllers. They are replicates of the two Gigabit Ethernet connectors at the CPC501 front panel, but can be used as 100 Mb/s ports only. These connectors are active only if the output of the Gigabit Ethernet controller is switched to the front panel.

For these versions of the Rear I/O module:
If the Gigabit Ethernet channel 1 or 2 is configured for front panel, the cable can be connected either to the front panel Gigabit connector, or to the corresponding Rear I/O module Fast Ethernet connector. Both connectors can not be populated at the same time.

Table 2-8: RJ45 Fast Ethernet Connector J2 Pinout

Pin Number	Signal	Function	In/Out
1	TX+	Transmit +	Out
2	TX–	Transmit –	Out
3	RX+	Receive +	In
4	NC	–	–
5	NC	–	–
6	RX–	Receive –	In
7	NC	–	–
8	NC	–	–

Integrated Ethernet LEDs

Yellow: Line: This LED monitors network connection. The LED lights up when the line is connected.

Green: Act: This LED monitors network activity. The LED lights up when network packets are sent or received through the RJ45 port. When this LED is not lit it means that the computer is not sending or receiving network data.

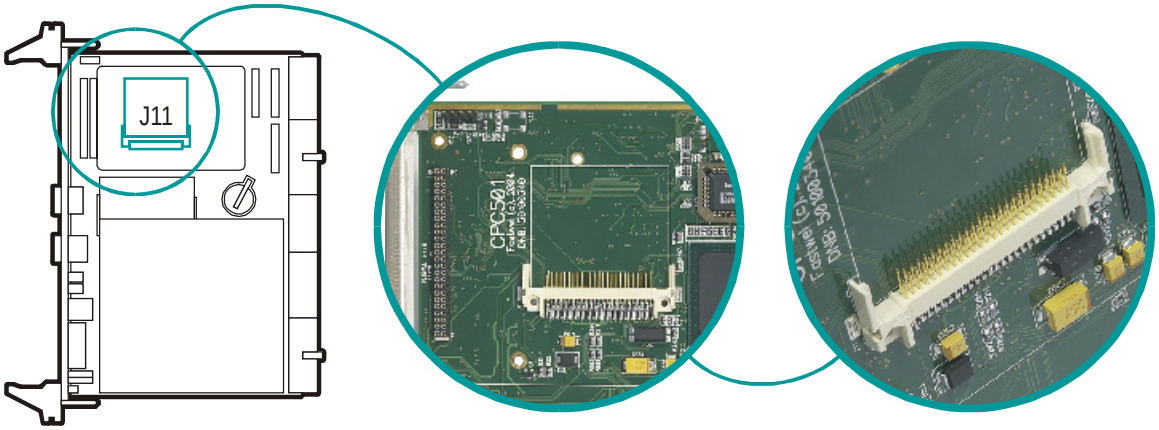
2.3.9 CompactFlash Socket

To enable usage of CF memory cards a CompactFlash type I socket (J11) is available on the CPC501 board. It is located under the hard disk drive (CPC50101). CF removable mass storage devices are fully compatible with 16-bit ATA/ATAPI-4 IDE interface with DMA support.

CompactFlash socket is connected to the primary slave EIDE port.

CompactFlash type II cards are not supported.

Figure 2-6: CompactFlash Socket Connector J11 (HDD, HDD adapter and SDRAM memory module not shown)



The CompactFlash connector pinout appears on the following page.

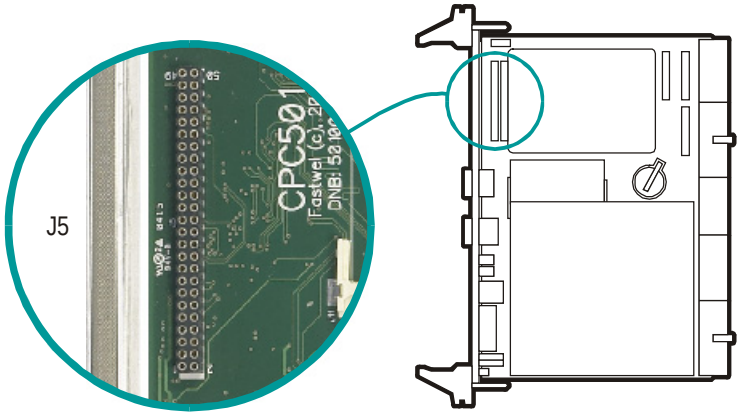
Table 2-9: CompactFlash Socket J11 Pinout

Pin Number	Signal	Function	In/Out
1	GND	Ground signal	–
2	D03	Data 3	In/Out
3	D04	Data 4	In/Out
4	D05	Data 5	In/Out
5	D06	Data 6	In/Out
6	D07	Data 7	In/Out
7	IDE_CS0	Chip select 0	Out
8	GND (A10)	–	–
9	GND (ATASEL)	–	–
10	GND (A09)	–	–
11	GND (A08)	–	–
12	GND (A07)	–	–
13	3.3 V	3.3 V power	–
14	GND (A06)	–	–
15	GND (A05)	–	–
16	GND (A04)	–	–
17	GND (A03)	–	–
18	A02	Address 2	Out
19	A01	Address 1	Out
20	A00	Address 0	Out
21	D00	Data 0	In/Out
22	D01	Data 1	In/Out
23	D02	Data 2	In/Out
24	NC (IOCS16)	–	–
25	NC (CD2)	–	–
26	NC (CD1)	–	–
27	D11	Data 11	In/Out
28	D12	Data 12	In/Out
29	D13	Data 13	In/Out
30	D14	Data 14	In/Out
31	D15	Data 15	In/Out
32	IDE_CS1	Chip select 1	Out
33	NC (VS1)	–	–
34	DIOR	I/O read	Out
35	DIOW	I/O write	Out
36	3.3 V (WE)	3.3 V power	–
37	INTRQ	Interrupt	In
38	3.3 V	3.3 V power	–
39	CSEL (GND pull-up)	Master/Slave	Out
40	NC (VS2)	–	–
41	Reset	Reset	Out
42	IORDY	I/O ready	In
43	INPACK	Acknowledge	Out
44	3.3 V (REG)	3.3 V power	–
45	NC (ACTIVE)	–	–
46	NC (PDIAG)	–	–
47	D08	Data 08	In/Out
48	D09	Data 09	In/Out
49	D10	Data 10	In/Out
50	GND	–	–

2.3.10 EIDE Interfaces

The EIDE interface supports several operation modes: PIO mode, 8237-type DMA mode, Ultra DMA, ATA-66 and ATA-100 modes. In PIO mode the central processor controls the data transfers. In all the DMA modes the CPU is not engaged in data transfer. DMA modes are similar to each other, but differ in data transfer protocols details and DMA clock frequency, thus providing different transfer rates. The ICH4 ATA-100 logic can provide transfer rates of up to 100 MB/sec (read) and up to 88 MB/sec (write).

Figure 2-7: EIDE Interface Connector J5 (HDD and HDD adapter not shown)



The current version of CPC501 has two independent EIDE ports. The primary port is connected to the 50-pin, 2-row female connector J5 and to the CompactFlash connector J11. The secondary port is connected to the 40-pin, 2-row male connector at Rear I/O module, AT standard interface connector for EIDE devices.

Note...

ATA-66 and ATA-100 work at higher frequencies and require a specialized cable, which has additional grounding wires to reduce reflections, noise, and inductive effects. This cable also supports all legacy IDE drives.

The blue end of the ATA-100 cable must be connected to the main board, the gray connector to the UltraDMA/100 slave device and the black connector to the UltraDMA/100 master device.

Note...

J5 connector is not installed on CPC50102 version utilizing PMC modules.

A 2.5” hard disk or Flash disk may be mounted directly onto the CPC501 module using the 50-pin connector J5 (CPC50101 only) and a special HDD mounting adapter, which is included in the supplied set.

Table 2-10: Pinout of the AT EIDE J5 Connector

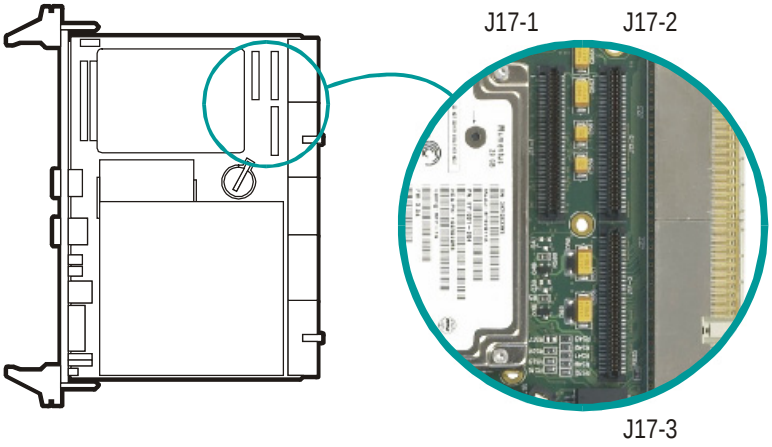
Pin Number	Signal	Pin Number	Signal
1	A	26	NC
2	B	27	IDEDRQ
3	C	28	GND
4	D	29	IOW #
5	NC	30	GND
6	NC	31	IOR #
7	IDERESET #	32	GND
8	GND	33	IOCHRDY #
9	HD7	34	GND
10	HD8	35	IDEDACKA #
11	HD6	36	GND
12	HD9	37	IDEIRQ
13	HD5	38	NC
14	HD10	39	A1
15	HD4	40	ATA66
16	HD11	41	A0
17	HD3	42	A2
18	HD12	43	HCS0
19	HD2	44	HCS1
20	HD13	45	LED #
21	HD1	46	GND
22	HD14	47	VCC
23	HD0	48	VCC
24	HD15	49	GND
25	GND	50	NC

2.3.11 Floppy Drive Interface

The onboard floppy disk controller supports either 5.25 inch or 3.5 inch (1.44 or 2.88 MB) floppy disk drives. **The floppy disk port is only available on the CompactPCI Rear I/O module.**

2.3.12 PMC Interface

Figure 2-8: PMC Connectors J17-1, J17-2 and J17-3



For flexible and easy expansion one onboard PMC socket is available. The J17-1 and J17-2 connectors provide the signals for the 32-bit PCI Bus. The 64-bit PMC interface is not implemented. User defined I/O signals are also supported via J17-3.

This interface has been designed to comply with the IEEEP1386.1 specification which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor. The CPC501 provides for 3.3 V PMC PCI signaling environment.

Note:

The PMC rear I/O signals from J17-3 are routed to CompactPCI connector J23, whose pinout is described later in this chapter.

Note:

PMC modules can be installed only on CPC50102 version, which has all the three PMC connectors (J17-1, J17-2 and J17-3), but is not equipped with the EIDE connector J5.

PMC connector pinouts follow on next page.

2.3.12.1 PMC Connectors J17-1 and J17-2 Pinouts

Table 2-11: PMC Connectors J17-1 and J17-2 Pinouts

J17-1				J17-2			
Pin	**Signal Name**	**Signal Name**	**Pin**	**Pin**	**Signal Name**	**Signal Name**	**Pin**
1	Signal	-12V	2	1	+12V	Signal	2
3	Ground	Signal	4	3	Signal	Signal	4
5	Signal	Signal	6	5	Signal	Ground	6
7	BUSMODE1#	+5V	8	7	Ground	Signal	8
9	Signal	Signal	10	9	Signal	Signal	10
11	Ground	Signal	12	11	BUSMODE2#	+3.3V	12
13	Signal	Ground	14	13	Signal	BUSMODE3#	14
15	Ground	Signal	16	15	+3.3V	BUSMODE4#	16
17	Signal	+5V	18	17	Signal	Ground	18
19	V (I/O)	Signal	20	19	Signal	Signal	20
21	Signal	Signal	22	21	Ground	Signal	22
23	Signal	Ground	24	23	Signal	+3.3V	24
25	Ground	Signal	26	25	Signal	Signal	26
27	Signal	Signal	28	27	+3.3V	Signal	28
29	Signal	+5V	30	29	Signal	Ground	30
31	V (I/O)	Signal	32	31	Signal	Signal	32
33	Signal	Ground	34	33	Ground	Signal	34
35	Ground	Signal	36	35	Signal	+3.3V	36
37	Signal	+5V	38	37	Ground	Signal	38
39	Ground	Signal	40	39	Signal	Ground	40
41	Signal	Signal	42	41	+3.3V	Signal	42
43	Signal	Ground	44	43	Signal	Ground	44
45	V (I/O)	Signal	46	45	Signal	Signal	46
47	Signal	Signal	48	47	Ground	Signal	48
49	Signal	+5V	50	49	Signal	+3.3V	50
51	Ground	Signal	52	51	Signal	Signal	52
53	Signal	Signal	54	53	+3.3V	Signal	54
55	Signal	Ground	56	55	Signal	Ground	56
57	V (I/O)	Signal	58	57	Signal	Signal	58
59	Signal	Signal	60	59	Ground	Signal	60
61	Signal	+5V	62	61	Signal	+3.3V	62
63	Ground	Signal	64	63	Ground	Signal	64

2.3.13 GP LEDs

The CPC501 provides two software programmable general purpose LEDs: GP1 (red) and GP2 (green) located on the CPC501 front panel.

2.3.13.1 GP1 (CPC501) and GP (RIO581, RIO585) LEDs Control

GP1 red LED control is realized by means of Super I/O LPC47M107 chip registers programming. This chip is also used to control GP LED on front panel of RIO58x.

1. GP1 (CPC501) and GP (RIO58x): enable control mode

```
Enable_LED_IO   proc    near
                mov     al,55h          ;Enter Configuration Mode
                out     2eh,al

                mov     al,7            ;Set Logical Device 0Ah
                out     2eh,al
                mov     al,0Ah
                out     2fh,al

GPIO_BASE       equ     600h
;This code optionally sets IO base address
;(Default for CPC501 BIOS 600h)
                mov     al,60h
                out     2eh,al
                mov     al,(GPIO_BASE SHR 8)
                out     2fh,al
                mov     al,61h
                out     2eh,al
                mov     al,(GPIO_BASE AND 0FFH)
                out     2fh,al

                mov     al,30h          ;Enable IO Registers
                out     2eh,al
                mov     al,01h
                out     2fh,al

                mov     dx,GPIO_BASE+47h;Init GP1 & RIO GP LEDs
                mov     al,6
                out     dx,al
                inc     dx
                mov     al,4
                out     dx,al

                mov     al,0AAh         ;Exit Configuration Mode
                out     2eh,al
                ret
Enable_LED_IO   endp
```

2. GP1 (CPC501) and GP (RIO58x): switch operation modes

GP1 LED (CPC501)

```
;=============================================================
;GP1_Control    GP1 Led Control
;input:         AL = 0  - OFF
;                    1  - Blink at 1 Hz rate
;                    2  - Blink at 1/2 Hz rate
;                    3  - ON
;=============================================================
GP1_Control     proc    near
                mov     dx,GPIO_BASE+5Eh
                out     dx,al
                ret
GP1_Control     endp
```

GP LED (RIO58x)

```
;=============================================================
;RIO_GP_Control RIO GP Led Control
;input:         AL = 0  - OFF
;                    1  - Blink at 1 Hz rate
;                    2  - Blink at 1/2 Hz rate
;                    3  - ON
;=============================================================
RIO_GP_Control  proc    near
                mov     dx,GPIO_BASE+5Dh
                out     dx,al
                ret
RIO_GP_Control  endp
```

3. GP1 (CPC501) and GP (RIO58x): disable control mode

```
Disable_LED_IO  proc    near
                mov     al,55h          ;Enter Configuration Mode
                out     2eh,al

                mov     al,7            ;Set Logical Device 0Ah
                out     2eh,al
                mov     al,0Ah
                out     2fh,al

                mov     al,30h          ;Disable IO Registers
                out     2eh,al
                mov     al,0
                out     2fh,al

                mov     al,0AAh         ;Exit Configuration Mode
                out     2eh,al
                ret
Disable_LED_IO  endp
```

2.3.13.2 GP2 LED Control

This green LED is controlled via CPLD XILINX XCR3128XL.

GP2 green LED control register: 303h (write)

–	–	–	–	–	LED	WD1	WD0
7	6	5	4	3	2	1	0

Default register state –- 11111011.

GP2 LED is switched on if this control register's bit "LED" is set to "1". It is possible to switch GP2 LED off by clearing the bit "LED".

2.3.14 CompactPCI Interface

The CPC501 supports a flexibly configurable, hotswap CompactPCI interface. In the system master slot the PCI-PCI bridge is operates in transparent mode. In the peripheral slot the CompactPCI interface is isolated so that it cannot communicate with the CompactPCI bus, this mode is known as the "passive mode".

2.3.14.1 System Master Configuration

In a system slot, the CPC501 can communicate with all other CompactPCI modules through a 64-bit, 33 MHz, transparent, PCI-to-PCI bridge PLX TECH PCI6254 (HB6).

The PCI6254 (HB6) bridge supports up to seven CompactPCI loads through a passive backplane. The bridge is fully compliant with the PCI Local Bus Specification Rev. 2.1.

2.3.14.2 Peripheral Master Configuration (Passive Mode)

In a peripheral slot, the module receives power but does not communicate on the CompactPCI bus; all CompactPCI signals are isolated.

In this configuration the communication is achieved via the two Gigabit Ethernet ports as defined in the PICMG 2.16 specification. In the passive mode the module may be hot-swapped.

2.3.14.3 Packet Switching Backplane (PICMG 2.16)

The CPC501 supports a dual Gigabit Ethernet link port (Node) on the J21 connector in accordance with the CompactPCI Packet Switching Backplane Specification PICMG 2.16, version 1.0. The two nodes (Gigabit Ethernet 1 and 2) are connected in the chassis via the CompactPCI Packet Switching backplane to the Fabric slots "A" and "B" respectively.

This PICMG 2.16 feature can be used in the system slot and in the peripheral slot.

2.3.14.4 Hotswap Support

To ensure that a module may be removed and replaced in a working bus without disturbing the system it requires the following additional features:

- Power ramping
- Precharge
- Hotswap control and status register bits
- A LED to indicate that the module may be safely removed

2.3.14.5 Power Ramping

On the CPC501, a special hotswap controller is used to ramp up the onboard supply voltage. This is done to avoid transients on the +3.3V, +5V, +12V and -12V power supplies from the Hotswap system. In case of any undesired power conditions (short-circuit, overvoltage, undervoltage, power surges) the hot-swap controller switches the power off to prevent the damage to the PCB and its components.

2.3.14.6 Precharge

Precharge is provided on the CPC501 by a resistor on each signal line (PCI bus), connected to a +1 V reference voltage. When the module is completely inserted in the slot, the reference voltage is switched off.

2.3.14.7 Handle Switch

A microswitch is located in the lower extractor handle. Opening the handle starts the hotswap procedure. The microswitch is routed to SW1 connector on the board.

2.3.14.8 ENUM# Interrupt

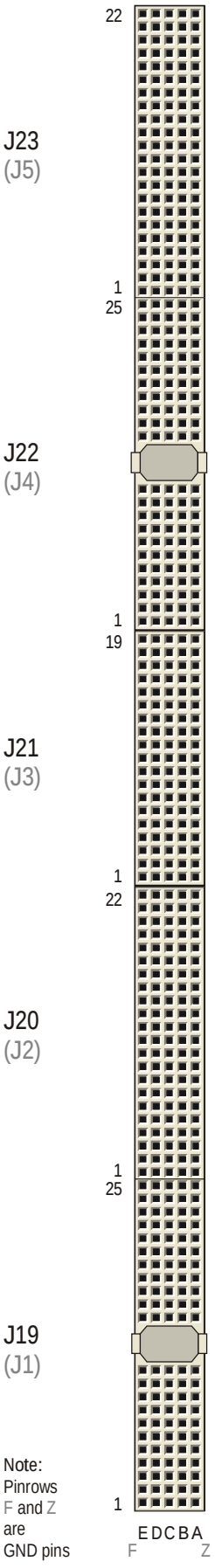
The onboard logic generates a low active interrupt signal to indicate that the module is about to be extracted from the system or have been inserted into the system. This interrupt is only generated in the peripheral master configuration. In system master configuration the ENUM signal is an input.

2.3.14.9 Blue LED

On the CPC501, a blue LED can be switched on or off by the PCI6254 (HB6). It is used to indicate that the shutdown process is finished and the module is ready for extraction or to show the readiness of the module for the complete insertion.

2.3.15 CompactPCI Bus Connectors

Figure 2-9: CompactPCI Connectors J19 – J23 (J1 – J5 according to the cPCI specification) →



The complete CompactPCI connector configuration consists of five connectors named J1 to J5. Their functions are as follows:

- J1/J2: 64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power.
- J3 has rear I/O and PICMG 2.16 interface functionality.
- J4 and J5 have rear I/O interface functionality.

The CPC501 is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus, but these systems are improved to support multiple slots and to operate in harsh industrial environments.

2.3.15.1 CompactPCI Connector Color Coding

Guide lugs on CompactPCI connectors serve to ensure a correct mating of connectors. A proper mating is guaranteed also by the use of color coded keys for 3.3V and 5V operation. Color coded keys prevent accidental installation of a 5V module into a 3.3V slot. CompactPCI backplane connectors' keying depends always on the signaling (VIO) level.

The CPC501 module is a universal 3.3V / 5V version.

Table 2-12: CompactPCI Coding Key Colors

Voltage Level	Key Color
3.3 V	Cadmium Yellow
5 V	Brilliant Blue
Universal module (5V and 3.3V)	None

CompactPCI connector pinouts appear on the following pages.

2.3.15.2 CompactPCI Connectors J19 and J20 Pinouts

The CPC501 is equipped with two 2×2 mm pitch female CompactPCI bus connectors, J19 and J20.

Table 2-13: CompactPCI Bus Connector J19 (J1) System Slot Pinout

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	LNG_VIO	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	LNG_5V	AD[2]	GND
22	GND	AD[7]	GND	LNG_3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	VIO	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	LNG_GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	LNG_GND	PERR#	GND
16	GND	DEVSEL#	GND	VIO	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	SHRT_GND	TRDY#	GND
14	GND	Key Area					GND
13	GND						GND
12	GND						GND
11	GND	AD[18]	AD[17]	AD[16]	LNG_GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	SHRT_GND	AD[23]	LNG_GND	AD[22]	GND
8	GND	AD[26]	GND	VIO	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	LNG_GND	AD[27]	GND
6	GND	REQ0#	GND	LNG_3.3V	CLK0	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	LNG_GND	GNT0#	GND
4	GND	IPMB_PWR	HEALTHY#	LNG_VIO	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	LNG_5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

Table 2-14: 64-bit CompactPCI Bus Connector J20 (J2) System Slot Pinout

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	RSV	RSV	RSV	GND
20	GND	CLK5	GND	RSV	GND	RSV	GND
19	GND	GND	GND	RSV	RSV	RSV	GND
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
17	GND	BRSVP2A17	GND	PRST#	REQ6#	GNT6#	GND
16	GND	BRSVP2A16	BRSVP2B16	DEG#	GND	BRSVP2E16	GND
15	GND	BRSVP2A15	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	VIO	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	VIO	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	VIO	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	VIO	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#	GND	VIO	C/BE[4]#	PAR64	GND
4	GND	VIO	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Note...

If the CPC501 is installed in a peripheral slot all the CompactPCI signals are isolated.

2.3.15.3 CompactPCI Rear I/O Connectors J21-J23 (J3 – J5) and Pinouts

The CPC501 conducts all I/O signals through the rear I/O connectors J21, J22 and J23. The CPC501 module provides optional rear I/O connectivity for building compact systems.

When the Rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the Rear I/O module. Thus the Rear I/O module makes it much easier to remove the CPU from the rack as there is practically no cabling on the CPU module.

For the system Rear I/O feature a special backplane is necessary. The CPC501 with Rear I/O is compatible with all standard 6U CompactPCI passive backplanes with rear I/O support on the system slot.

The pinout of the J21 (J3) connector complies with the PICMG 2.16 standard.

Table 2-15: Backplane J21 (J3) Pin Definition (PICMG 2.16 Pinout)

Pin	Z	A	B	C	D	E	F
19	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
18	GND	LP0_DA+	LP0_DA-	GND	LP0_DC+	LP0_DC-	GND
17	GND	LP0_DB+	LP0_DB-	GND	LP0_DD+	LP0_DD-	GND
16	GND	LP1_DA+	LP1_DA-	GND	LP1_DC+	LP1_DC-	GND
15	GND	LP1_DB+	LP1_DB-	RSVD	LP1_DD+	LP1_DD-	GND
14	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
13	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
12	GND	FD_DS0	FD_DENSEL1	FD_MTR0	FD_INDEX	FD_WDATA	GND
11	GND	FD_DS1	FD_DSKCHG	FD_MTR1	FD_DENSEL0	FD_RDATA	GND
10	GND	FD_WP#	FD_HDSEL	FD_DIR	FD_TRK0	FD_STEP	GND
9	GND	FD_WGATE#	SIDE_D15	SIDE_D14	SIDE_D13	USB0+	GND
8	GND	SIDE_D12	SIDE_IOW	VCC	SIDE_IOR	USB0-	GND
7	GND	SIDE_A2	SIDE_A1	SIDE_A0	SIDE_D0	SIDE_D1	GND
6	GND	SIDE_D2	SIDE_D3	SIDE_D4	SIDE_D5	SIDE_D6	GND
5	GND	RSVD	PMDAT	SPKR	KDAT	RSVD	GND
4	GND	PRST	PMCLK	VCC	KCLK	COM3_RXD	GND
3	GND	COM3_CTS	COM3_RTS	COM3_DSR	COM3_DCD	COM3_TXD	GND
2	GND	SIDE_D7	SIDE_D8	COM3_RI	COM3_DTR	COM4_RXD	GND
1	GND	SIDE_D9	SIDE_D10	SIDE_D11	BATT	COM4_TXD	GND

Table 2-16: Backplane J22 (J4) Pin Definitions

Pin	Z	A	B	C	D	E	F
25	GND	VCC	RSVD	RSVD	+3.3V	VCC	GND
24	GND	RSVD	PD0	INIT	RSVD	IRQ15	GND
23	GND	+3.3V	RSVD	RSVD	VCC	IDE_RST#	GND
22	GND	RSVD	PD1	RSVD	SIORDY	RSVD	GND
21	GND	+3.3V	RSVD	AUTOFD	SDCS3#	SMB_CLK	GND
20	GND	RSVD	PD2	SLCTIN	RSVD	SMB_DATA	GND
19	GND	+3.3V	PD3	STROBE	SDCS1#	GND	GND
18	GND	RSVD	PD4	RSVD	RSVD	LAN2_MDI2+	GND
17	GND	+3.3V	PD5	BUSY	SDDACK#	LAN2_MDI2-	GND
16	GND	RSVD	PD6	RSVD	RSVD	LAN2_MDI3+	GND
15	GND	+3.3V	PD7	ACK	SDDREQ#	LAN2_MDI3-	GND
14	GND	Key area					GND
13	GND						GND
12	GND						GND
11	GND	AC_SDATAOUT	RSVD	PE	DDC_DATA	LAN1_MDI3-	GND
10	GND	AC_SDATAIN2	RSVD	RSVD	RSVD	LAN1_MDI3+	GND
9	GND	AC_SDATAIN1	RSVD	SLCT	DDC_CLOCK	LAN1_MDI2-	GND
8	GND	AC_SDATAIN0	GND	RSVD	RSVD	LAN1_MDI2+	GND
7	GND	GND	LVDS_TXP2	ERROR	RSVD	GND	GND
6	GND	AC_BITCLK	LVDS_TXN2	RSVD	RSVD	USB_OC#	GND
5	GND	GND	GND	LVDS_TXP1	RSVD	RSVD	GND
4	GND	AC_SYNC	GND	LVDS_TXN1	GND	GND	GND
3	GND	LVDS_ENVDD	LVDS_FPVEE	GND	LVDS_TXP0	LVDS_TXCLKP	GND
2	GND	AC_RST#	RSVD	GND	LVDS_TXN0	LVDS_TXCLKN	GND
1	GND	VCC	-12V	GND	+12V	VCC	GND

Table 2-17: Backplane J23 (J5) Pin Definitions

Pin	Z	A	B	C	D	E	F
22	GND	PMCR4	PMCR3	PMCR2	PMCR1	PMCR0	GND
21	GND	PMCR9	PMCR8	PMCR7	PMCR6	PMCR5	GND
20	GND	PMCR14	PMCR13	PMCR12	PMCR11	PMCR10	GND
19	GND	PMCR19	PMCR18	PMCR17	PMCR16	PMCR15	GND
18	GND	PMCR24	PMCR23	PMCR22	PMCR21	PMCR20	GND
17	GND	PMCR29	PMCR28	PMCR27	PMCR26	PMCR25	GND
16	GND	PMCR34	PMCR33	PMCR32	PMCR31	PMCR30	GND
15	GND	PMCR39	PMCR38	PMCR37	PMCR36	PMCR35	GND
14	GND	PMCR44	PMCR43	PMCR42	PMCR41	PMCR40	GND
13	GND	PMCR49	PMCR48	PMCR47	PMCR46	PMCR45	GND
12	GND	PMCR54	PMCR53	PMCR52	PMCR51	PMCR50	GND
11	GND	PMCR59	PMCR58	PMCR57	PMCR56	PMCR55	GND
10	GND	+3.3V	PMCR63	PMCR62	PMCR61	PMCR60	GND
9	GND	TDN2_2	RDN2_2	COM1_RXD	TDN1_2	RDN1_2	GND
8	GND	TDP2_2	RDP2_2	COM1_TXD	TDP1_2	RDP1_2	GND
7	GND	COM2_ENABLE	COM1_ENABLE	COM1_RTS	USB1+	+3.3V	GND
6	GND	COM1_DTR	COM1_CTS	COM1_DSR	COM1_DCD	COM1_RI	GND
5	GND	COM2_RXD	COM2_TXD	COM2_RTS	COM2_DTR	RED_OUT	GND
4	GND	COM2_DSR	COM2_DCD	COM2_RI	COM2_CTS	HSYNC	GND
3	GND	COM4_DTR	COM4_CTS	COM4_DSR	GP_LED	BLUE_OUT	GND
2	GND	COM4_RTS	COM4_RI	FAN_SENSE2	FAN_PWM	VSYNC	GND
1	GND	COM4_DCD	RIO_PRSNT	FAN_SENSE1	USB1-	GREEN_OUT	GND

2.3.15.4 Rear I/O Interfaces

Rear I/O interfaces are available only if a Rear I/O module is installed.

Ethernet Interfaces

Gigabit Ethernet signals are available on the CPC501 and RIO58x front panel connectors and on the backplane interface (PICMG 2.16 pinout). Each Gigabit Ethernet channel can be switched over to the backplane or to one of the CPC501 and RIO58x front panels. It is not possible to use the CPC501 front panel Gigabit Ethernet socket and the Rear I/O module Gigabit Ethernet socket for the same channel at the same time. Switching over from backplane to front panels and between them is effected under BIOS control (see Chapter 5 for details). **Fast Ethernet** interface is available on the CPC501 front panel (J2) as a function of the Fast Ethernet controller and on previous versions of Rear I/O modules as a function of the Gigabit Ethernet controllers.

VGA CRT Interface

The VGA signals are available on both rear I/O and front I/O. The 75 ohm termination resistors for the red, green and blue video signals are installed on the CPC501.

Note:

Both VGA ports are electrically identical and not separated.
Do not connect devices at both connectors (front I/O and rear I/O) at the same time.

LVDS Interface

LVDS port utilizes a 20-pin socket (Molex 52515-2011) on RIO581 front panel and is used for connection of a flat-panel monitors. LVDS socket is available at the RIO581 module only.

Serial Interface COM1

COM1 can be switched over to the front panel of CPC501 or to the Rear I/O module via the BIOS Setup. Only one interface may be used (rear I/O or front I/O).

Serial Interfaces COM2, COM3 and COM4

The serial interfaces COM2, COM3 and COM4 are available via the Rear I/O module only.

USB Interface

Two of five USB 2.0 interfaces are available only via the Rear I/O.

Keyboard/Mouse Interface

Keyboard and mouse interfaces are available via the Rear I/O module only. Simultaneous use of a keyboard and a mouse requires Y-cable.

Parallel Port LPT1

The parallel port LPT1 interface is only available via the Rear I/O.

Secondary EIDE Interface

Both master and slave secondary interfaces are available at the Rear I/O module via the on-board CON7 40-pin IDC connector.

Floppy Interface

The floppy interface is only available via the Rear I/O.

Audio Interface

There are three audio connectors (MicIN, Phones and Line IN; 3.5 mm) on the RIO585 front panel and three more audio connectors on board (Aux In, CD In and Line Out). These connectors are available at the RIO585 module only. Moreover, all Rear I/O modules have an on-board PC-speaker connector.

Please see Appendix A for detailed information about Rear I/O interfaces.

Chapter 3

Installation

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3 Installation

The CPC501 is easy to install. However, it is necessary to follow the procedures and safety regulations below to install the module correctly without damage to the hardware, or harm to personnel.

The installation of the peripheral drivers is described in the accompanying information files. For details on installation of an operating system, please refer to the relevant software documentation.

3.1 Safety Regulations

The following safety regulations must be observed when installing and operating the CPC501 processor module. Fastwel bears no responsibility for any damage caused by nonobservance of these rules.

Warning!

When handling or operating the module, special attention should be paid to the heatsink, because it can get very hot during operation. Do not touch the heatsink when installing or removing the module.

Moreover, the module should not be placed on any surface or in any kind of package until the module and its heatsink have cooled down to ambient temperature.

Caution!

If your module does not allow hotswapping, switch off the system power before installing the module in a free slot. Disregarding this requirement could be harmful for your life or health and can damage the module or entire system.

ESD Equipment!

This product comprises electrostatically sensitive components. Please follow the ESD safety instructions to ensure module's operability and reliability:

- Use grounding equipment, if working at an anti-static workbench. Otherwise, discharge yourself and the tools in use before touching the sensitive equipment.
- Try to avoid touching contacts, leads and components.

Extra caution should be taken in cold and dry weather.

3.2 Initial Installation

The following procedures are related only to the initial installation of the CPC501 into a system case. Procedures for normal removal and hotswap operations are located in other sections of this chapter. To perform an initial installation of the CPC501 in a system do the following:

1. Keep to the safety regulations of the Section 3.1 when performing the following operations.

Warning!

Failure to accomplish the following instruction may damage the module or result in incorrect system operation.

2. Ensure that the module configuration corresponds to the application requirements before installing. For information regarding the configuration of the CPC501 refer to Chapter 4. For the instructions on installation of CPC501 peripheral devices and rear I/O devices refer to the appropriate subsections in Chapter 3.
3. To install the CPC501:
    1. Make sure that no power is connected to the system.
    2. Avoiding contact with other modules of the system, carefully insert the module into the chosen slot until it contacts the backplane connectors. Do not apply force pushing the module into the backplane connectors.
    3. Using both ejector handles, engage the module with the backplane. The module is engaged completely, when the ejector handles are locked.
    4. Fix the module with the two front panel retaining screws.
    5. Connect the required external interfacing cables to the module's connectors and make sure that the module and all connected cables are properly fixed.
4. The CPC501 is now ready for operation. For details on operation of the CPC501 processor module, refer to CPC501 specific application and software manuals.

3.3 Normal Removal

The procedure in this section describes operations for normal removal only. The hotswap procedure is described in the section below.

To remove the module from the system case do the following:

1. When performing the next actions, keep to safety regulations of the Section 3.1. Pay special attention to the temperature of the heatsink!
2. Before proceeding ensure that system power is switched off.
3. Disconnect all cables that may be connected to the module.
4. Unscrew the front panel retaining screws.
5. Unlock the ejection handles by pressing the integrated buttons and then press on them pulling apart until the module connectors are disconnected from the backplane.
6. Carefully pull the module out of the slot. Do not touch the heatsink, since it can get very hot during operation.
7. Dispose of the module at your discretion. The module should not be placed on any surface or in any form of package until the board and the heatsink have cooled down to room temperature.

3.4 Hotswap

The CPC501 supports hotswap operation. Installed in the system slot, it supports peripheral modules hotswapping. When installed in a peripheral slot, its hotswap capabilities depend on the type of backplane in use and the system controller's capabilities. The reason for this being that communications with the system controller may require either front panel Ethernet I/O or use of a packet switching backplane.

3.4.1 System Master Hotswap

Hotswapping of the CPC501 itself when used as the system controller is possible, but will result in any case in a cold restart of the CPC501 and consequently in a reinitialization of all peripheral modules. In any case, the above mentioned safety requirements above must be observed.

3.4.2 Peripheral Hotswap

It is assumed that the module to be hotswapped is installed in the system chassis and the power is on. To hotswap the CPC501 do the following:

1. Follow the safety regulations presented in Section 3.1. Please, pay special attention to the warning concerning the heatsink temperature!
2. Unscrew both front panel retaining screws.
3. Unlock both module ejection handles. Very small amount of movement of the lower handle activates the hotswap switch. Do not disengage the module completely, follow the instructions below.

4. The blue HS LED should light up after a short period of time. This indicates that the system has recognized that the CPC501 is to be hotswapped and now shows to the operator that hotswapping of the module may be continued. If the LED lights up, go to the next step of this procedure.
5. Disconnect all cables that may be connected to the module.
6. Pressing on the ejector handles, disengage the module from the backplane and carefully slide it out from the system case. Remember that the heatsink can get very hot during operation!
7. Dispose of the “old” module if needed following the safety requirements presented in Section 3.1.
8. Prepare the replacement module, check if it is properly configured for the application.
9. Carefully insert the “new” module into the “old” module slot until it makes contact with the backplane connectors.
10. After the blue LED lights up, use both ejector handles to engage the module with the backplane connectors. When the ejector handles are locked, the module is completely seated in place.
11. Fix the module in the system case with two front panel retaining screws.
12. Connect all required interface cables to the module. Hotswap of the CPC501 is now complete.

3.5 Peripheral Devices Installation

A lot of peripheral devices can be connected to the CPC501. Their installation procedures differ significantly. Therefore the following sections provide mainly general guidelines regarding installation of peripheral devices.

3.5.1 USB Devices Installation

The CPC501 can accept Plug&Play connection of USB 2.0 computer peripheral devices (printers, keyboards, mice, etc.) All USB devices may be connected or disconnected while the host power is on.

3.5.2 CompactFlash Cards Installation

The CompactFlash socket of CPC501 supports all available 3.3 V or 5 V CompactFlash Type I ATA cards. "Hotplugging" is not supported.

Warning!

Do not connect or remove the CompactFlash cards while the module is powered-up. This may damage your system.

Note...

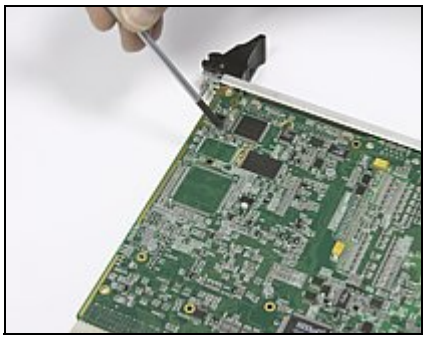
It is recommended to use CF-cards, which has been initialized and formatted in this module.
By default, CPC501 utilizes LBA mode. Utilization of CompactFlash cards, which has been initialized and formatted in another mode, may lead to misoperation of the module.

3.5.3 Hard Disk Installation

The procedure below is applicable to hard disk which may be connected to the CPC501 via J5 connector (CPC50101 only). A 2.5" hard disk is installed on the CPC501 using the special HDD adapter, which is supplied with the module. To install a hard disk, it is necessary to perform the following operations in the given order:

1

2



3

1. Carefully install the HDD adapter on the CPC501, so that it connects to the J5. Make sure all the pins are engaged correctly.
2. Remove the Master/Slave jumper from HDD, if exists. Install the hard disk on the adapter, sliding the hard disk connector into the adapter's socket.
3. Fasten four retaining screws from the back side of the CPC501 to fix the HDD and the adapter on the board.
4. Use BIOS Setup program to assign a drive letter to the installed hard disk drive (Main menu > Basic CMOS Configuration > Drive Assignment Order) and choose necessary boot options.

3.5.4 Battery Replacement

The lithium battery must be replaced with Panasonic BR2032 or a battery with similar characteristics.

The expected life of a 190 mAh battery (Panasonic BR2032) is about 5 years. However, this typical value may vary because battery life depends on the operating temperature and the shutdown time of the system in which the battery is installed.

Note...

It is recommended to replace the battery after approximately 4 years to be sure it is operational.

Important:

Replacing the battery, make sure the polarity is correct ("+" up).

Dispose of used batteries according to the local regulations.

3.5.5 Rear I/O Modules Installation

The installation technique for RIO58x rear I/O modules is similar to the one of CPC501 processor module. It is necessary to follow the same procedures and safety instructions described in sections 3.1, 3.2 and 3.3 in this chapter.

For the proper functioning of the Rear I/O COM1 port and Ethernet port, make sure they are configured for rear operation via the BIOS Setup (see Chapter 5 for details).

Chapter 4

Configuration

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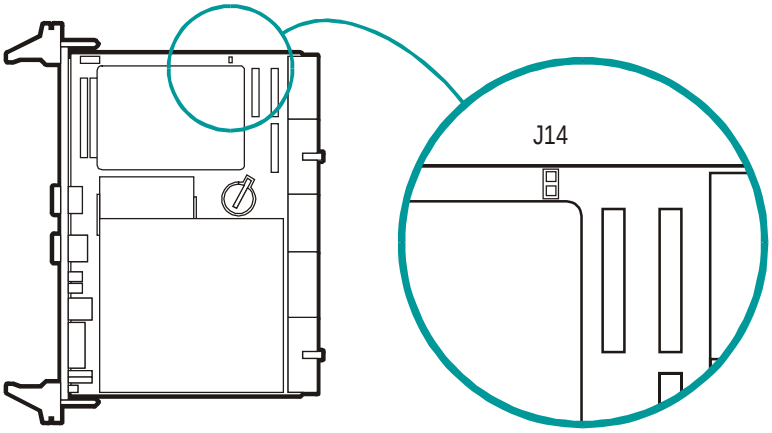
4 Configuration

4.1 J14 Jumper Description

If the system does not boot (due to, for example, the wrong BIOS configuration or incorrect password) the settings stored in CMOS may be cleared using jumper J14.

Figure 4-1: Jumper J14 Location



Procedure for clearing CMOS settings:

1. Switch off the system power
2. Set the J14 jumper into the closed position
3. Wait for at least 10 seconds. CMOS setting are reset to factory defaults
4. Set the J14 jumper back to the open position
5. Switch the power on
6. Configure the system using the BIOS Setup program

4.2 Interrupts Handling

Interrupt handling of the CPC501 module corresponds to the standard AT IRQ mapping (8259 IRQ controller integrated in the chipset). The functions of the interrupts described below are the default ones, but can be modified via the BIOS Setup.

Table 4-1: Interrupt Settings

IRQ	Priority	Standard Function
IRQ0	1	System timer
IRQ1	2	Keyboard controller
IRQ2	–	Second IRQ controller input (IRQ8-IRQ15)
IRQ3	11	COM2, COM4
IRQ4	12	COM1, COM3
IRQ5	13	Reserved
IRQ6	14	Floppy disk controller
IRQ7	15	LPT
IRQ8	3	System RTC
IRQ9	4	PCI or ACPI
IRQ10	5	PCI
IRQ11	6	PCI
IRQ12	7	PCI or PS/2 mouse
IRQ13	8	Coprocessor error
IRQ14	9	Primary IDE channel
IRQ15	10	Secondary IDE channel
NMI	–	Reserved

4.2.1 On-board PCI Interrupts

The ICH4 handles up to 8 PCI interrupt inputs. The table below describes the connected to these PIRQs PCI devices and their functions.

Table 4-2: PCI Interrupt Routing

ICH4 IRQ Input	PCI Device	Internal ICH4 Function
PIRQA	PCI to PCI Bridge IRQA	USB 1 controller
PIRQB	PCI to PCI Bridge IRQB	AC97 + MODEM + SMBUS
PIRQC	PCI to PCI Bridge IRQC	USB 2 controller
PIRQD	PCI to PCI Bridge IRQD	USB 3 controller
PIRQE	Free	LAN controller IRQA
PIRQF	PMC IRQC + Gigabit Ethernet	free
PIRQG	PMC IRQD + Gigabit Ethernet	free
PIRQH	Security	USB 2.0 controller

For details, please refer to the Intel ICH4 documentation.

4.3 Memory Maps

The CPC501 module employs the standard AT ISA memory mapping. The details of memory mapping are presented in the following subsections.

4.3.1 First Megabyte Memory Map

The following table shows the memory map for the first megabyte:

Table 4-3: First Megabyte Memory Map

Memory Address Range	Size	Function
0xE0000 – 0xFFFFF	128 k	BIOS based in FWH Reset vector 0xFFFF0
0xD0000 – 0xDFFFF	64 k	Free
0xCC000 – 0xCFFFF	16 k	Free
0xC0000 – 0xCC800	48 k	VGA card BIOS
0xA0000 – 0xBFFFF	128 k	Normally used as video RAM according to: CGA: 0xB8000-0xBFFFF Monochrome: 0xB0000-0xB7FFF EGA/VGA: 0xA0000-0xAFFFF
0x00000 – 0x9FFFF	640 k	DOS memory space

4.3.2 I/O Addresses

The following table presents the I/O memory mapping:

Table 4-4: I/O Address Map

Address	Device
000,00F	DMA controller #1
020,02D	Interrupt controller #1
040,043	Timer
060,064	Keyboard interface
070,077	RTC port
080,09F	DMA page register
0A0,00A	Interrupt controller #2
0C0,0DF	DMA controller #2
0F0,0FF	Math coprocessor
170,17F	Secondary hard disk
1F0,1FF	Primary hard disk
2E8,2EF	Serial port COM4
2F8,2FF	Serial port COM2
378,37F	Parallel printer port LPT1
3E8,3EF	Serial port COM3
3F0,3F7	Floppy Disk
3F8,3FF	Serial port COM1

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Chapter 5

Phoenix® BIOS Setup

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5 Phoenix® BIOS Setup

The Phoenix® BIOS in your SBC is an adapted version of a standard BIOS for IBM PC AT-compatible personal computers equipped with Intel®x86 and compatible processors. The BIOS provides low-level support for the central processing, memory, and I/O system units.

With the help of BIOS Setup program, you can modify the BIOS configuration parameters and control the special features of your module. The Setup program is started by pressing the F2 key and offers a convenient menu interface to modify basic system configuration settings and switching between the subsystems operation modes. These settings are stored in a dedicated battery-backed memory, CMOS RAM, that keeps the information when the power is switched off. For increased security, the CMOS data and some of the service parameters are stored also in a nonvolatile serial EEPROM memory. This allows to restore the critical data in emergency cases after battery failure.

5.1 Boot Details

5.1.1 Booting without a Monitor, Keyboard or Mouse

To boot without a monitor, keyboard or mouse set the item "POST Errors" to "Disabled" at the page "Main" in PhoenixBIOS Setup program. This setting is a default one.

Note!

If the module was booted without a connected monitor, the display will be empty, even if a monitor is connected later during operation. To get the correct display output it is necessary to reboot the module with a connected monitor. This is a Intel VideoBIOS particularity.

5.1.2 Booting from USB

To boot from a device connected to USB:

- Connect the device to boot from to a USB port. The appropriate USB controller should be enabled;
- Enter the PhoenixBIOS Setup program;
- Find this USB device at the "Boot" page and use «+» «–» buttons to move it in order to change its boot priority;
- Save changes and reboot the module.

To get the on-line help about the details of BIOS Setup program operation, please apply to the screen tips and the integrated help system.

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Chapter 6

Thermal and Power Issues

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6 Thermal and Power Issues

6.1 Temperature Control

Intensive operation of Intel Pentium M processor in harsh environment requires a special technology to keep the processor's die temperature within allowed limits. The following sections provide system integrators with the information, which will help to meet thermal requirements when developing systems based on CPC501.

6.1.1 Passive Regulation

The thermal management concept of CPC501 module includes four separate but correlated functions. Their main purpose is to protect the processor from overheating and reduce its power consumption. Dedicated thermal control subsystem allows the processor to operate within safe temperature range without the need for special software or interrupt handling.

The four thermal protection functions provided by the processor are:

1. **Thermal Throttling**: The Pentium M internal thermal monitor controls the temperature of the processor. The internal temperature sensor is located near the hottest area of the processor die. Each processor is individually adjusted at the factory to compensate the potential manufacturing variations of its characteristics. To reduce the processor power dissipation the internal thermal monitor switches the processor core clock on and off with a duty cycle factor of 50%.
2. The Intel® Pentium® M processor supports the Intel **SpeedStep**® enhanced technology. It allows to switch the processor core voltage and frequency between several modes from High Frequency Mode to Low Frequency Mode without resetting the system. For example, the processor operating at 1.6 GHz and 1.484 V (HFM) can be switched down to 600 MHz and 0.956 V (LFM), thus reducing the processor power consumption in approx. 4 times.
3. **Thermtrip** technology. This function is always on to protect the processor in any event. In case of a serious cooling subsystem failure, the processor will automatically shut down when the die temperature has reached approximately 125°C. Once Thermtrip is activated, the system does not return to the normal operation mode automatically, it is necessary to reset the BIOS settings (see Section 4.1) and to cold restart the system.
4. **External thermal monitor** (LM82) gathers information about the processor and board surface temperatures from two sensors. This information may then be requested by a program to undertake the appropriate actions.

Recommendations

Generally, there is no need to enable the Thermal Management functions if the module is operated in a optimally designed environment with sufficient air flow. However, to guarantee a stable system in unsteady industrial environment, both the internal and the external thermal monitors should be enabled. These two monitors protect the processor and the whole system against overheating.

Note:

Thermal Management functions should be disabled when performing Benchmarks and performance tests, otherwise the results will be incorrect due to the power reduction processes influence.

6.1.2 Active Regulation

To provide controlled active heat dissipation CPC501 is equipped with a specially designed heatsink. Together with a system chassis equipped with adjustable forced air flow system this provides a basis for reliable and steady operation. Forced air flow of sufficient volume is vital for high performance processors operating in high temperature environments.

When developing applications using the CPC501, the system integrator must take into account the overall system thermal requirements. System chassis must satisfy these requirements. When performing thermal calculations for certain application, the developer must consider the contribution of peripherals to be used with the CPC501 to the total heat emission. These devices must also be capable to operate at the temperatures within the system operating range, especially those, which are directly attached to the CPC501 processor module.

Warning!

Since Fastwel does not assume responsibility for any damage to the CPC501 module or other system parts resulting from overheating of the central processor, it is important to ensure that the CPC501 operational environment parameters conform to the thermal requirements described in this Manual.

6.2 System Power

The Intel Pentium M processor family require special characteristics of the power supply unit and the backplane.

The CPC501 module itself has been designed to provide best possible power supply for each system unit. However, in order to guarantee reliable and faultless operation the following requirements must be taken into account. Absolute maximum input voltages presented in the table below must not be exceeded to guarantee that the CPC501 is not damaged. The ranges for the different input power voltages, within which the module is functional, are also presented.

Table 6-1: DC Input Voltage Ranges and Limits

Power Voltage, V	Maximum Permitted Value, V	Absolute Limits, V	Recommended Range, V
+3.3	+3.6	3.2 to 3.47	3.3 to 3.47
+5	+5.5	4.9 to 5.25	5.0 to 5.25
+12	+14.0	11.4 to 12.6	–
-12	-14.0	-11.4 to -12.6	–

Power supplies to be used with the CPC501 should comply with these requirements.

Only backplanes which have two power layers for each of the +3.3V and the +5V supply voltage are recommended for CPC501. Input power connections to the backplane itself should provide minimum power loss. Avoid using long input lines, low carrying capacity cables, high resistance connections.

To select the appropriate system power supply, it is necessary to consider the CPC501 own power consumption (about 35 watts), the consumption of the remaining system components, possible variations of power consumption during operation (e.g. due to temperature changes) and some reserve. Taking all this into account, it is recommended to use a 150 watt power supply. If possible, power supplies with voltage sensing should be used. This may require an appropriate backplane.

Table 6-2: CPC501 Components Power Consumption

System Modules		Power Consumption
Keyboard	(5 V)	100 mW
DDR SDRAM SODIMM PC2700 1 GB	(2.5 V)	5 W
CompactFlash card	(3.3 V)	100 to 300 mW

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Appendices

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Appendix A

A Rear I/O Modules

A.1 Introduction

RIO581 and RIO585 Rear I/O modules have been designed for use with the Fastwel CPC501 6U CompactPCI processor module. These Rear I/O modules expand I/O functionality of the CPC501 being plugged in from the back of the system into the appropriate backplane connectors in line with the CPU module. Processor module can work with only one Rear I/O module at a time.

A particular advantage of the rear I/O capability is that there is no or less cabling on the CPU module which makes it much easier to remove the processor module from the rack.

A.1.1 Specifications

Power Consumption:

0.1 A @ +3.3 V; 0.1 A @ +5 V; 0.3 A @ +12 V (without external devices)

Dimensions of the 6U rear I/O modules:

233.35 x 80 x 20.32 mm (6U rear I/O card size)

A.1.2 Rear I/O Modules Versions

At the present time each of the two Rear I/O modules, RIO581 and RIO585, is available in two versions, differing in the operating temperature range:

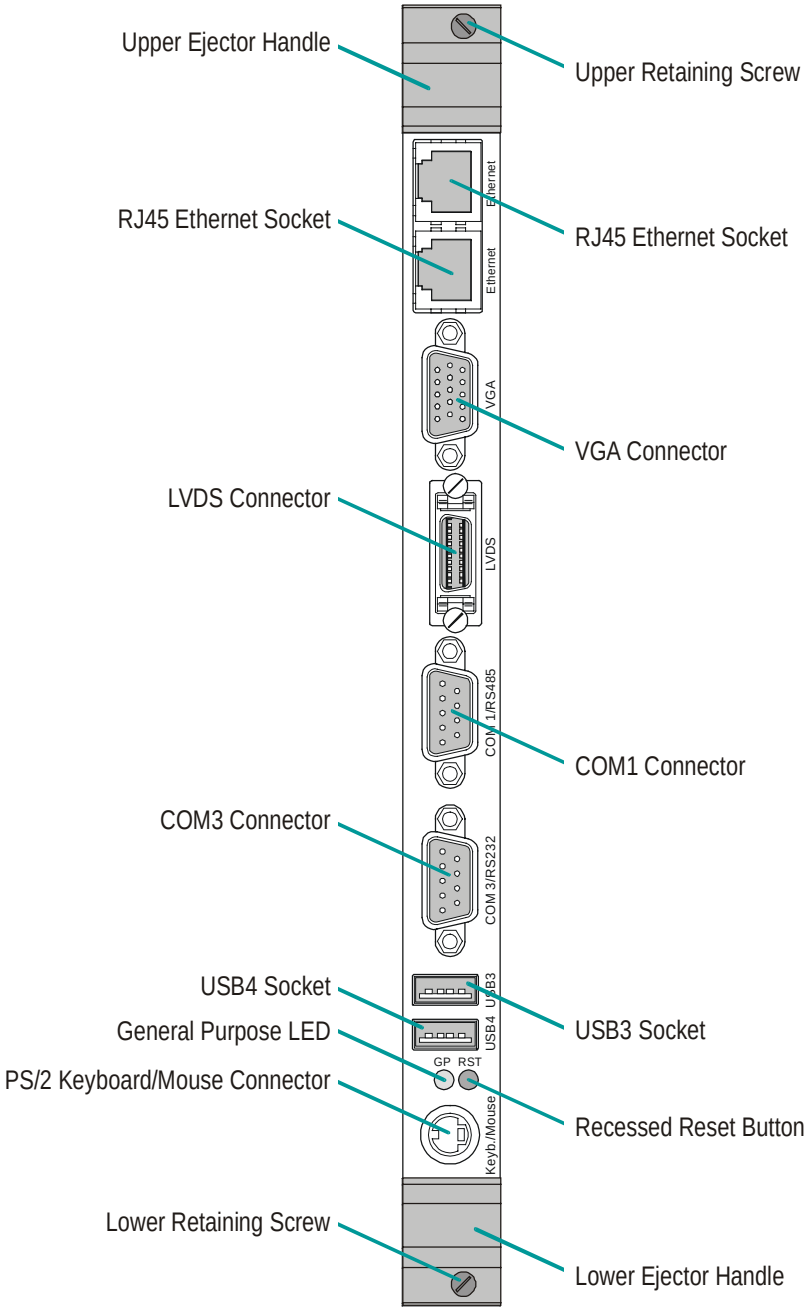
Table A-1: Rear I/O Modules Versions

Version	Operating Temperature Range
CPC58101	-40 … +85°C
CPC58101-C	0 … +70°C
CPC58501	-40 … +85°C
CPC58501-C	0 … +70°C

The differences between RIO581 and RIO585 themselves are reflected below in this Appendix. In short, RIO585, as distinguished from RIO581, has additional audio connectors at the front panel and on board, and has not LVDS connector.

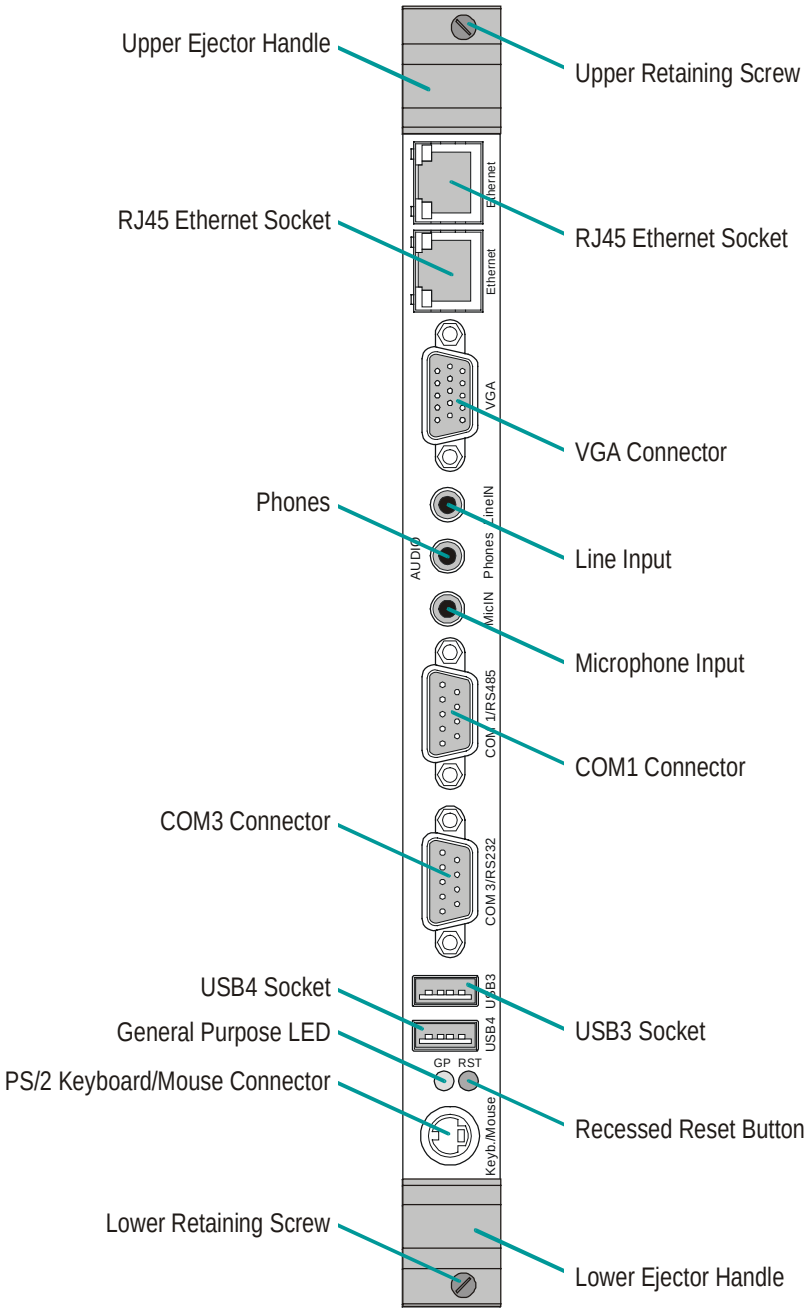
A.2 Front Panel

Figure A-1: RIO581 Front Panel



The design of the front panel may slightly differ for various versions of the module.

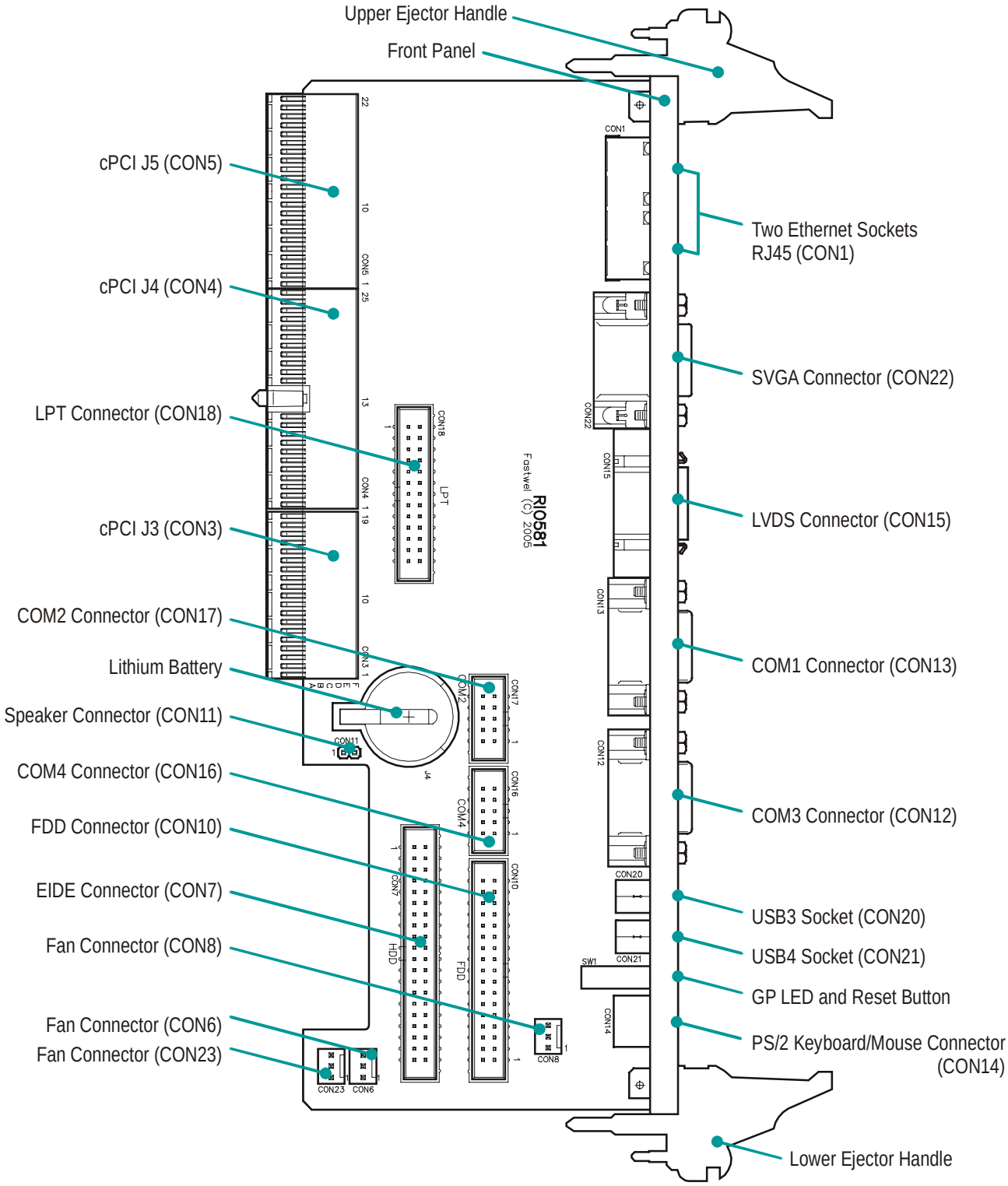
Figure A-2: RIO585 Front Panel



The design of the front panel may slightly differ for various versions of the module.

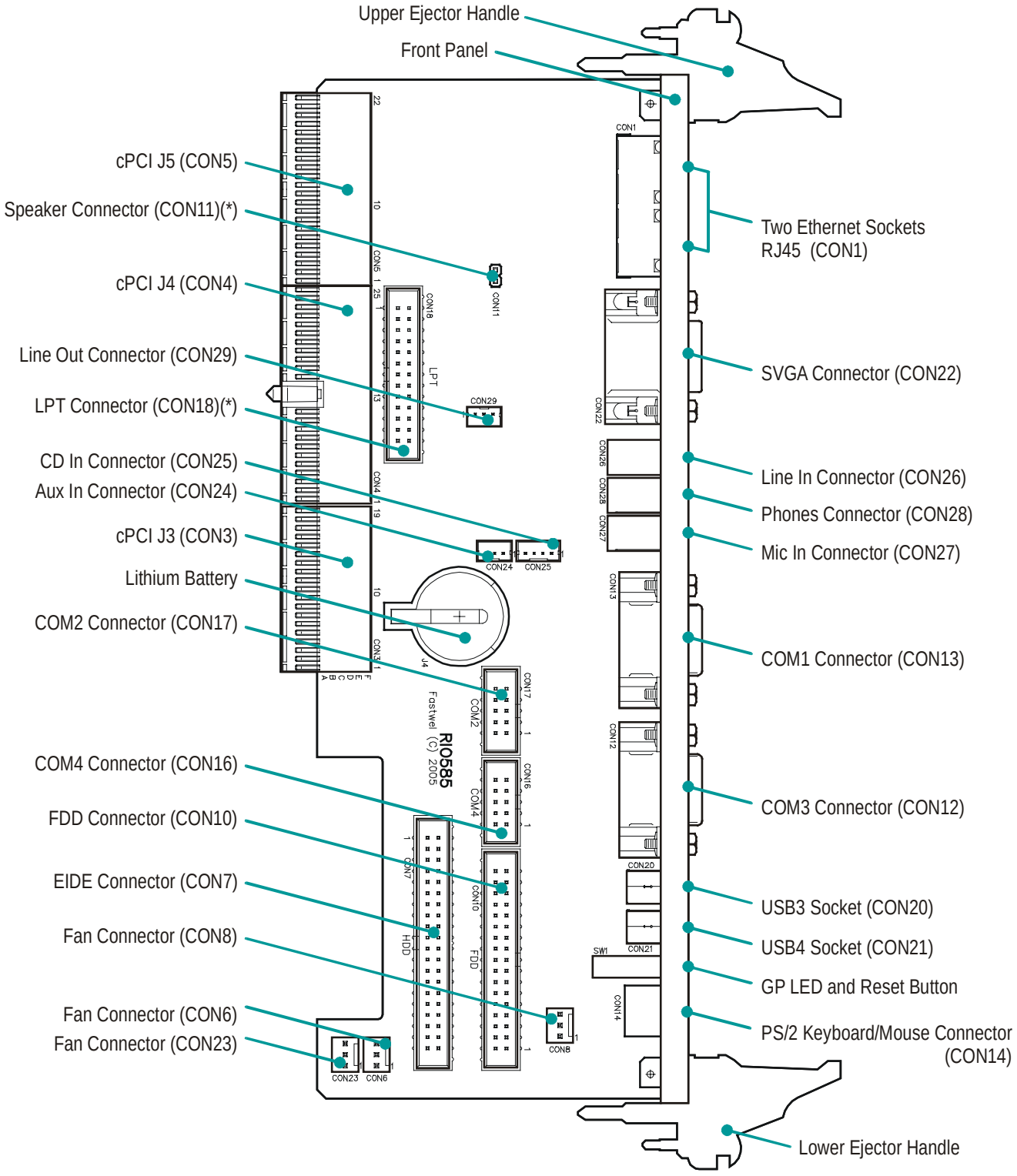
A.3 Rear I/O Modules Layout

Figure A-3: RIO581 Module Layout (Top)



The components and connectors layout may slightly differ for various versions of the module.

Figure A-4: RIO585 Module Layout (Top)



(*) - Approximate position

The components and connectors layout may slightly differ for various versions of the module.

A.4 RIO58x Delivery Checklist

The RIO58x supplied set includes:

1. RIO58x Rear I/O module
2. HDD ribbon cable, 80-threads
3. FDD ribbon cable, 34-threads
4. PS/2 Y-cable
5. Antistatic bag
6. Consumer package

Note:

Keep the antistatic bag and the original package at least until the warranty period is over. It can be used for future storage or warranty shipments.

A.5 Rear I/O Modules Interfaces

The following sections present information on Rear I/O modules interfaces. The notation RIO58x means that the description applies to both RIO581 and RIO585 modules, unless noted otherwise.

A.5.1 Overview of Modules Interfaces

A.5.1.1 Front Panel Interfaces

Interfaces available via the front panel:

- Two Gigabit Ethernet(*) channels, each with 8-pin RJ45 modular jack
- VGA-CRT interface, 15-contact female high-density D-Sub connector
- VGA-LVDS port for connection of a FlatPanel, 20-pin socket; RIO581 only (Molex 52515-2011)
- Audio connectors: MicIN, Phones, LineIN, (3.5 mm standard sockets); RIO585 only
- COM1 interface (RS485), 9-pin D-Sub connector
- COM3 interface (RS232), 9-pin D-Sub connector
- Two USB 2.0 ports, type A 4-contact sockets
- Reset button
- GP programmable LED
  (see instructions on programming in CPC501 User Manual, subsection 2.3.13.1)
- PS/2 connector for mouse and/or keyboard, 6-pin MiniDIN

(*) Two Fast Ethernet sockets for previous versions of the module.

A.5.1.2 Onboard Interfaces and Connectors

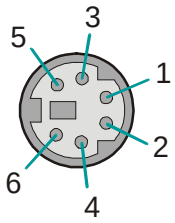
Interfaces, accessible via RIO58x onboard connectors:

- CompactPCI specification 6U rear I/O on J3, J4 and J5
- Floppy disk interface via the 34-pin 2.54 mm IDC connector
- EIDE interface via the 40-pin 2.54 mm IDC connector
- Serial interface COM2 (RS485) via the 10-pin 2.54 mm IDC connector
- Serial interface COM4 (RS232) via the 10-pin 2.54 mm IDC connector
- LPT-Interface via the 26-pin 2.54 mm IDC connector
- Audio interface (AuxIn, LineOut – 3-pin connectors; CD In – 4-pin connector), RIO585 only
- PC speaker connector (2-pin connector)
- Fan power connectors (3-pin)
- Li-battery holder for CPC501 RTC

A.5.2 Detailed Description of Modules Interfaces

A.5.2.1 Keyboard/Mouse Interface

Figure A-5: Keyboard/Mouse Connector CON14



The PC/AT standard keyboard/mouse connector CON14 is a PS/2-type 6-pin shielded mini-DIN connector. Both devices can be connected simultaneously using the Y-cable supplied with the module.

Table A-2: Keyboard/Mouse Connector CON14 Pinout

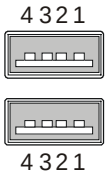
Pin Number	Name	Function	In/Out
1	KDATA	Keyboard data	In/Out
2	MDATA	Mouse data	In/Out
3	GND	GND signal	–
4	VCC	VCC signal	–
5	KCLK	Keyboard clock	Out
6	MCLK	Mouse clock	Out

Note:

The keyboard/mouse power supply unit is protected by a 500 mA fuse. All signal lines are EMI-filtered.

A.5.2.2 USB Interfaces

Figure A-6: USB Connectors CON20 and CON21



There are two identical USB 2.0 interfaces on the RIO58x module, each with a maximum transfer rate of 480 Mbps, provided for connecting USB peripheral devices. One USB device may be connected to each port. To connect more than two USB devices to the module an external hub is required.

Note:

Some USB devices may operate via the Rear I/O connectors in USB 1.1 mode.

Table A-3: USB Connectors CON20 and CON21 Pinouts

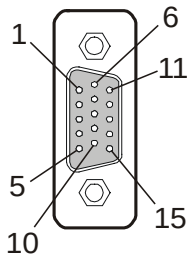
Pin Number	Name	Function	In/Out
1	VCC	VCC signal	–
2	UV0 -	Differential USB -	In/Out
3	UV0+	Differential USB+	In/Out
4	GND	GND signal	–

Note:

The maximum current for each USB port is limited to the amount of 0.5 A by the module's circuitry. All signal lines are EMI-filtered.

A.5.2.3 VGA-CRT Interface

Figure A-7: D-Sub VGA-CRT Connector CON22



The 15-contact female connector CON22 is used to connect a VGA analog monitor to the RIO58x Rear I/O module.

Table A-4: VGA Connector CON22 Pinout

Pin #	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
9	VCC	Power +5V 500 mA, fuse protection	Out
12	DDCdata	I^2C™ data	In/Out
13	Hsync	Horizontal sync. TTL	Out
14	Vsync	Vertical sync. TTL	Out
15	DDCclk	I^2C™ clock	Out
5, 6, 7, 8	GND	GND Signal	–
4, 10, 11	Free	–	–

Note:

The VGA signals are available on both rear I/O and front I/O. In this configuration both interfaces are active.

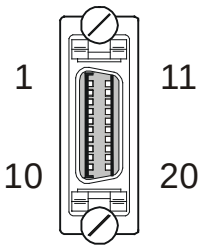
Both VGA ports are not electrically separated. Plug-n-Play capability is supported at the CPC501 and is not supported at the RIO58x.

Do not connect devices to both connectors (front I/O and rear I/O) at the same time.

The VCC power line is protected by a 500 mA fuse.

A.5.2.4 LVDS Interface (RIO581 only)

Figure A-8: LVDS Connector CON15



For connecting LVDS TFT displays, RIO581 module is equipped with a standard 20-contact LVDS connector (Molex 52515-2011) on the front panel. The pixel clock can be from 20 to 65 MHz.

Table A-5: LVDS Connector CON15 Pinout

Pin Number	Function
1	+RTX 1
2	–RTX 1
5	+RTXCLK
6	–RTXCLK
7	GND
8	VCC
11	+RTX 2
12	–RTX 2
15	+RTX 0
16	–RTX 0
17	+12V
18	RFPVEE
3, 4, 13, 14	Shield
9, 10, 19, 20	NC

A.5.2.5 Serial Port Interfaces

The serial port interfaces COM1 (CON13) and COM3 (CON12) are located on the front panel of RIO58x as 9-pin D-sub connectors, while COM2 (CON17) and COM4 (CON16) are onboard as 10-contact IDC connectors.

COM3 and COM4 are PC-compatible RS-232 serial ports with 5 V charge-pump technology with no need for a +12 V and -12 V supply. These two COM ports are fully compatible with the 16550 controller, include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer rate of up to 230.4 Kbps.

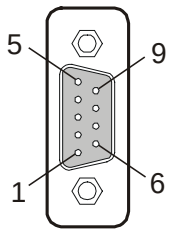
COM1 and COM2 have the half-duplex RS-485 interface with the data transfer rate of 460.8 Kbps.

The functions of each serial port interface are shown in the following table:

Table A-6: Functions of the Serial Port Interfaces

Interface	Function
COM1	RS485
COM2	RS485
COM3	RS232
COM4	RS232

Figure A-9: D-Sub Serial Connectors CON13 and CON12



The COM1 and COM3 interfaces use the 9-pin D-sub connectors on the front panel. Serial connectors' pinouts are presented in the tables below.

The Serial Port connectors' pinouts appear on the following page

The following table gives the pinout of the onboard flat cable IDC connectors COM2 and COM4.

Table A-7: Serial Port Connectors CON17 (COM2) and CON16 (COM4) Pinout

Pin	RS485 (COM2)	RS232 (COM4) (Standard PC)
1	+TRXD	DCD
2	–TRXD	DSR
3	NC	RXD
4	NC	RTS
5	NC	TXD
6	NC	CTS
7	NC	DTR
8	NC	RIN
9	GND	GND
10	NC	NC

The following table gives the pinout of the 9-pin D-sub connectors COM1 and COM3.

Table A-8: Serial Port Connectors CON13 (COM1) and CON12 (COM3) Pinout

Pin	RS485 (COM1)	RS232 (COM3) (Standard PC)
1	+TRXD	DCD
2	NC	RXD
3	NC	TXD
4	NC	DTR
5	GND	GND
6	–TRXD	DSR
7	NC	RTS
8	NC	CTS
9	NC	RIN

Note:

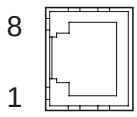
To ensure the proper functioning of the rear COM1 I/O serial interface, the driver for COM1 port on the CPC501 must be disabled using the BIOS Setup program.

Note:

The RS485 interfaces (COM1 and COM2) provide for support of up to 256 network segments. In case the module is supposed to serve as a terminal network device, it is necessary to mention this fact when ordering the module. The required SMT connection elements (J18 for COM1 and J17 for COM2) will be installed at the factory to enable 120 ohm terminal resistors.

A.5.2.6 Gigabit Ethernet Interfaces

Figure A-10: RIO58x Gigabit Ethernet Connectors



Each of the two RIO58x front panel Ethernet connectors is realized as an RJ45 connector for twisted-pair cabling. The interface provides automatic detection and switching between 10Base-T and 100Base-TX data transmission modes.

Each of the two Ethernet channels may be independently configured for the backplane (PICMG 2.16), for front I/O or for rear I/O module via the BIOS Setup (see Chapter 5 for details) or user software utility.

Note...

If the Gigabit Ethernet channel is configured for PICMG 2.16, both corresponding front panel (CPC501 and RIO58x) Gigabit connectors will have no functionality.

Note...

For some previous versions of RIO585 Rear I/O module these two connectors have Fast Ethernet functionality as a function of the two Gigabit Ethernet controllers of CPC501. They are replicates of the two Gigabit Ethernet connectors at the CPC501 front panel, but can be used as 100 Mb/s ports only. These connectors are active only if the output of the Gigabit Ethernet controller is switched to the front panel.

For these versions of the Rear I/O module:
If the Gigabit Ethernet channel 1 or 2 is configured for front panel, the cable can be connected either to the CPC501 front panel Gigabit connector, or to the corresponding Rear I/O module Fast Ethernet connector. Both connectors can not be populated at the same time.

RJ45 Connectors CON1A and CON1B Pinout

The CON1A and CON1B connectors supply the 10Base-T, 100Base-TX and 1000Base-T interfaces to the front panel of RIO58x.

Table A-9: Pinouts of Gigabit Ethernet Connectors CON1A and CON1B

Pin	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	Signal	I/O	Signal	I/O	Signal
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX–	O	TX–	I/O	BI_DA–
3	I	RX+	I	RX+	I/O	BI_DB+
4	–	–	–	–	I/O	BI_DC+
5	–	–	–	–	I/O	BI_DC–
6	I	RX–	I	RX–	I/O	BI_DB–
7	–	–	–	–	I/O	BI_DD+
8	–	–	–	–	I/O	BI_DD–

A.5.2.7 EIDE Port

Both master and slave secondary interfaces are available at the RIO58x CON7 header. The maximum length of the cable that may be used for connection of IDE devices is 50 cm.

The following table sets out the signal names and functions of the CON7 connector pins.

Table A-10: Pinout of AT Standard Secondary EIDE Connector

Pin	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	–
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	–
20	NC	–	–
21	IDEDRQ	DMA request	In
22	GND	Ground signal	–
23	IOW	I/O write	Out
24	GND	Ground signal	–
25	IOR	I/O read	Out
26	GND	Ground signal	–
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	–
29	IDEDACK	DMA Ack	Out
30	GND	Ground signal	–
31	IDEIRQ	Interrupt request	In
32	NC	–	–
33	A1	Address 1	Out
34	NC	–	–
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	NC	–	–
40	GND	Ground signal	–

A.5.2.8 Floppy Drive Interface

The RIO58x is provided with a standard FDD 2-row 34-pin male on-board connector, CON10, which accepts connection of up to two floppy drives.

Warning!

Pay attention to the correct connection of the floppy drive cable. Please, note that cable inversion will lead to continuous operation of the floppy drive, that may damage the diskette in it.

Table A-11: Floppy Drive Connector CON10 Pinout

Pin Number	Signal	Function	In/Out
2	SELECT0	Density Select 0	Out
4	NC	-	-
6	SELECT1	Density Select 1	Out
8	INDEX	Index pulse	In
10	MOTEN1	Motor 1 enable	Out
12	DRVSEL2	Driver select 2	Out
14	DRVSEL1	Driver select 1	Out
16	MOTEN2	Motor 2 enable	Out
18	DIRECTION	Step direction	Out
20	STEP	Step pulse	Out
22	WRDATA	Write data	Out
24	WREN	Write enable	Out
26	TRACK0	Track 0 signal	In
28	WRPROT	Write protect	In
30	RDDATA	Read data	In
32	HEADSEL	Head select	Out
34	DSKCHG	Disk change	In
Odd Numbers	GND	Ground signal	-

A.5.2.9 LPT Interface

The LPT interface is routed through the CON18 26-pin on-board connector. To use a standard parallel port device a special adapter is necessary.

Table A-12: LPT Interface Connector CON18 Pinout

Pin	Signal	In/Out	Pin	Signal	In/Out
1	STROBE	Out	14	GND	–
2	AUTOFD	Out	15	PD6	In/Out
3	PD0	In/Out	16	GND	–
4	ERROR	In	17	PD7	In/Out
5	PD1	In/Out	18	GND	–
6	INIT	Out	19	ACK	In
7	PD2	In/Out	20	GND	–
8	SLCTIN	Out	21	BUSY	In
9	PD3	In/Out	22	GND	–
10	GND	–	23	PE	In
11	PD4	In/Out	24	GND	–
12	GND	–	25	SLCT	In
13	PD5	In/Out	26	GND	–

A.5.2.10 Audio Interface and PC Speaker Connector

On the RIO585 module audio interface is available via three on-board pinrow connectors (CON24, CON25 and CON29), and three front panel connectors (CON26, CON27 and CON28), which are standard 3.5 mm audio jacks. Information on these connectors is collected in the table below.

Table A-13: RIO585 Audio Interface Connectors

Name	Location	Designation
Phones (CON28)	Front panel	Output to headphones
Mic In (CON27)	Front panel	Input from microphone
Line In (CON26)	Front panel	Line input
Aux In (CON24)	Board	Auxiliary line input, 3 pins
CD In (CON25)	Board	Input from CD drive, 4 pins
Line Out (CON29)	Board	Line Output, 3 pins

Both RIO581 and RIO585 modules have an on-board 2-pin PC-speaker connector (CON11). If the polarity of the speaker matters, please, connect "–" of the speaker to the contact #1 of the CON11.

Table A-14: Audio Connectors CON24, CON25 and CON29 Pinouts

CON24		CON25		CON29	
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	AUX_IN_R	1	CD_IN_R	1	LINE_OUT_R
2	GNDA	2	CD_IN_COMM	2	GNDA
3	AUX_IN_L	3	CD_IN_COMM	3	LINE_OUT_L
–	–	4	CD_IN_L	–	–

A.5.2.11 Fan Control Interface

The fan control connectors (CON6 and CON8) and the connector for an external cooling fan (CON23) are located on board of RIO58x modules. They have the following pinouts:

Table A-15: Fan Connectors CON6, CON8 and CON23 Pinouts

CON6		CON8		CON23	
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	Ground	1	Ground	1	Ground
2	Fan Supply Voltage	2	Fan PWM1	2	External Fan Power
3	Fansense 2	3	Fansense 1	3	NC

A.5.2.12 CompactPCI Interface

RIO58x modules are equipped with CON3, CON4 and CON5 CompactPCI connectors.

CompactPCI Connectors J3-J5 (CON3-CON5) Pinouts

The RIO58x modules are provided with three female rear I/O connectors J3, J4 and J5. For reference regarding similar connectors of the CPC501, please refer to Chapter 2, "Detailed Description" of this Manual.

Table A-16: Backplane J3 (CON3) Pin Definitions

Pin#	Z	A	B	C	D	E	F
19	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
18	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
17	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
16	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
15	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
14	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
13	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
12	GND	FD_DS0	FD_DENSEL1	FD_MTR0	FD_INDEX	FD_WDATA	GND
11	GND	FD_DS1	FD_DSKCHG	FD_MTR1	FD_DENSEL0	FD_RDATA	GND
10	GND	FD_WP#	FD_HDSEL	FD_DIR	FD_TRK0	FD_STEP	GND
9	GND	FD_WGATE#	SIDE_D15	SIDE_D14	SIDE_D13	USB0+	GND
8	GND	SIDE_D12	SIDE_IOW	VCC	SIDE_IOR	USB0-	GND
7	GND	SIDE_A2	SIDE_A1	SIDE_A0	SIDE_D0	SIDE_D1	GND
6	GND	SIDE_D2	SIDE_D3	SIDE_D4	SIDE_D5	SIDE_D6	GND
5	GND	RSVD	PMDAT	SPKR	KDAT	RSVD	GND
4	GND	PRST	PMCLK	VCC	KCLK	COM3_RXD	GND
3	GND	COM3_CTS	COM3_RTS	COM3_DSR	COM3_DCD	COM3_TXD	GND
2	GND	SIDE_D7	SIDE_D8	COM3_RI	COM3_DTR	COM4_RXD	GND
1	GND	SIDE_D9	SIDE_D10	SIDE_D11	BATT	COM4_TXD	GND

Table A-17: Backplane J4 (CON4) Pin Definitions

Pin#	Z	A	B	C	D	E	F
25	GND	VCC	RSVD	RSVD	+3.3V	VCC	GND
24	GND	RSVD	PD0	INIT	RSVD	SIDE_IRQ	GND
23	GND	+3.3V	RSVD	RSVD	VCC	SIDE_RST	GND
22	GND	RSVD	PD1	RSVD	SIDE_CHRDY	RSVD	GND
21	GND	+3.3V	RSVD	AUTOFD	SIDE_CS1	RSVD	GND
20	GND	RSVD	PD2	SLCTIN	RSVD	RSVD	GND
19	GND	+3.3V	PD3	STROBE	SIDE_CS0	GND	GND
18	GND	RSVD	PD4	RSVD	RSVD	LAN2_MDI2+	GND
17	GND	+3.3V	PD5	BUSY	SIDE_DACK	LAN2_MDI2-	GND
16	GND	RSVD	PD6	RSVD	RSVD	LAN2_MDI3+	GND
15	GND	+3.3V	PD7	ACK	SIDE_DRQ	LAN2_MDI3-	GND
14	GND	Key area					GND
13	GND						GND
12	GND						GND
11	GND	AC_SDOUT	RSVD	PE	DDC_DATA	LAN1_MDI3-	GND
10	GND	RSVD	RSVD	RSVD	RSVD	LAN1_MDI3+	GND
9	GND	RSVD	RSVD	SLCT	DDC_CLOCK	LAN1_MDI2-	GND
8	GND	AC_SDIN	GND	RSVD	RSVD	LAN1_MDI2+	GND
7	GND	GND	LVDS_TXP2	ERROR	RSVD	GND	GND
6	GND	AC_BITCLK	LVDS_TXN2	RSVD	RSVD	USB_OC#	GND
5	GND	GND	GND	LVDS_TXP1	RSVD	RSVD	GND
4	GND	AC_SYNC	GND	LVDS_TXN1	GND	GND	GND
3	GND	RSVD	LVDS_FPVEE	GND	LVDS_TXP0	LVDS_TXCLKP	GND
2	GND	AC_RST#	RSVD	GND	LVDS_TXN0	LVDS_TXCLKN	GND
1	GND	VCC	RSVD	GND	+12V	VCC	GND

= RSVD for RIO585

= RSVD for RIO581

Table A-18: Backplane J5 (CON5) Pin Definitions

Pin#	Z	A	B	C	D	E	F
22	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
21	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
20	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
19	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
18	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
17	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
16	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
15	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
14	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
13	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
12	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
11	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
10	GND	+3.3V	RSVD	RSVD	RSVD	RSVD	GND
9	GND	TDN2	RDN2	COM1_RXD	TDN1	RDN1	GND
8	GND	TDP2	RDP2	COM1_TXD	TDP1	RDP1	GND
7	GND	COM2_ENABLE	COM1_ENABLE	COM1_RTS	USB1+	RSVD	GND
6	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
5	GND	COM2_RXD	COM2_TXD	COM2_RTS	RSVD	RED_OUT	GND
4	GND	RSVD	RSVD	RSVD	RSVD	HSYNC	GND
3	GND	COM4_DTR	COM4_CTS	COM4_DSR	GP_LED	BLUE_OUT	GND
2	GND	COM4_RTS	COM4_RI	FAN_SENSE2	RSVD	VSYNC	GND
1	GND	COM4_DCD	GND	FAN_SENSE1	USB1-	GREEN_OUT	GND

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Appendix B

B Supplementary Information

B.1 Related Standards and Specifications

The Fastwel's CompactPCI modules comply with the requirements of the following standards:

Table B-1: Related Standards

Type	Standard	Test Parameters
CE: Emission	EN50081-1	–
CE: Immission	EN61000-6-2	–
CE: Electrical safety	EN60950	–
Mechanical dimensions	IEEE 1101.10	–
Vibration (sinusoidal)	IEC60068-2-6-82; Fc	2 g / 10-500 Hz / 10 (acceleration / frequency range / test cycles per axis)
Permanent shock	IEC60068-2-29-87; Eb	30 g / 11 ms / 1000±10 / 1 s (peak acceleration / shock duration half sine / number of shocks / recovery time)
Single shock	IEC60068-2-27-87; Ea	50 g / 9 ms / 18 / 5 s (peak acceleration / shock duration / number of shocks / recovery time in seconds)
Reduced atmospheric pressure	IEC 60068-2-13-83, M	9 kPa (1.305 psi); approx. corresponds to 17000 m (over 55700 ft) above sea level

Important...

Some versions of the module may have the test results differing from the ones presented in the above table. For more information please contact Fastwel's official representatives.

Information related to this product and its components can be found in the following specifications:

Table B-2: Related Specifications

Product	Specification
CompactPCI Systems and Boards	CompactPCI Specification 2.0, Rev. 3.0 CompactPCI Packet Switching Backplane Specification PICMG 2.16 Rev. 2.0 CompactPCI System Management Specification PICMG 2.9 Rev. 1.0 CompactPCI Hotswap Specification PICMG 2.1 Rev. 2.0
PMC Add-on Modules and Carriers	Draft standard for Common Mezzanine Card Family: P1386, Draft 2.4a Draft standard for Physical and Environment Layers for PCI Mezzanine Cards: P1386.1, Draft 2.4
CompactFlash Cards	CF+ and CompactFlash Specification Revision 1.4

Appendix C

C Useful Abbreviations, Acronyms and Short-cuts

Abbreviation	Meaning
IPMI	Intelligent Platform Management Interface
IPMB	Intelligent Platform Management Bus (IPMI)
BMC	Baseboard Management Controller (IPMI) In a CompactPCI chassis, there can be only one BMC present.
PM	Peripheral Management Controller (IPMI) The PM is a microcontroller located on the peripheral device in a CompactPCI system. It handles the measurements and the protocol stack.
I^2C™	Inter Integrated Circuit Two-thread serial protocol, used in SMB and IPMI
KCS interface	Keyboard Controller Style interface (IPMI) Interface for communication between control software and BMC, similar to a keyboard controller interface
BT interface	Block Transfer interface (IPMI) Block transfer interface for communication between control software and BMC
Satellite	Satellite Controller (IPMI) In a CompactPCI chassis, there can be several satellites. Each satellite is connected to the other modules via the dual port IPMB interface.
SEL	System Event Log (IPMI) The SEL repository is present only in the BMC.
SDR, SDRR	Sensor Data Record, Sensor Data Record Repository (IPMI) The SDRR is only present in the BMC. Normally, the SDRR contains all sensor records of the chassis.
SMB	System Management Bus
SMS	System Management Software
DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory
SODIMM	Small Outline Dual In-Line Memory Module
ECC	Error Correction Code Data error correction technology used in memory modules
FWH	Firmware Hub Nonvolatile memory chip, part of Intel chipset, used for BIOS storage in CPC501
GMCH	Graphics and Memory Controller Hub
DAC	Digital-Analog Converter
USB	Universal Serial Bus
LPC	Low Pin Count External devices communication interface
UART	Universal Asynchronous Receiver-Transmitter
UHCI	Universal Host Controller Interface USB Host Controller Interface
EHCI	Enhanced Host Controller Interface (Universal Serial Bus specification)
UTP	Unshielded Twisted Pair
CRT-display	Cathode Ray Tube Display

Abbreviation	Meaning
PMC	PCI (Peripheral Component Interconnect) Mezzanine Card
CMC	Common Mezzanine Card
LVDS	Low Voltage Differential Signal Digital monitors communication specification
RTC	Real Time Clock
BIOS	Basic Input-Output System
PC	Personal Computer
PICMG	PCI Industrial Computer Manufacturers Group
AHA	Accelerated Hub Architecture GMCH and ICH4 communication bus specification
AGP	Accelerated Graphics Port
AGTL	Advanced Gunning Transceiver Logic PSB (Processor Side Bus) signal exchange specification
SMBus	System Management Bus
EEPROM	Electrically Erasable Programmable Read-Only Memory
NAND Flash	Not And (electronic logic gate) Flash memory specification
SSD	Solid State Disk
PLCC	Plastic Leaded Chip Carrier
RAMDAC	Random Access Memory Digital-to-Analog Converter
DAC	Digital-to-Analog Converter
DVMT	Dynamic Video Memory Technology
TTL	Transistor-Transistor Logic
ECP/EPP	Extended Capabilities Port / Enhanced Parallel Port Parallel port specifications
FDD	Floppy Disk Drive
EIDE	Enhanced Integrated Drive Electronics Mass storage devices interface
DMA	Direct Memory Access
PIO	Programmed Input/Output EIDE: Directly processor controlled data exchange
Rear I/O Module	Rear Input-Output Module Auxiliary interface module, which is connected to the cPCI backplane rear connectors
PWM output	Pulse-Width Modulation Cooling fan control technique
ESD	Electrostatically Sensitive Device Electrostatic Discharge
ACPI	Advanced Configuration and Power Interface
POST	Power On Self Test
cPCI	CompactPCI Industrial automation systems standard
EOS	Electrical Overstress
MDI	Media Dependent Interface Interface with connection type automatical detection