CPC510

3U Compact PCI
CPU Board

User Manual

Revision 1.00

The product described in this manual is compliant with all related CE standards.

Product Title: CPC510
Document name: CPC510 User Manual
Manual version: 1.00
Reference document: IMEC.421459.510

Revision Record

Revision No.	Brief description of changes	Board index	Revision date
1.00	Initial version	CPC510	April 2013

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NOTATIONS

CAUTION HIGH VOLTAGE!
This symbol and sign warns you about the dangers related to electric discharges (> 60 V) when touching the device and its components. Non-compliance with the safety measures mentioned or prescribed by the rules may pose a danger to your life or health or could damage the product. Please read the below subparagraph related to how to handle high voltages.

ATTENTION! ELECTROSTATIC SENSITIVE DEVICE!
This symbol and sign informs you that the electronic boards and their components are sensitive to static electricity. Therefore, it is required to be extra extra cautious when handling and testing it so as to ensure its integrity and working capacity of the device.

ATTENTION! HOT SURFACE!
This symbol and sign warns you about the danger of touching a hot surface of the device.

ATTENTION!
This sign encourages you to pay attention to the Manual's aspects, which incomplete understanding and ignoring may pose a danger to your health or could lead to the equipment damages.

NOTE!
This sign indicates that there are text fragments which require careful consideration.

Safety requirements

This product of Fastwel LLC has been developed and tested in order to provide the compliance with the electric safety requirements. Its design provides for a longtime failsafe operation. The product life cycle can be sufficiently reduced due to its improper use during unpacking and installation process. Therefore, for the sake of your safety you'll need to comply with the below listed recommendations in order to provide the correct operation of the device.

HIGH VOLTAGE SAFE HANDLING PROCEDURES

ATTENTION!
All the works with this device should be performed only by the employees who have sufficient qualification to do it.

CAUTION, HIGH VOLTAGE!
Before installing the board into the system, please make sure that the mains supply has been switched off. This also refers to installation of mezzanine boards. In the course of installation, repairs and maintenance of the device there is a serious risk of electric shock therefore always unplug the power cord at the time of operation. This also refers to other feeder cables.
.

BOARD HANDLING PROCEDURES

Electrostatic Sensitive Device (ESD).
The electronic boards and their components are sensitive to the static electricity. Therefore it is required to pay additional attention while handling these devices in order to ensure their safety and operability.

- Store this product in its protective packaging while it is not used for operational purposes.

- If possible, unpack or pack this product only at EOS/ESD safe workplaces. Otherwise, it is important to be electrically discharged before touching the product. This can be done by touching a metal part of your system case with your hand or tool. It is particularly important to observe antistatic precautions when setting jumpers or replacing components.

- If the product contains batteries for RTC or memory back-up, ensure that the module is not placed on conductive surfaces, including antistatic mats or sponges. This can cause short-circuit and result in damage to the battery and PCB.

TRANSPORTATION, UNPACKING AND STORAGE

Transportation

The device should be transported in original manufacturer's separate packaging (transport packaging), which contains an individual antistatic bag and a cardboard box, in the closed transport (automobile, railway, air transportation in heated and pressurized compartments) in storage conditions 5 defined in the IEC 721-2-1 standard (GOST standard 15150-69) or in storage conditions 3 during sea transportation.
The packaged modules should be transported in accordance with the shipping rules, specified for this particular type of transport.
During handling and transportation operations, the packaged modules should not undergo sharp pounding, falls, shocks and exposure to atmospheric precipitation. The goods should be stored in a carrier vehicle in such a manner which will prevent their moving.

Unpacking

Prior to unpacking, before transportation at subzero temperature of ambient air the modules should be kept within 6 hours under storage conditions 1 defined in the IEC 721-2-1 standard (GOST standard 15150-69).
It is prohibited to place the packaged module close to the heat source, prior to unpacking.
Retain all original packaging at least until the warranty period is over. You may need it for shipments or for storage of the product.

After unpacking the product, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socketed components), contact Fastwel's official distributor from which you have purchased the product for additional instructions.

Storage

Module storage conditions for group 1 are defined in the IEC 721-2-1 standard (GOST standard 15150-69).

MANUFACTURER'S WARRANTY

Warranty Liabilities

The Manufacturer hereby guarantees the product conformity with the requirements of the 4013-025-72782511-09 technical conditions provided that the Consumer complies with the operating, storage, transportation and installation conditions and procedures, specified by the accompanying documents.
The Manufacturer hereby guarantees that the products supplied thereby are free from defects in workmanship and materials, provided operation and maintenance norms were observed during the currently established warranty period. The Manufacturer's obligation under this warranty is to repair or replace free of charge any defective electronic component being a part of a returned product. Products that broke down through the Manufacturer's fault during the warranty period will be repaired free of charge. Otherwise the Consumer will be invoiced as per the current labor remuneration rates and expendable materials cost

Liability Limitation Right

The Manufacturer shall not be liable for the damage inflicted to the Consumer's property because of the product breakdown in the process of its utilization.

Warranty Period

The warranty period for the products made by Fastwel Group is 24 months since the sale date (unless otherwise provided by the supply contract).
The warranty period for the custom-made products is 36 months since the sale date (unless otherwise provided by the supply contract.

Limitation of warranty liabilities

The above warranty liabilities shall not be applied:
To the products (including software), which were repaired or were amended by the employees, that do not represent the manufacturer. Exceptions are the cases where the customer has made repairs or made amendments to the devices in the strict compliance with instructions, preliminary agreed and approved by the manufacturer in writing;
To the products, broken down due to unacceptable polarity reversal (to the opposite sign) of the power supply, improper operation, transportation, storage, installation, mounting or accident.

Returning a product for repair

1. Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization.
2. Attach a failure inspection report with a product to be returned in the form, accepted by the Manufacturer, with a description of the failure circumstances and symptoms.
3. Place the product in the consumer packaging (antistatic bag) and cardboard box, in which the product had been supplied. Failure to package in antistatic material will VOID all warranties of the Customer on a unilateral basis.
4. The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer

1. Introduction

1.1. Overview

CPC510 is a highly integrated 3U CPCI Serial solution for using in real time systems, manufacturing control, high-speed collection and processing of data. CPC510 is another product in the range of 3U CPCI modules manufactured by Fastwel Group.

The board is based on the Intel Ivy Bridge CPU (2- or 4-core CPUs) which has one of the highest performances in its class.

CPC510 uses high speed I/O interfaces (PCI-Express, Gigabit Ethernet) and modern technologies for video data processing. Modular structure of the device enables a flexible setting of the system for particular fields, which optimizes a price-quality relationship.

To expand CPC510 functionalities, MIC584 mezzanine module is used. Its detailed description is given in the User Manual.

Stable operation of CPC510 enables its use in all industrial applications. Components, on which CPC510 is based, are carefully selected in accordance with the embedded system applicability criteria which make the module perfectly fit for the long life cycle systems.

The module has the following structure of I/O channels:
- 2 GB/s Ethernet controllers (2x routed to the front panel);
- 12x USB 2.0 ports supporting HS, FS and LS data rates (2x on the front panel, 2x on the mezzanine, 8x on the backplane connector);
- 4x USB 3.0 ports (routed to the backplane connector)
- 6x SATA ports (4x ports are routed to the backplane connector, 1x - to the mezzanine board, 1 – switchable: backplane/mezzanine board)
- 1x DisplayPort, routed to MIC590 board (to the front panel of CPC510-02)
- 1x LVDS, routed to MIC590 board
- 2x DisplayPorts on the front panel.
- HD Audio, routed to the mezzanine connector.
- LPC, routed to the mezzanine connector.

1.2. Technical characteristics

- **Intel Ivy Bridge CPU** (with 2 or 4 cores)

- **RAM:**
- DDR3 SDRAM 1333, 1600 MHz or DDR3L SDRAM 1066, 1333 MHz with ECC, up to 8 GB, soldered, 2x channels.

- **Video output (simultaneous output to 3 displays):**
- 2x DisplayPort connectors (resolution up to 2560x1600@60 Hz), routed to the front panel.
- DisplayPort Interface (resolution up to 2560x1600@60 Hz), routed to MIC590 board (to the front panel of CPC510-02)
- LVDS interface dual channel 25-112 MHz, 18/24 bit/pixel (compatible with ANSI/TIA/EIA-644 specification), routed to MIC590 (LVDS connector is located on MIC590 board, CPC510-02 version, see Fig. A-1)

- **LPC bus**
- Routed to the mezzanine connector

- **PCI-E bus**
- Processor hosts. Support of PCI-E 2.0 (up to 5 GT/s)
- Routed via PCI-E switch to J1 and J2 CPCI Serial connectors supporting up to two devices x8
- Support of the Non-Transparent operation mode for FatPipe#1
- Routed to PCI-E switch to the J4 CPCI Serial connector supporting x4 devices
- PCH hosts. PCI-E 2.0 support (up to 5 GT/s)
- Routed to the mezzanine board, on the left side. Supports up to 3-x PCI Express devices x1 in accordance with PICMG 2.30 specification.

- **SMBUS**
- Compatibility with 2.0 specification.
- Speed up to 100 Kbps

- **FLASH BIOS:**
- 2 x 32 Mb SPI-Flash

- **MicroSD interface**
- Support of SDHC 2.0
- Connected to USB 2.0 interface

- **SATA interface:**
-Support of RAID 0, 1, 5, 10

- **SATA II interface**
One interface is permanently routed to the mezzanine connector:
- Single interface – switchable between the backplane and mezzanine connectors;
- 2x ports are routed to the backplane connector.

- **SATA III interface:**
- 2x interfaces are routed to the backplane connector.

- **2x LAN 10/100/1000 Mbit ports on PCI-E x4 Gen2:**
- 2x ports are routed to the front panel connectors.
- Implementation of a server network adapter.

- **USB ports:**
- 13x USB 1.1 ports (12 Mb/s), USB 2.0 (480 Mb/s) and 4 USB 3.0 ports (4.8 Gb/s).
- 2x USB2.0 ports are routed to the front panel connectors.
- 2x USB2.0 ports are routed to the mezzanine connector.
- 8x (4x) USB2.0 ports are routed to the backplane connector *.
- 1x USB2.0 port is used for implementation of MicroSD interface.
- 4x USB3.0 ports are routed to the backplane connectors *.

** when using USB 3.0, 4x USB 2.0 ports are utilized by USB 3.0 ports*

- **FRAM**
- 32 KB, where 1 KB is intended for Bios Setup settings.
- implemented with SPI FPGA bus.

- Real time clock:
- Supplied by CR2032 (3 B) lithium battery.

- **Audio:**
- HD Audio interface, routed to the mezzanine connector.

- **Watchdog timer:**
- Internal, with a possibility of programmed control

- **SGPIO interface:**
- Support for signaling according to the SFF-8485 Specification.

- **Hardware monitor**
- Implemented via SMBUS interface.
- Monitoring of three supply voltages
- Monitoring of the CPU temperature
- Monitoring of the PCB temperature

- **Indication:**
- Board Startup Diagnostics LED / Hot Swapping LED
- SATA Drives Access LED
- Temperature state LED
- PCI Express Interconnections state LED
- Two software-controlled LEDs (user-defined).
- **OS Compatibility:**
- Windows 7
- Linux 2.6

- **Power Requirements**:
- Power voltage +12V, +5V_STBY (optional).

- **Operating temperature range**:
- Industrial Modification: from 40°C to +85°C.
- Commercial Modification: from 0°C to +70°C.

- **Humidity**:
- Up to 80% non-condensing.
- **Vibration / Single shock resistance**:
- 5g/100g.

- **MTBF**:
- No less than 100,000 hours.

- **Weight**:
- CPC510-01 with heat sink – no more than 550 g;
- CPC510-02 (with MIC590) with heat sink – no more than 700 g.

1.3. CPC510 hardware configurations

CPC510 is currently manufactured according to the following table:

Table 1-1: CPC510 hardware configurations

CPC510 CPU Board		Variable data for the versions			
		CPC510	MIC590	Temperature range	
				0...+70°	-40°...+85°
-01	CPC510-01-i72C1.7-RAM4096MB-R1-C	-01	-	+	-
-02	CPC510-01-i72C1.7-RAM4096MB-R2-I			-	+
-03	CPC510-01-i72C2.5-RAM4096MB-R2-C	-02		+	-
-04	CPC510-02-i72C1.7-RAM4096MB-R1-C	-03	+	+	-
-05	CPC510-02-i72C1.7-RAM4096MB-R2-I			-	+
-06	CPC510-02-i72C2.5-RAM4096MB-R2-C	-04		+	-

There are two (except for the module with i72C2.5 CPU) types of hardware configurations:

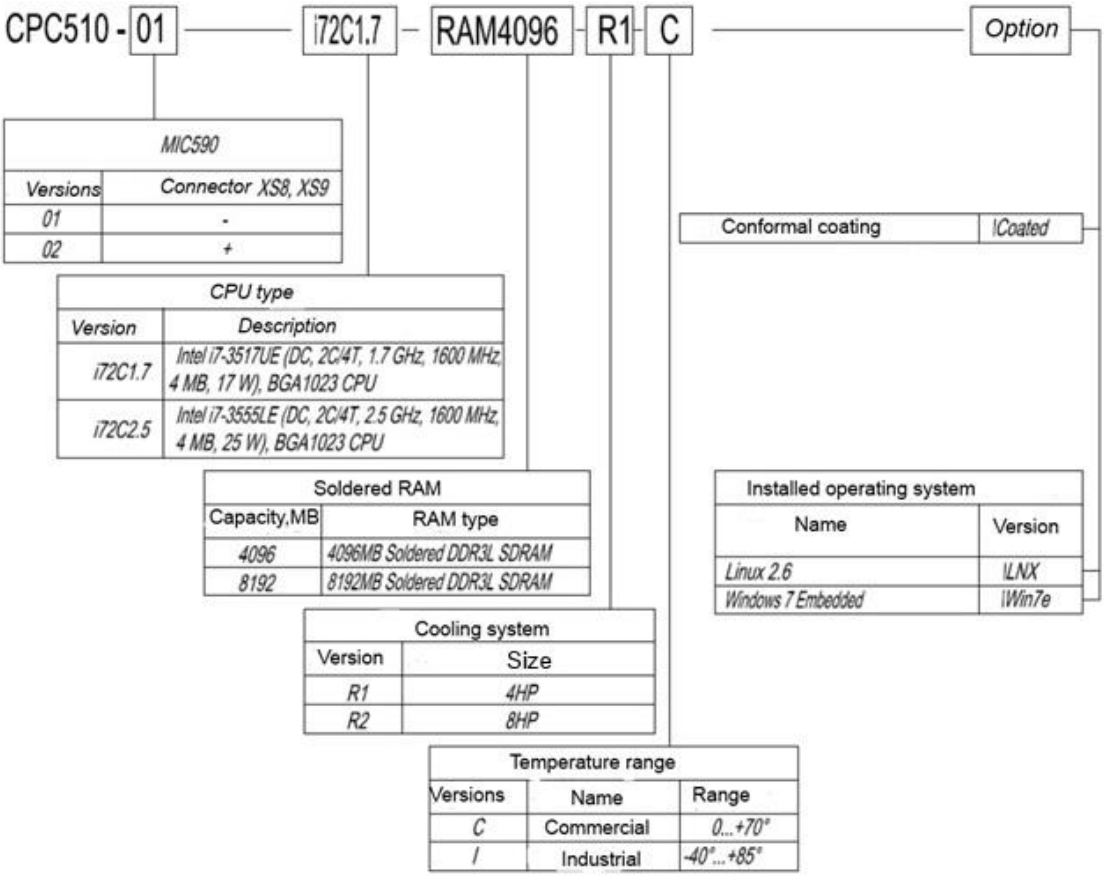
- (from - 40 to +85°C) – for industrial operating temperature range;

- (from 0 to +70°C) – for commercial temperature range.

Configurations with 2.5 GHz CPUs should be equipped with the forced air cooling systems, see subparagraph **7.1.3 Board cooling recommendations**.

By using an order sample, client may choose a required version (see Fig. 1-1).

Fig. 1-1: Configuration table of CPC510



1. CPC510 board with i7-3555LE CPU (2,5 GHz) is manufactured for a commercial operating temperature range (from 0 to + 70°C).
2. All CPC510 versions with 2.5 GHz CPUs are manufactured with high-profile heat sinks R2 (8 HP).
3. CPC510 versions with 1.7 GHz CPU for industrial temperature range are manufactured with high-profile heat sinks R2 (8HP).

Heat sink R1 is made in 4HP size (see Fig. 1-2 External view of CPC510-01 with the installed heat sink R1), heat sink R2 is a combined version: 4HP/8HP.
CPC510-02 version (see Fig. 1-1) includes MIC590 board. MIC590 is installed to the left from CPC510 CPU Board. MIC590 is designed for extending CPC510 functionalities (additional video ports). More detailed information on MIC590 is given in the Annex A.

1.4. CPC510 delivery checklist

The board delivery kit contains:
-CPC510 or CPC510 along with MIC590 (board of video/ PCI bridge functionalities extension).
- Package.
- The following boards will be supplied as an option:
- MIC584 - mezzanine board with the extended I/O functionalities.
- KIC550 board. Carrier-board, 2,5” storage device or 2,5” SSD.

1.5. Package

CPC510 is packed in a box with the following dimensions: 350 x 260 x 70 mm.

Weight of the packed boards, in kg, no more than	CPC510-01	0,9
	CPC510-02	1,05

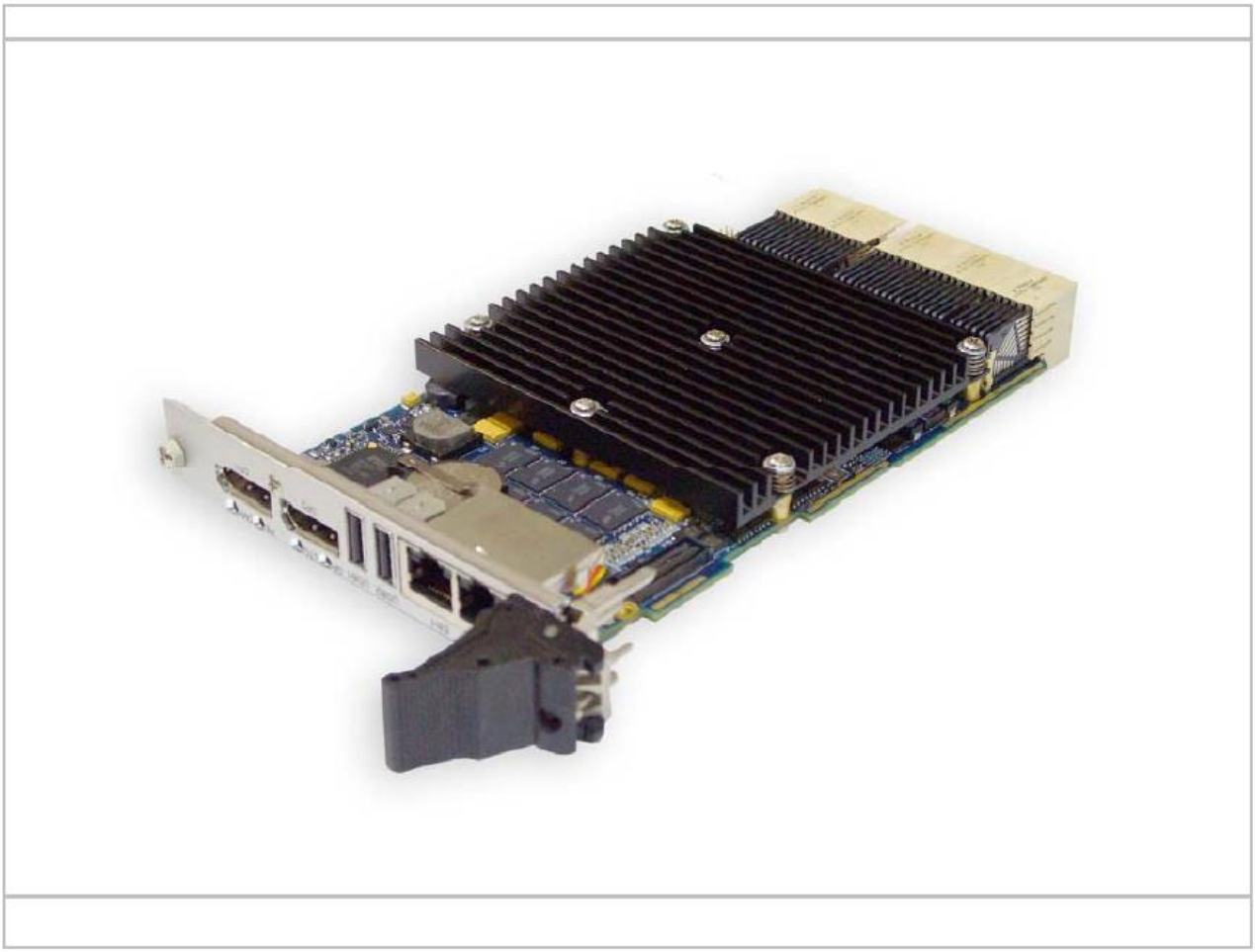
Note
Retain all original packaging at least until the warranty period is over. You may need it for shipments or for storage of the product.

1.6. External view and element layout

The following figures will help to identify components, understand their relationship and functions. The versions might have some insignificant variations, not shown on diagrams and photos.

1.6.1 External view of CPC510

Fig. 1-2: External view of CPC510-01with the installed heat sink R1

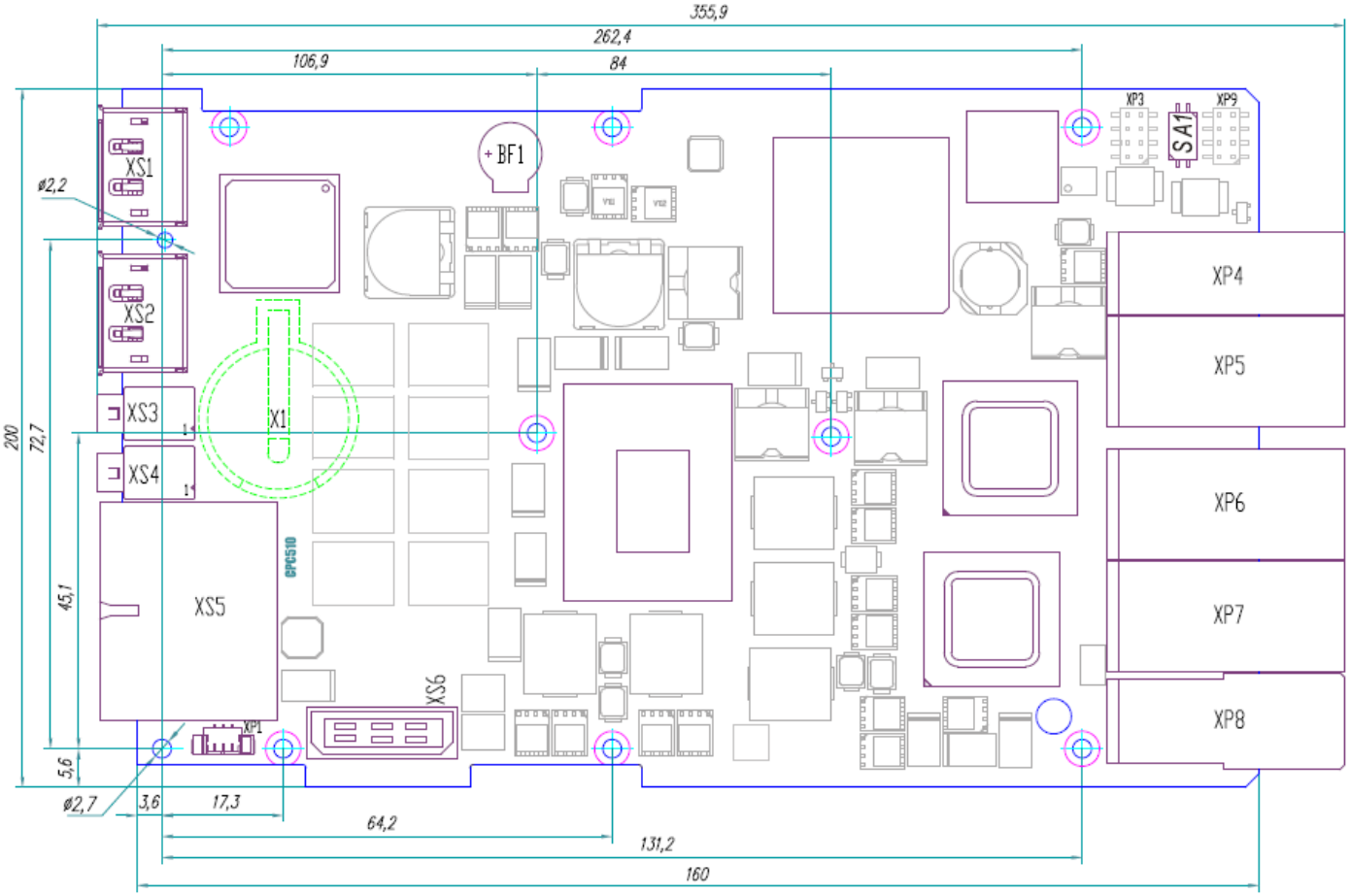


External view of the board versions might have some variations from the one shown on the Figure.

The Figure shows CPC510-01 version with the installed heat sink R1 (4HP).

1.6.2 Layout of main components

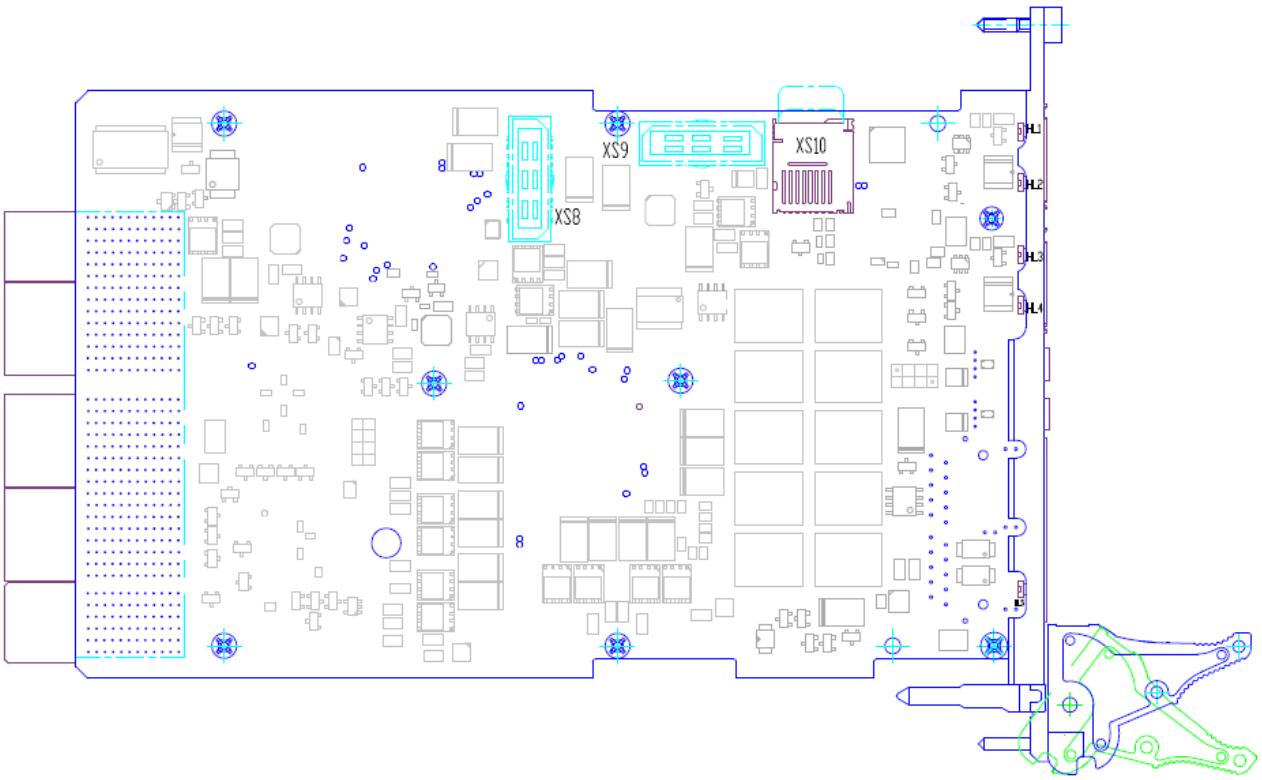
Fig. 1-3: Layout of main components of CPC510 (top view)



External view of the board versions might have some variations from the one shown on the Figure.

This figure shows the top side of CPC510. Heat sink is not shown.

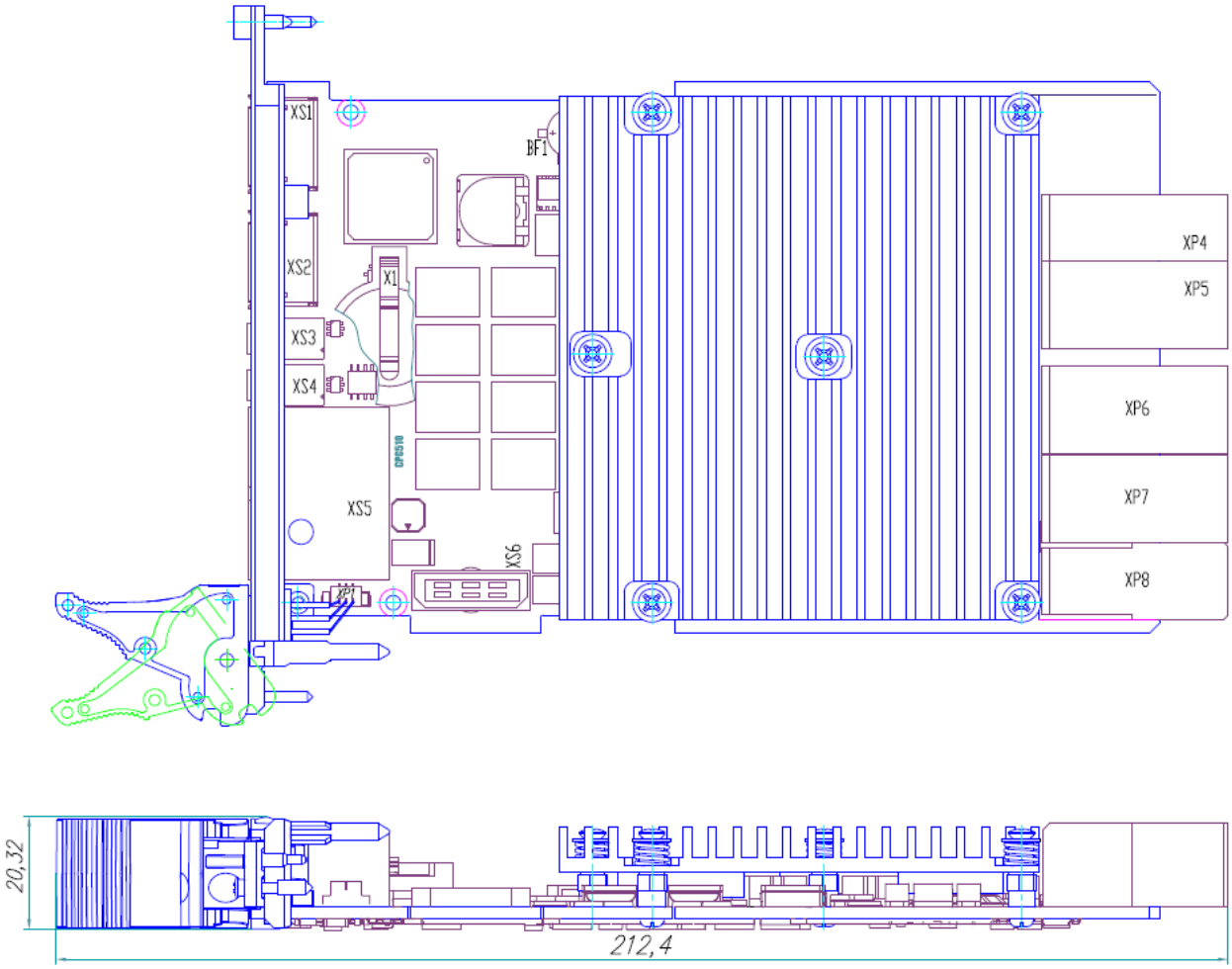
Fig. 1-4: Layout of CPC510 main components (top view)



External view of the board versions might have some variations from the one shown on the Figure.

This Figure shows the lower side of CPC510 board. As opposed to CPC510-02, version CPC510-01 has no XS8 and XS9 connectors (For CPC510 version see Fig. 1-1).

Fig. 1-5: CPC510-01 board with the installed heat sink R1



External view of the board versions might have some variations from the one shown on the Figure.

Heat sink with a profile increased for the purpose of heat removal improvement (no more than 15,2 mm from the board level), makes no obstacles for the board use in CompactPCI sub-rack.

Fig. 1-6: CPC510-01 Board with the installed heat sink R2 (8HP)

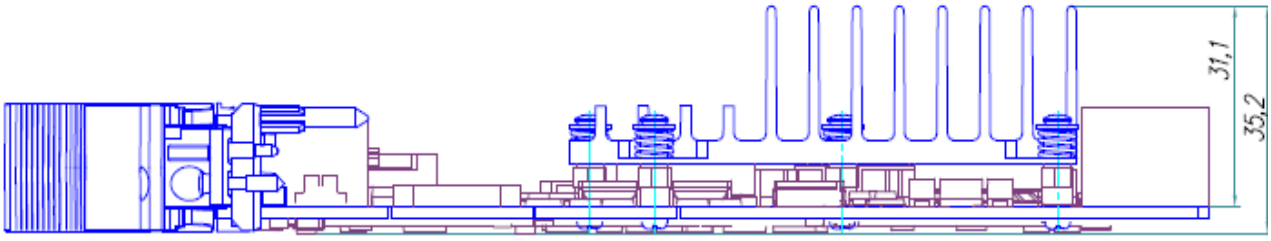


Fig. 1-7: CPC510-02 Board with the installed heat sink R1 (4HP) and MIC590

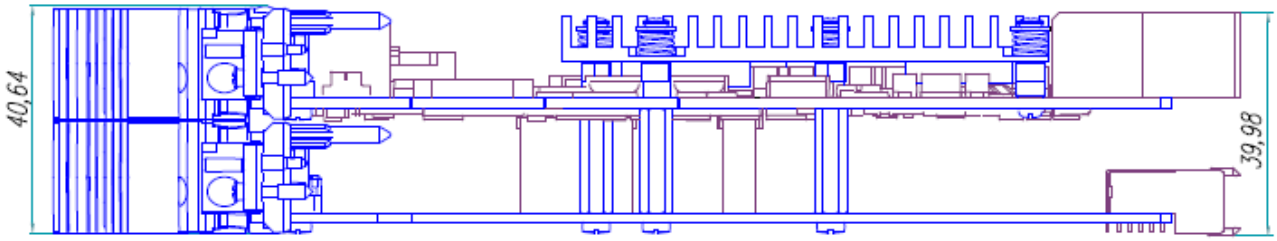
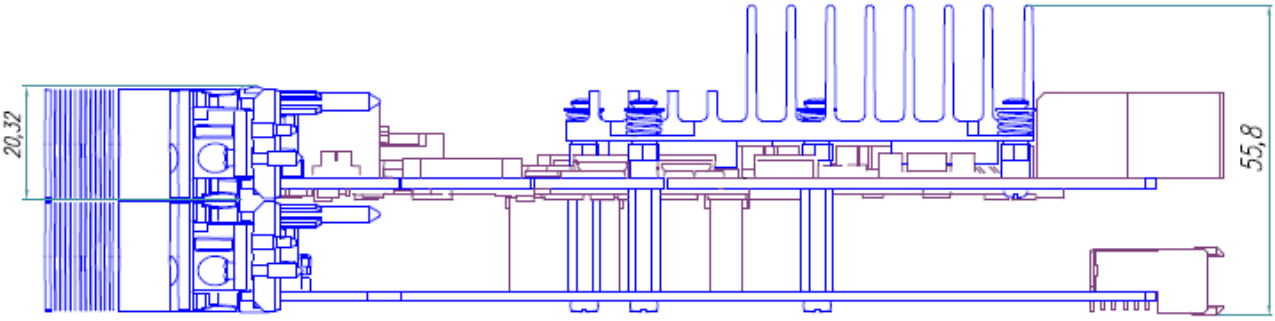


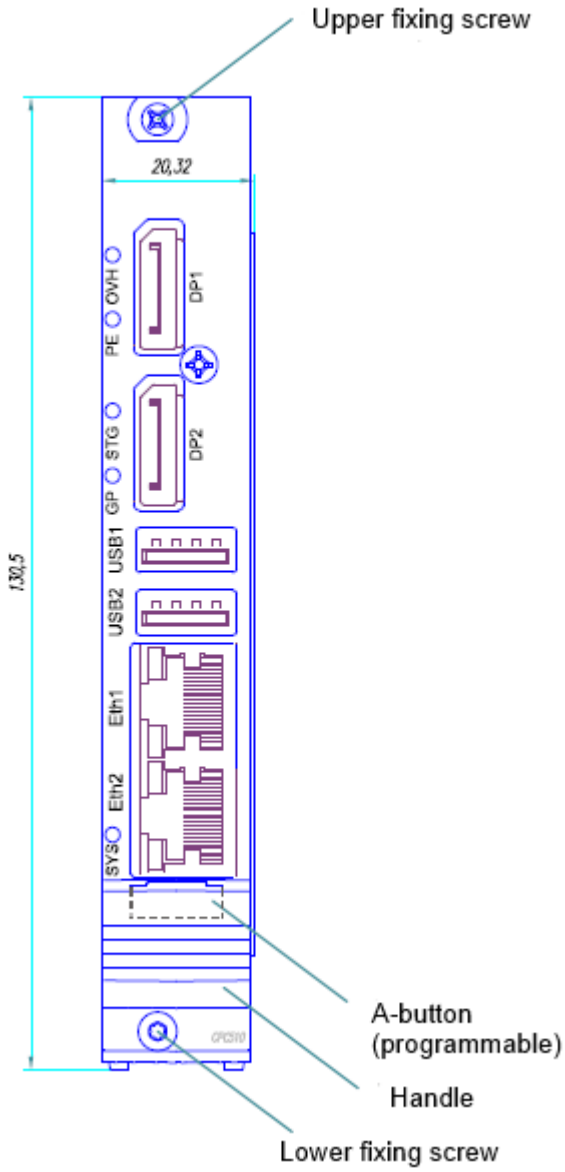
Fig. 1-8: CPC510-02 Board with the installed heat sink R2 (8HP) and MIC590



External view of the board versions might have some variations from the one shown on the Figure.

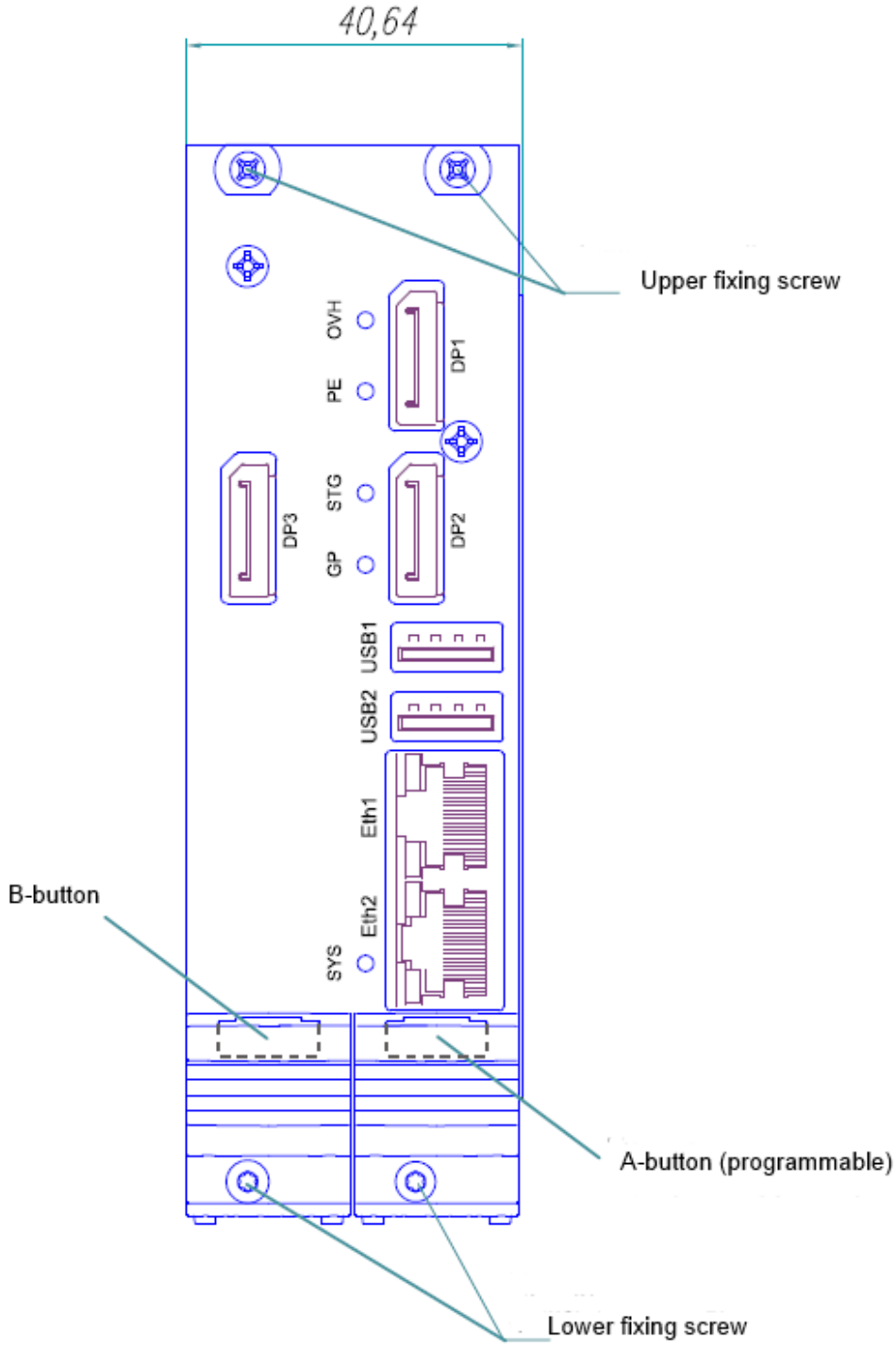
1.6.3 Front panel

Fig. 1-9: Front panel of CPC510-01



External view of the board versions might have some variations from the one shown on the Figure.

Fig. 1-10: Front panel of CPC510-02



External view of the board versions might have some variations from the one shown on the Figure.

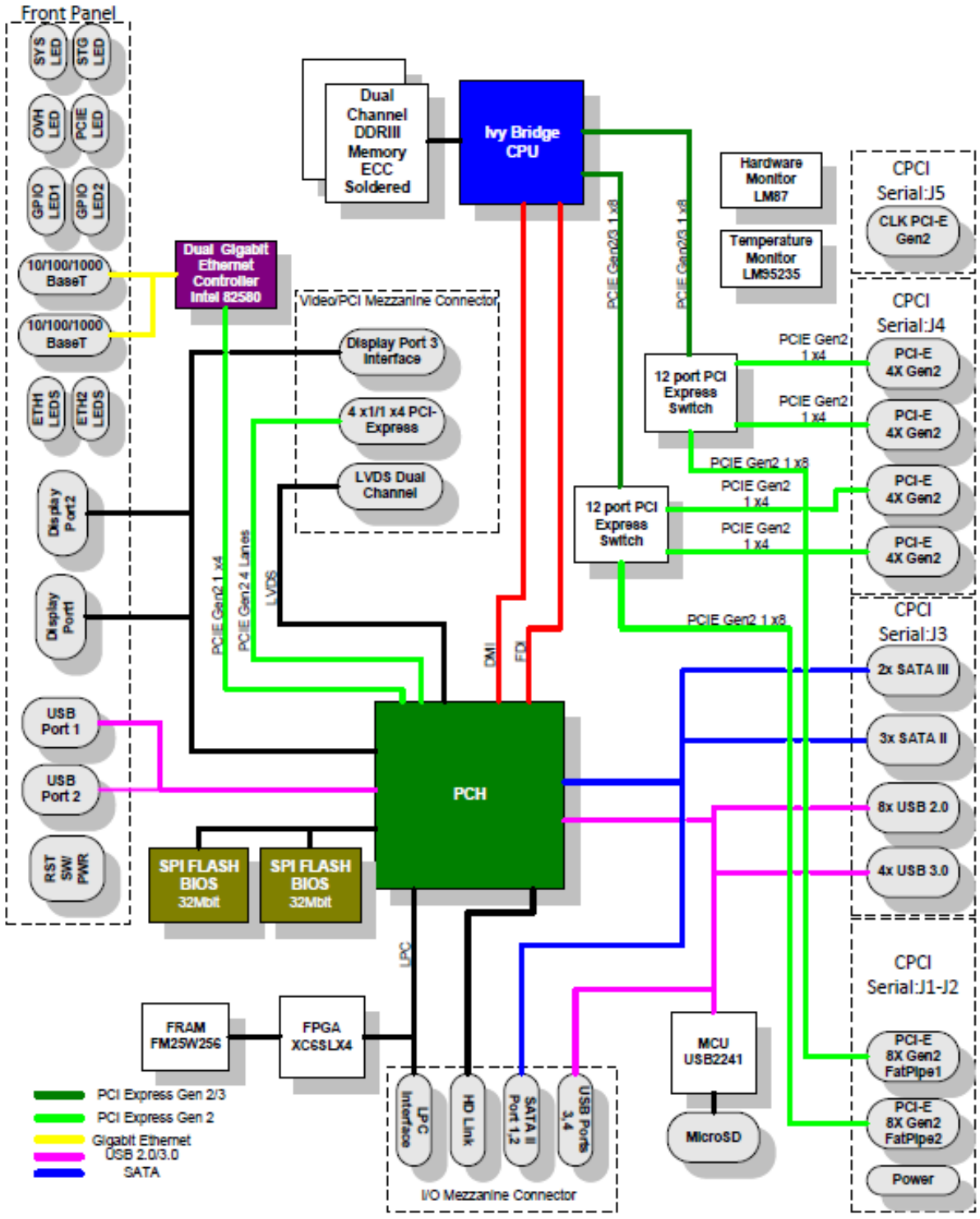
A and B buttons have mechanical functions: they are intended for installation/de-installation of CPC510 board (see subparagraphs 4.2 Installation procedure of CPC510 and 4.3 De-installation procedure).

Apart from that, A button is a programmable switch designed for manual power off/reset, if necessary.

2. Specifications

2.1. Block diagram

Fig. 2-1: Block-diagram of CPC510



2.2. Peculiarities of functional units

• **Intel IvyBridge CPU**
Intel 32- bit 2-/ 4- cores CPU is based on the improved Nehalem core with 22 nm technology. The CPU is a highly-integrated solution combining several CPU cores, 2-channel SDRAM/DDR3 and DDR3L controller with ECC memory support and 3D/2D graphics adapter. The CPU is designed for application in embedded systems and is implemented in BGA package.

• **Panther Point PCH**
Highly integrated interface controller including standard IBM PC AT platform peripherals.

• **MEMORY**
The board can have up to 8GB DDR3 SDRAM 1333, 1600MHz or DDR3L
SDRAM 1066, 1333MHz soldered.
• **BIOS**
For storing BIOS, two SPI-bus based 32 Mb Flash microchips are used.

• **RTC, CMOS**
Real time clock is integrated into PCH. When the power is switched off, RTC is powered from a lithium battery installed on the board. BIOS Setup settings are stored in FRAM.

• **FRAM FM25W256.**
Nonvolatile memory 256 Kb, may be used for storing user data and BIOS SETUP settings.

• **MicroSD. Bridge USB2241.**
The board is equipped with MicroSD interface connected to USB 2.0 port.

• **Ethernet controller Intel 82580**
The board has 2 built-in Gigabit Ethernet interfaces. 2 ports are routed to the front panel connectors. Interfaces are implemented in Intel high-speed server controller.

• **USB 2.0**
The board is equipped with 13 USB 2.0 channels:
- 2x USB2.0 ports are routed to the front panel connectors.
- 2x USB2.0 ports are routed to the mezzanine connector.
- 8x (4) USB2.0 ports are routed to the backplane connector.
- 1x USB2.0 port is used for MicroSD interface.

• **USB 3.0**
The board has 4x USB 3.0 channels. They are routed to the backplane connector.
When the board is installed in the peripheral slot, USB-interface routed to the J1 connector is switched off automatically.

• **SATA interface:**
SATA II and SATA III interfaces are used (RAID 0, 1, 5, 10 support).

SATA II
4x interfaces for connection of storage devices are routed to the mezzanine connector and backplane connector.

SATA III
2x interfaces for connection of storage devices are routed to the backplane connector.

• **Display Port**
The ports are intended for the connection of digital display with DisplayPort interface or for further conversion to other video standards. Maximum resolutions supported: (2560x1600@60 GHz).
2x ports are routed to the front panel of the board.
1x port is routed to MIC590 (front panel of CPC510-02).

• **LVDS interface**
LVDS-interface is designed for the connection of digital panel with LVDS interface dual channel 25-112 MHz, 18/24 bit/pixel (compatible with ANSI/TIA/EIA- 644DisplayPort specification or for the further conversion to other video standards. Maximum resolutions supported: (1600x1200@60 GHz). LVDS is routed to MIC590 (LVDS-connector is shown on Fig. A-1)

• **PCI-E x4 interface. PCI-E Switch PLX8624.**
4x PCI-E Gen2 x4 channels are routed to J4 CPCI Serial connectors. They make it possible to connect 3U Compact PCI Serial extension boards with a set of links x1, x2, x4 (5 Gb/s).

• **PCI-E x8 interface (FAT Pipe). PCI-E Switch PLX8624.**
2x PCI-E Gen2 x8 channels are routed to J1 and J2 CPCI Serial connectors. They make it possible to connect Compact PCI Serial extension boards with a set of links x1, x2, x4, x8 (5 Gb/s). Support of the NON-Transparent mode (FatPipe#1 port) for implementation of multiprocessor systems.

• **4x channel PCI-E interface. PCH Host.**
4-x PCI-E Gen2 channels are routed to the mezzanine connector on the left side. They enable to implement a PCI-E bridge to PCI/PCI-X on MIC590, which will offer an opportunity to create Legacy/Serial hybrid systems.

• **SPI**
The interface is implemented in FPGA on LPC bus. Supports FRAM memory chip (located on the board). Maximum clock frequency: 25 MHz.

• **Audio**
Support can be implemented via mezzanine.

• **Watchdog**
Hardware reset timer is implemented in FPGA on LPC bus.

• **Reset and power supply monitoring**
CPU reset signal is generated from the following sources:
-supervisor - when power supply is switched on;
-“Reset” button (button on the ejector handle of the CPU module);
-Watchdog timer;
-Reset# signal of PCI bus (in the Slave mode).

• **Switches (Jumpers)**
The board is equipped with the switches having the following functions (see paragraph 5):
- BIOS Setup reset to default settings;
- Forced selection of the Transparent mode.

• **Indication**
User LEDs for start diagnostics and operation of storage devices are routed to the front panel. The LEDs are described in subparagraph 2.6.

2.3 System extension possibilities

In order to connect peripherals to the board, especially, video/audio interfaces and serial ports, it is required to use interface modules: mezzanines boards - MIC584 (mezzanine I/O extension board), MIC590 (mezzanine board (included into CPC510-02), see Section A MIC590 board); interface module KIC550 for extension of CPU board functionalities - see Table 2-1:
MIC584 Board contains the following set of interfaces:
• 2xUSB 2.0
• 2xSATA
• Audio IN/OUT/MIC
• 4xRS-232
• 2xRS-485
• LPT
• PS/2 keyboard +mouse
KIC550 Board contains the following set of interfaces:
• 1xUSB 2.0/3.0
• 2.5” SATA storage device
• CFast
MIC590 board contains the following set of interfaces:
• 1xDisplayPort
• Dual channel LVDS interface with illumination control
• PCI-E bridge to PCI/PCI-X

Table 2-1: Interface modules used for improvement of CPC510 I/O functionalities

Product number	Description	Connector
MIC584	Mezzanine extension module (description is given in the User Manual)	XS6 connector
MIC590 (the board is installed in CPC510-02)	Mezzanine extension board	Internal connectors of CPC510-02
KIC550	Interface Module for extension of the CPU board functionalities (description is given in the User Manual)	Compact PCI Serial connector

MIC584 is connected from the right side of CPC510 CPU board, while MIC590 is installed on the left side. One of the major advantages to install modules in such a way is that you don't have to use cable connections, which makes it easier to install or de-install CPU module from the system enclosure.

2.4 Peripherals

CPC510 has the following peripherals:

2.4.1 Timers

CPC510 is equipped with various types of timers:

- **RTC - Real-Time Clock**

PCH contains real-time clock compatible with MC146818A, with 256 bytes of battery-powered C-MOS memory. The clock has functions of time-keeping, alarm-clock, programmable function of intermittent interruption and a calendar for 100 years.

- **Counter/Timer**

Similar as with PC/AT, the module has three 8254 type counters/timers, integrated to PCH.

- **Additional timer**

PCH includes an additional programmable timer that prevents system blocking during its startup. With the first timer overrun, signal SMI# is generated which calls a subroutine to exit the program "hanging" of the system. If the timer overruns for the second time, then a system "Reset" signal is generated for release the system from hanging.

-**Watchdog Timer**

The watchdog timer is meant to eliminate system blocking both at the time of its startup, and during its operation. When the watchdog is actuated, "Reset" signal, interruption or SMI are generated. Actuation time is set via BIOS Setup menu. During the system startup, BIOS code execution is controlled by the watchdog timer.

2.4.1.1 Watchdog timer

The watchdog is implemented in FPGA as a device based on the LPC bus. The watchdog timer consists of 24-digit register of the counter [Timer Current Value Register], decremented at the frequency of 32,768 kHz, and initial value register [Timer Initial Value Register]. When the counter register is set to zero, either interruption, or NMI, or automatic board reset can be generated. Response time can be set from 0 up to 512 seconds, at a pitch of 30,52μs.
Without the preliminary initialization, a default delay period of the watchdog timer actuation shall amount to a maximum value of 512 seconds. Below you can find formula for calculation of the duration of actuation delay TWD (μs) depending on the Timer Initial Value Register (KWD):
TWD [μs] = KWD * 106/ 215

E.g. KWD = 1 (000001h) corresponding to the time of actuation delay 30,52μs, and the KWD = 16777215 (FFFFFFh) –of the delay time which is 512 seconds.
Counter reset to the initial value can be carried out in a number of different ways:
- By entering any figure in the counter register [Timer Current Value Register]
- By entering any figure in the port 80h (the mode is switched on in [Timer Init Register])
- By writing or reading using addresses in two windows (basic window addresses are specified in the relevant registers [Window Base Address], address mask is specified in the register [Windows 1&2 Address mask register], the mode is selected in [Timer Init Register]). Window size is from 1 to 16 byte, depending on the value in the mask register.

Access to watchdog timer registers

Device configuration is based on Plug-and-Play architecture. Registers of the watchdog timer can be accessed via standard I/O registers (index and data), when entering the configuration mode.

CONFIG PORT	302h	Write
INDEX PORT	302h	Read/Write
DATA PORT	303h	Read/Write

Configuration mode

The device enters the configuration mode when the following configuration key is written in the CONFIG PORT:
Configuration key = <46h><57h>
Device exits the configuration mode when the following configuration key is written in the CONFIG PORT:
Configuration key = <57h><46h>
INDEX and DATA ports are available only in configuration mode.

Device programming

Sequence of operations during device programming:

- Enter configuration mode:
MOV DX, 302H
MOV AL, 46H
OUT DX, AL
MOV AL, 57H
OUT DX, AL

- Write LDN to the register
(watchdog timer has a logical number 1):
MOV DX, 302H
MOV AL, 7
OUT DX, AL
MOV DX, 303H
MOV AL, 1
OUT DX, AL

- Watchdog timer's registers are available for writing and reading. E.g., reading of the 3eh register status and writing its value back:
MOV DX, 302H
MOV AL, 3EH
OUT DX, AL
MOV DX, 303H
IN AL, DX
OUT DX, AL

- Exit the configuration mode:
MOV DX, 302H
MOV AL, 57H
OUT DX, AL
MOV AL, 46H
OUT DX, AL

Global configuration registers

INDEX	Type	HARD RESET	Configuration register
7h	R/W	01h	LDN

Logical Device Number register (index 7h)

Index = 7h		
Bit	**Name**	**Description**
7:0	LDN	Write/Read: Writing to this register selects the logical device

Configuration registers of the logical device 1 (WDT)

INDEX	I/O PORT ADDRESS	TYPE	HARD RESET	CONFIGURATION REGISTER
30h	-	R/W		Activate
38h	Base+0	R/W		Timer current value [7:0]
39h	Base+1	R/W		Timer current value [15:8]
3ah	Base+2	R/W		Timer current value [23:16]
3bh	Base+3	R/W	00h	Timer initial value [7:0]
3ch	Base+4	R/W	40h	Timer initial value [15:8]
3dh	Base+5	R/W	00h	Timer initial value [23:16]
3eh	Base+6	R/W	00h	Status register
3fh	Base+7	R/W	03h	Control register
60h	-	R/W		Base[15:8] - I/O port base address bits[15:8]
61h	-	R/W		Base[7:3] - I/O port base address bits[7:3] Base[2:0] - should be 0;
70h	-	R/W	00h	Primary interrupt select
F0h	-	R/W	00h	Reserved
F1h	-	R/W	00h	Timer Init Register
F2h	-	R/W	00h	Window 1 base address bits[7:0]
F3h	-	R/W	00h	Window 1 base address bits[15:8]
F4h	-	R/W	00h	Window 2 base address bits[7:0]
F5h	-	R/W	00h	Window 2 base address bits[15:8]
F6h	-	R/W	FFh	Window 1 Mask bits [7:4] Window 2 Mask bits [3:0]

Activate register

Index = 30h		
Bit	**Name**	**Description**
7.1	-	Not used
0	Activate	Write/Read: 1 – This logical device is switched on 2 – This logical device is switched off

I/O port base address registers

Index = 60h		
Bit	**Name**	**Description**
7:0	I/O_Base_Adress[15:8]	Write/Read: Bits 15:8 of the base address of current logical device
Index = 60h		
Name		**Description**
7:0	I/O_Base_Adress[7:0]	Write/Read: Bits 7:0 of the base address of current logical device

Primary interrupt select register (index 70h)

Index = 70h		
Bit	**Name**	**Description**
7:4	-	Not used
3:0	Interrupt_select	Write/Read: 00h – Interrupt is switched off 01h – IRQ1 02h – SMI 03h – IRQ3 04h – IRQ4 05h – IRQ5 06h – IRQ6 07h – IRQ7 08h – IRQ8 (interrupt is switched off) 09h – IRQ9 0ah – IRQ10 0bh – IRQ11 0ch – IRQ12 0dh – IRQ13 (interrupt is switched off) 0eh – IRQ14 (interrupt is switched off) 0fh – IRQ15 (interrupt is switched off)

Timer Init register

Index = F1h		
Bit	**Name**	**Description**
7:5	-	Not used
4	P80E	Write/Read: Counter reset when data is written to port 80h 1 – switched on 0 –switched off
3	WND2_WR_EN	Write/Read Counter reset with the write cycle to window 2 1 – switched on 0 – switched off
2	WND2_RD_EN	Write/Read Counter reset with the write cycle to window 2 1 – switched on 0 – switched off
1	WND1_WR_EN	Read/Write Counter reset with the write cycle to window 1 1 – switched on 0 – switched off
0	WND1_RD_EN	Write/Read: Counter reset with the write cycle from window 1 1 – switched on 0 – switched off

Window 1 port base address registers

Index = f2h		
Bit	**Name**	**Description**
7:0	Window1_Base_Adress[7:0]	Write/Read: Bits 7:0 of the base address of window 1
Index = f3h		
Bit	**Name**	**Description**
7:0	Window1_Base_Adress[15:8]	Write/Read: Bits 15:8 of the base address of window 1

Window 2 port base address registers

Index = f4h		
Bit	**Name**	**Description**
7:0	Window2_Base_Adress[7:0]	Write/Read: Bits 7:0 of the base address of window 2
Index = f5h		
Bit	**Name**	**Description**
7:0	Window2_Base_Adress[15:8]	Write/Read: Bits 15:8 of the base address of window 2

Windows 1&2 address mask register

Index = f6h		
Bit	**Name**	**Description**
7:4	Window1_MASK[3:0]	Write/Read: Bits 3:0 of the address mask of window 1
3:0	Window2_MASK[3:0]	Read/Write: Bits 3:0 of the address mask of window 2

Description of I/O registers of WDT controller

Timer Current Value Register [23:0]

Base+0h		
Bit	**Name**	**Description**
7:0	Timer_Current_Value[7:0]	Write/Read: Bits 7:0 of the counter's current value
Base=+1h		
Bit	**Name**	**Description**
7:0	Timer_Current_Value[15:8]	Read/Write: Bits 15:8 of the counter's current value
Base=+2h		
Bit	**Name**	**Description**
7:0	Timer_Current_Value[23:16]	Read/Write: Bits 23:16 of the counter's current value

Timer Initial Value Register [23:0]

Base+3h		
Bit	**Name**	**Description**
7:0	Timer_Initial_Value[7:0]	Read/Write: Bits 7:0 of the counter's initial value
Base=4h		
Bit	**Name**	**Description**
7:0	Timer_Initial_Value[15:8]	Read/Write: Bits 15:8 of the counter's initial value
Base=+5h		
Bit	**Name**	**Description**
7:0	Timer_Initial_Value[23:16]	Read/Write: Bits 23:16 of the counter's initial value

Status Register

Base+6h		
Bit	**Name**	**Description**
7:3	-	Redundant
2	STM	Read/Write: Flag of the second timeout. Set in "1" provided that TMF=1 and RSTE=1. Reset by writing "1".
1	SME	Read: Flag of SMI generation per timeout. If SMI mode is selected in the interrupt register, the flag will be set in "1"(index 70h).
0	TMF	Write/Read: Timeout flag. The flag is set into "1", when the timer counter is set to zero. In which case an interrupt will be generated for the flag. Reset is carried out by writing "1" or writing to 80h port or when windows 1 and 2 are addressed (if these modes are switched on).

Control Register

Base+7h		
Bit	**Name**	**Description**
7:2	-	Redundant
1	CNTE	Write/Read: Counter decrement 1 – Switched on 0 – Switched off
0	RSTE	Read/Write: Board reset per timeout 1 – Reset is allowed 0 – Reset is prohibited

2.4.2 Battery

CPC510 uses one 3.0 V lithium battery for RTC power supply. Please, use Panasonic BR2032 or compatible batteries (see 4.4.3 Battery change). The board can function without battery, in which case the real time clock will not work.

2.4.3 Devices on local SMBus

CPC510 has SMBus (System Management Bus), which ensures functions of system monitoring and configuration. This bus uses 2-wire interface I2C™. It enables to connect several serial access devices (microchips of LM87 hardware monitor, memory EEPROM, clock-signal generator).

Table 2-2: Addresses of SMBus devices

No.	SMB Address	Device
1	0D2H	Clock-signal generator SLG8SP533V
2	0A0H и 0A2H	Memory module SPD EEPROM
3	5CH	Hardware monitor LM87 (PCB & CPU Sensor)
4	4CH	Temperature monitor LM95235 (RAM Sensor)

Two temperature monitors control CPU crystal die and memory chips temperature. The temperature monitor, upon request may provide information to software tools of current system state control, which enables operation of the board in the safe temperature mode.

2.4.4 Nonvolatile memory

2.4.4.1 MicroSD

The board is equipped with XS10 connector for the MicroSDHC type card (see Page 1-4: Location of main CPC510 components (bottom view)). MicroSD interface utilizes one of the internal USB 2.0 ports.

2.4.4.2 High-speed FRAM memory for storing user date

The board is equipped with a high-speed FRAM-memory module (32 KB) used to store proprietary information: 1 KB, used by manufacturer and 31 KB for critical user data.
Registers and FRAM device programming are described further.

2.2.4.2.1. FRAM registers (logical device 3)

No.	SMB Address	Type	HARD RESET	Configuration register
30h	-	R/W		Activate
2	0A0H и 0A2H			
3	5CH			

For using FRAM, it is required to set a base device address and activate it (LDN=3) similarly as with the watchdog timer. Further FRAM operation is carried out in the field of I/O regarding the set base address. Bit <0> in the control register (Base+3) activates an automatic mode of address increase during write/read of data register (base+2).

2.2.4.2.2. FRAM module programming

Sequence of operations during device startup:
- Enter the configuration mode

```
MOV DX, 302H
MOV AL, 46H
OUT DX, AL
MOV AL, 57H
OUT DX, AL
```

- Write LDN to the register
(FRAM has logical number 3)

```
MOV DX, 302H
MOV AL, 7
OUT DX, AL
MOV DX, 303H
MOV AL, 3
OUT DX, AL
```

- Set the base address of the device in the I/O field (e.g. 310h):

```
MOV DX, 302H
MOV AL, 60H
OUT DX, AL
MOV DX, 303H
MOV AL, 3H
OUT DX, AL
```

```
MOV DX, 302H
MOV AL, 61H
OUT DX, AL
MOV DX, 303H
MOV AL, 10H
OUT DX, AL
```

- Activate the device:

```
MOV DX, 302H
MOV AL, 30H
OUT DX, AL
MOV DX, 303H
MOV AL, 1H
OUT DX, AL
```

- Exit the configuration mode:

```
MOV DX, 302H
MOV AL, 57H
OUT DX, AL
MOV AL, 46H
OUT DX, AL
```

Further operation with FRAM is in I/O field by the addresses 310h-313h.

- Writing a byte of data (32h) to FRAM by the address (144h)

```
MOV DX, 310H
MOV AL, 44H
OUT DX, AL
MOV DX, 311H
MOV AL, 01H
OUT DX, AL
MOV DX, 312h
MOV AL, 32h
OUT DX, AL
```

- Writing a byte of data from FRAM by the address (101h)

```
MOV DX, 310H
MOV AL, 01H
OUT DX, AL
MOV DX, 311H
MOV AL, 01H
OUT DX, AL
MOV DX, 312h
IN AL, DX
```

2.5 Board interfaces

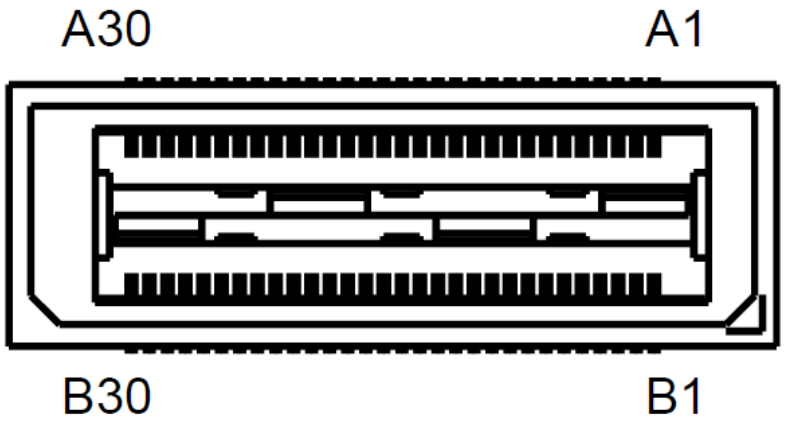
2.5.1 CompactPCI Serial connectors

CPC510 is developed in accordance with CompactPCI Serial bus architecture.
The board uses five connectors of CompactPCI Serial interfaces (see Fig. 1-3: Location of main components on CPC510 board (top view)). CompactPCI Serial standard enables to use the device under severe operation conditions with the increased number of extension connectors.

2.5.2 Connector for mezzanine board installation

In order to connector peripherals to the board, interface boards are used, see Table 2-1: Interface boards used to expand I/O functionalities of CPC510. MIC584 mezzanine board is connected on the right side of CPC510 CPU board to the XS6 connector (Connector Socket High Speed, 60 pin), see Fig. 1-3 and Fig. 2-2.
Description of MIC584 is given in the relevant User Manual.
MIC590 is installed on the left side of CPC510 (version -02). An extension slot closest to CPC510 will be used. CPC510-02 board is supplied pre-assembled, together with MIC590 (see Fig. 1-7 and Fig. 1-8).

Fig. 2-2: XS6 connector for installation of MIC584 mezzanine board



XS6 connector is located at the top of CPC510 (see Fig. 1-3: Location of main components on CPC510 (top view)).

Table 2-3: Purpose of the XS6 connector's contacts for installation of MIC584

Contact	Purpose
A1	+5V
A2	+5V
A3	USB_PN0
A4	USB_PP0
A5	GND
A6	-
A7	-
A8	GND
A9	SATA_TXN1
A10	SATA_TXP1
A11	GND
A12	AZ_BITCLK
A13	GND
A14	AZ_SYNC
A15	AZ_RST#
A16	AZ_SDIN
A17	AZ_SDOUT
A18	+3.3V
A19	KBRST#
A20	A20GATE
A21	+3.3V
A22	PLT_RST#
A23	GND
A24	CLK_33MHZ
A25	GND
A26	CLK_14MHZ
A27	GND
A28	CLK_32KHZ
A29	GND
A30	+5VA

Contact	Purpose
B1	+5V
B2	+5V
B3	USB_PN1
B4	USB_PP1
B5	GND
B6	-
B7	-
B8	GND
B9	SATA_RXN1
B10	SATA_RXP1
B11	GND
B12	LPC_AD0
B13	LPC_AD1
B14	LPC_AD2
B15	LPC_AD3
B16	LPC_FRAME#
B17	GND
B18	SERIRQ
B19	+3.3V
B20	DRQ0#
B21	+3.3V
B22	SMB_CLK
B23	SMB_DATA
B24	GND
B25	USB_OC#0
B26	USB_OC#1
B27	+3.3VA
B28	INIT_3V3
B29	BIOS_DIS#
B30	+5VA

2.5.3 Keyboard/mouse interface

CPC510 makes is possible to connect keyboard/mouse via USB port on the front panel. In addition to it, PS/2 keyboard/mouse interface is implemented on MIC584 via LPC interface and is available via MIC584 extension board (see description of MIC584 given in the relevant User Manual). Connector for keyboard and mouse (PS/2 6-pin MiniDIN connector) are located on the front panel of MIC584.

CPC510 has a keyboard controller emulator which is program-compatible with 8042, and is implemented in FPGA. This is required for proper operation of the supported operating systems when CPC510 is used without MIC584.

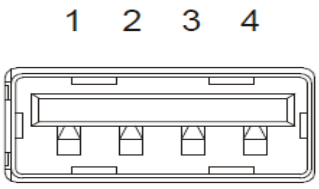
2.5.4 USB interfaces

CPC510 is equipped with the following USB-ports:
- 13x USB 1.1 ports (12 Mb/s), USB 2.0 (480 Mb/s) and 4x USB 3.0 ports (4.8 Gb/s).
- 2x USB2.0 ports are routed to the front panel connectors.
- 2x USB2.0 ports are routed to the mezzanine connector.
- 8(4)x USB2.0 ports are routed to the backplane connector *.
- 1x USB2.0 port is used for MicroSD interface.
- 4x USB3.0 ports are routed to the backplane connectors *.

** * when USB 3.0 is used, 4x USB 2.0 ports are utilized by USB 3.0 ports*

The ports support high-speed, full-speed, and low-speed modes. USB 2.0 in the high-speed mode enables to transfer data with the speed up to 480 Mb/s, which is 40 times faster than in the full-speed mode (USB 1.1).
Each port makes it possible to connect one USB peripheral devices. In order to connect more devices it is required to use an external hub.
USB power supply source is protected with an automatic fuse for 500 mA.

Fig. 2-3: USB1, USB2 connectors



Two standard USB 2.0 type A: USB1 and USB2 connectors are to be installed on the front panel

Table 2-4: Purpose of USB1 and USB2 connector contacts located on the front panel of CPC510

CONTACT NUMBER	CIRCUIT	FUNCTION
1	VCC	VCC signal
2	UV0-	Differential USB-
3	UV0+	Differential USB+
4	GND	GND signal

2.5.5 DisplayPort

DisplayPort connector on the front panel of CPC510 (see subparagraph 1.5.3) is designed for the connection of digital displays with the resolution up to 2560x1600@60 Hz. The output also enables to connect DVI-D monitors via adapter *.

** Prototype version does not support this function*

Fig. 2-4: DisplayPort connector

Table 2-4-1: Purpose of DisplayPort connector contacts

XS6 (DP)	
Contact	**Purpose**
1	LANE0+
2	GND
3	LANE0-
4	LANE1+
5	GND
6	LANE1-
7	LANE2+
8	GND
9	LANE2-
10	LANE3+
11	GND
12	LANE3-
13	AUX_EN#
14	CONFIG2
15	AUX+
16	GND
17	AUX-
18	HP_DETECT
19	GND
20	+3.3V

2.5.6 Serial interfaces (RS-232 и RS-485)

Serial interfaces (implemented via LPC interface) are available only where MIC584 mezzanine extension board is used (see Description of MIC584 given in the relevant User Manual).
MIC584 is equipped with 6 serial ports:
- COM1 (RS232) interface, 9-pin D-Sub connector on the front panel of MIC584;
- COM2-COM4 (RS232) interfaces, routed to 10-pins double-sided (IDC2-10) XP11-XP13 connectors of MIC584;
- COM5, COM6 (RS485) interfaces, routed to the 10-pins double-sided (IDC2-10) XP7 connector of MIC584.

The serial ports are fully compatible with 16C550 controller and include a full set of modem matching and control signals, support generation of maskable interrupts and transfer of data at the speeds up to 460,8 Kb/s.

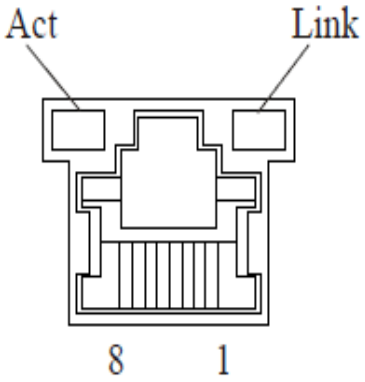
2.5.7 Parallel port interface

Standard parallel interface (IEEE1284, ECP/EPP/SPP) is implemented in MIC584 via LPC-interface and is available only via MIC584 mezzanine extension board MIC584 (see Description of MIC584 given in the relevant User Manual).

2.5.8 Gigabit Ethernet interface

The board has two ports 10Base-T/100Base-TX/1000Base-T Ethernet based on the high-speed server controller Intel® 82580. Controller's architecture is optimized for achieving a high performance at the minimum energy consumption. Controller is connected to the system via a high-performance PCI-E bus. Intel® 82580 architecture includes receive and transmit queues to limit the traffic on PCI-E bus, as well as PCI-E interface, maximizing the use of data packages for efficient bus load.
RJ45 Gigabit Ethernet connectors are located on the front panel of CPC510 and are marked with XS5.
Interfaces ensure an automatic detection of transfer speed and switching among data transfer modes 10Base-T, 100Base-TX and 1000Base-T.

Fig. 2-5: External view of RJ45 Ethernet connector



Front panel of CPC510 is equipped with 2 Gigabit Ethernet ports

2.5.8.1 Purpose of RJ45 connector contacts

RJ45 connectors enable to use 10Base-T, 100Base-TX and 1000Base-T interfaces from the front panel.

Table 2-5: Purpose of Gigabit Ethernet connector contacts

Contact	MDI / Standard Ethernet cable					
	10Base-T		100Base-TX		1000Base-T	
	I/O	Signal	I/O	Signal	I/O	Signal
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA–
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-	-	I/O	BI_DC+
5	-	-	-	-	I/O	BI_DC–
6	I	RX-	I	RX-	I/O	BI_DB–
7	-	-	-	-	I/O	BI_DD+
8	-	-	-	-	I/O	BI_DD–

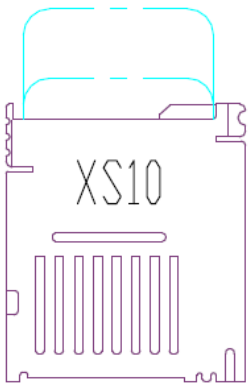
2.5.8.2 Status LEDs of Ethernet channel

The green "Line" LED is on if the line is connected.
The green "Act" LED is on if PC receives and transfers packages via RJ45 connector.

2.5.9 MicroSD connector

CPC510 is equipped with XS10 connector that supports MicroSDHC cards.
The MicroSD interface is transmitted to the internal USB 2.0 port. MicroSDHC has a storage capacity up to 64 GB. Below you can see an external view of MicroSD connector with the installed memory card.

Fig. 2-6: External view of MicroSD connector



MicroSD connector with the installed memory card

2.5.10 SATA interface

- **SATA interface:**
- RAID 0, 1, 5, 10 support

- **SATA II interface**
- One interface is permanently routed to the mezzanine connector:
- One interface can be switched between backplane connector and mezzanine connector;
- Two ports are routed to the backplane connector.

- **SATA III interface:**
- Two interfaces are routed to the backplane connector.

It should be noted that Fastwel Group manufactures MIC584 in two versions: MIC584-01 and MIC584-02, and both of them are compatible with CPC510. Version MIC584-01 is equipped with SATA connectors. If a user installs MIC584-02 mezzanine board on CPC510, then CPC510 together with MIC584-02 will be operating properly, except for the two SATA channels which will not be implemented.
Detailed description of MIC584 is given in the User Manual.

2.5.11 HD (high definition) audio:

Audio interface is implemented on MIC584 mezzanine board:
- Linear I/O;
- Headphones output;
- Microphone output.

More detailed information is described in the relevant User Manual.

2.6. LEDs

The front panel of CPC510 is equipped with LEDs described in the table below:

Table 2-6: Designation and functions of LEDs of CPC510

№	Mnemonic	Description
1	SYS	Two colors, read and blue. Blue – “Power Off” mode. Red –
2	STG	Hardware malfunction
3	GP	Two colors, red and green. Red – programmable. Green – programmable. During the start, green LED demonstrates the state of the start-up process
4	PE	Two colors, red and green. Red – communication error over PCI Express interface. Green Led steady – connection over PCI Express interface. Green flashing – connection over PCI Express is limited.
5	OVH	Two colors, red and green. Red – CPU overheating, memory and PCH. Orange, flashing – CPU overheating, memory and PCH before critical point (borderline state).

Support of the signaling system according to the SFF-8485 specification.

2.6.1 GP LED configuration and control registers (logical device 5)

Table 2-7: GP LED configuration and control registers P

INDEX	Address of I/O port	Type	HARD RESET	Configuration register
30h	-	R/W	00h	Activate. Bit[0] in “1” – module’s LED is active
-	Base+0	R/W	01h	LED data register [3:0]. The rest bits are not important, and are read as 0.
60h	-	R/W	-	Base[15:8] - I/O port base address bits[15:8]
61h	-	R/W	-	Base[7:0] - I/O port base address bits[7:0]

For operation with GP indicator you’ll need to set a base device address and activate it (LDN=5) similarly to the watchdog timer or FRAM-module. Control of GP indicator operation is carried out via the LED register. LED is modified in the I/O field regarding the set base address.

2.6.2 LED register initialization

Sequence of operations at the time of device initialization:
- Enter the configuration mode

```
MOV DX, 302H
MOV AL, 46H
OUT DX, AL
MOV AL, 57H
OUT DX, AL
```

- Write an LDN of the register to the register (LED register has a logical number 5)

```
MOV DX, 302H
MOV AL, 7
OUT DX, AL
MOV DX, 303H
MOV AL, 5
OUT DX, AL
```

- Set the base device number in the I/O field (e.g. 31dh):

```
MOV DX, 302H
MOV AL, 60H
OUT DX, AL
MOV DX, 303H
MOV AL, 3H
OUT DX, AL
MOV DX, 302H
MOV AL, 61H
OUT DX, AL
MOV DX, 303H
MOV AL, 1dH
OUT DX, AL
```

- Activate the device:

```
MOV DX, 302H
MOV AL, 30H
OUT DX, AL
MOV DX, 303H
MOV AL, 1H
OUT DX, AL
```

- Exit the configuration mode:

```
MOV DX, 302H
MOV AL, 57H
OUT DX, AL
MOV AL, 46H
OUT DX, AL
```

2.6.2.1 Designation of separate bits of the LED register

Designation of separate bits of the LED control register is shown in the table below:

Table 2-8: Designation of LED register control bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Redundant bits. Read as "0".				GP red LED Bit1	GP red LED Bit0	GP green LED Bit1	GP green LED Bit0

GP is a two-color LED indicator has two independent read and green light emitting diodes. Therefore, green, red or orange LEDs are available (red and green are switched on simultaneously), depending on the combination of activated diodes. Thus, an independent programmed control of each LED via the LED register is supported. State of each LED is described by two bits. The following combinations are supported:

Table 2-9: Combinations of GP indicator's control bits

Bit 1	Bit 0	State
0	0	LED is OFF
0	1	LED is flashing with a frequency of 8 Hz
1	0	LED is flashing with a frequency of 1 Hz
1	1	LED is constantly ON

3. Application of CPC510

CPC510 board is designed for operation as part of the Compact PCI Serial, Legacy Compact PCI and hybrid – Plus I/O systems. The board corresponds to CPCI-S.0 R1.0 [1] and Compact PCI Plus IO R1.0 [2] specifications.
The board is manufactured as two versions: CPC510-01 and CPC510-02.
CPC510-02 is different because it is equipped with MIC590. Therefore, CPC510-02 version is an assembly of two boards with a minimum width of 8HP. MIC590 interfaces make it possible to use CPC510-02 in the Compact PCI Plus IO systems or in the systems with Legacy+Serial combination.
Below there are examples of various systems based on CPC510.

3.1 Compact PCI Serial system

3.1.1 Board-to-board connections

Compact PCI Serial system is a major area of CPC510 board application, since it enables to implement all the advantages of Intel Core both in terms of the processing power and high-speed board-to-board connections.
According to [1] specification for the standard 9-slot backplane, the system slot can support the following functionalities of board-to-board connections:
• Up to 2 PCI Express interfaces x8 (Fat Pipe)
• Up to 6 PCI Express interfaces x4
• Up to 8 USB 2.0/3.0 interfaces
• Up to 8 SATA interfaces
• Up to 8 Gigabit Ethernet interfaces
In which case, each Gigabit Ethernet interface can have a Star or Full Mesh interconnection types.
Out of the above interfaces, CPC510 supports:
• 2x PCI Express interfaces x8 Gen 2 (Fat Pipe)
• 4x PCI Express interfaces x4 Gen 2
• 8x USB 2.0 interfaces
• 4x USB 3.0 interfaces
• 5x SATA interfaces
A number of the supported interfaces makes it possible to create high-efficient and compact scalable systems. Apart from that, lack of board-to-board and device-to-device connections enables to increase reliability and repair capability.
Standard Compact PCI Serial system includes one CPU-module (host), installed into red system slot (System) and a set of peripheral units installed into peripheral slots (Perip.). The implemented connection pattern is Star. Gigabit Ethernet interface will not be considered since it is not supported by CPC510.

It should be noted that there are less than 8 PCI Express, SATA and USB 3.0 interfaces available for CPC510. Therefore, PCI Express interface is supported in peripheral slots from 1 to 6, SATA interface is supported in slots from 8 to 4, and USB 3.0 interfaces – in slots from 1 to 4 (see Fig. 3-1). SATA interface of the slot #4 can be soft switched (via the menu of system BIOS) –switched for being used on MIC584. In which case, SATA interface will be supported in the 8 to 5 slots. When CPC510-02 is used, MIC590 occupies a free space (guide rails should be installed) to the left of the system slot, without connecting to the backplane.

*Fig. 3-1: Numbering of CPC510 interfaces in the Compact PCI Serial backplan***e**

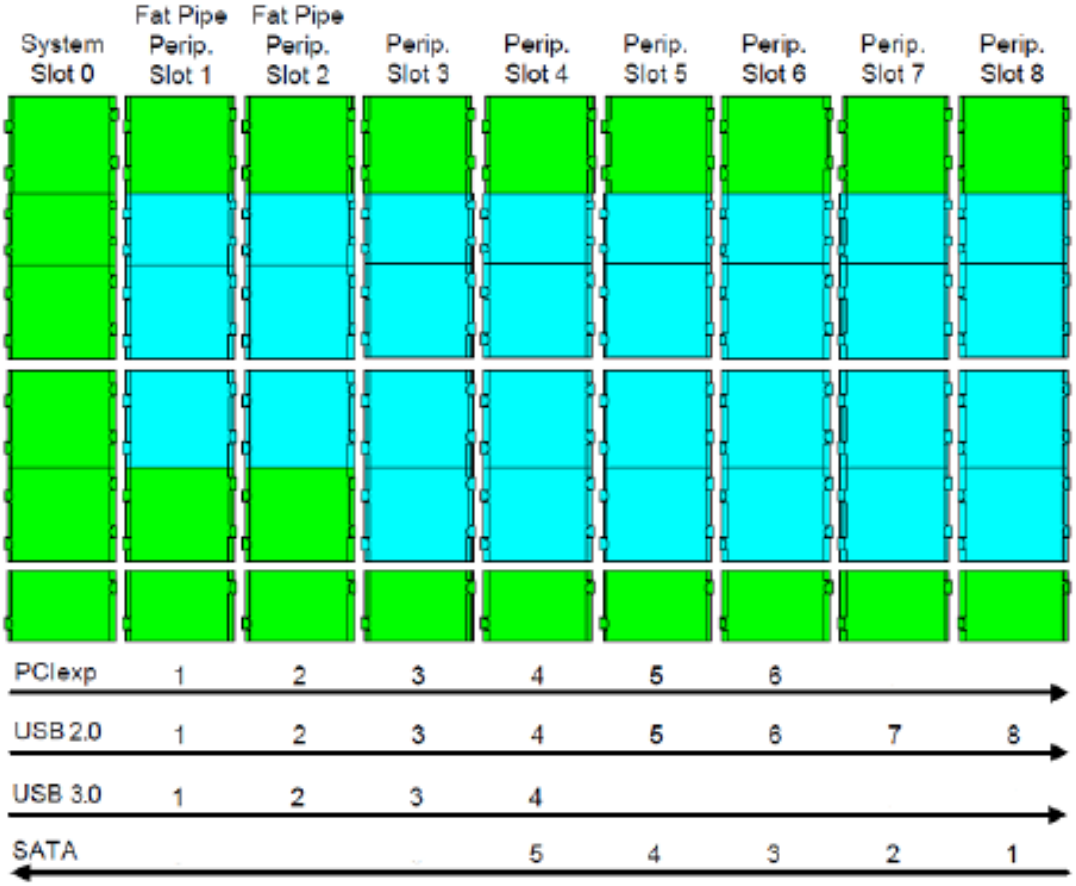
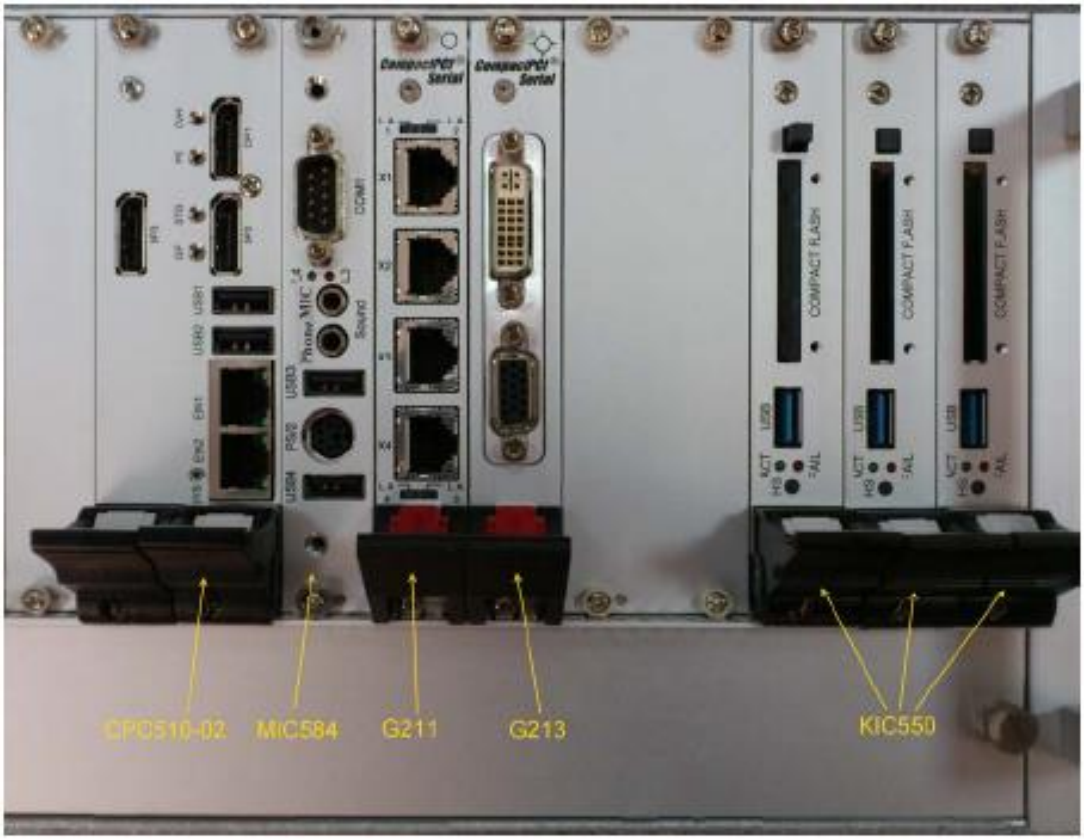


Fig. 3-2 has a picture of implemented standard configuration of Compact
PCI Serial system is shown. The system shown on Fig. 3-2 contains the following components:
• 24579-420 Schroff 4 U, 9 slot, with rear I/O and ATX PSU, shielded 19" chassis, 300 W;
• 3U CompactPCI CPU board CPC510-02;
• MIC584-01 mezzanine I/O board;
• G211 - 3U CompactPCI® Serial Quad Gigabit Ethernet Interface, MenMicro;
• G213 - 3U CompactPCI® Serial XMC/PMC Carrier with the installed XMC G460 - Dual Display Graphics XMC Module with AMD/ATI E4690 GPU, AdLink;
• 3x 3U modules, KIC550-01 CPCI Serial PCIE/SATA carrier of storage devices.

The power supply unit installed in the sub-rack supports the control function, but the control signals and standby supply output are not connected. In order to implement the control function, it is necessary to connect the required signals to the “Utility” (see www.schroff.biz).

Fig. 3-2: Example of standard implementation of Compact PCI Serial system

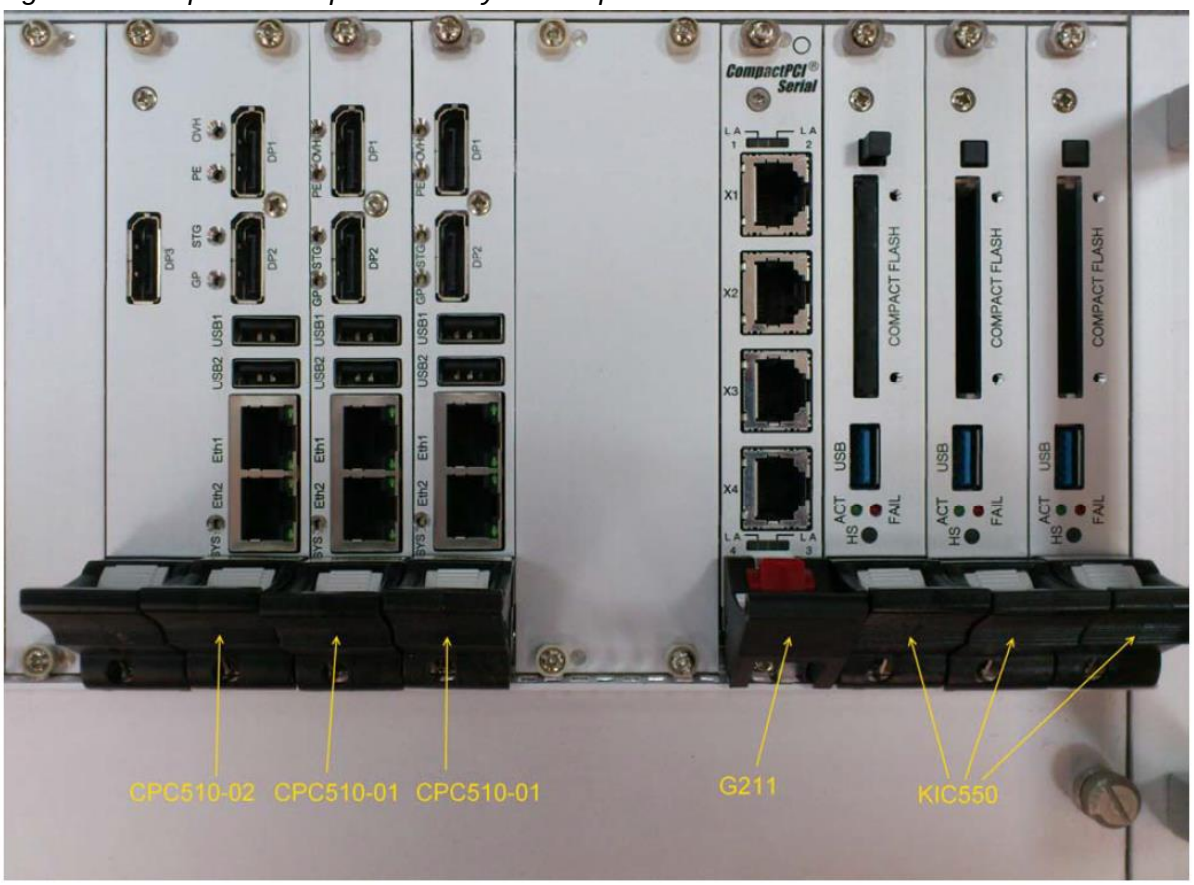


In addition to operation both as a system host module, CPC510 supports operation in peripheral slot as an endpoint. The PLX switches installed onboard of the PCI Express PLX -module enable to implement nontransparent mode (NT-mode) for one of the downstream ports (see Table 5-1). This enables to isolate CPU boards among the boards using PCI Express-connections. Such a connection makes it possible to build multiprocessor cluster systems. In general, using a standard 9-slot backplane CPC510 CPU Board in a system slot enables to arrange operation of two CPC510-01 boards with a connection via PCI Express x8 Gen2 bus (40 Gb/s) and four CPC510-01 boards with a connection via PCI Express x4 Gen2 bus (20 Gb/s). The rest two peripheral slots can be used for the storage system (e.g., KIC550).
Software booting on peripheral CPU boards may be carried out both from the integrated MicroSD memory card, and via RIO backplane connector when there is a relevant rear I/O board. An example of multiprocessor system implementation is shown on Fig.3. Components used in the system:

• 24579-420 Schroff 4 U, 9 slot, with rear I/O and ATX PSU, shielded 19" chassis, 300 W;

• 3U, CPCI Serial CPC510-02 CPU Board, Fastwel;
• MIC584-01 mezzanine I/O Board, Fastwel;
• 2x 3U, CPCI Serial CPC510-01 CPU Boards, Fastwel;
• G211 - 3U CompactPCI® Serial Quad Gigabit Ethernet Interface, MenMicro;
• 3 x 3U Boards, CPCI Serial PCIE/SATA storage device carrier KIC550-01, Fastwel.

Fig. 3-3: Example of multiprocessor system implementation



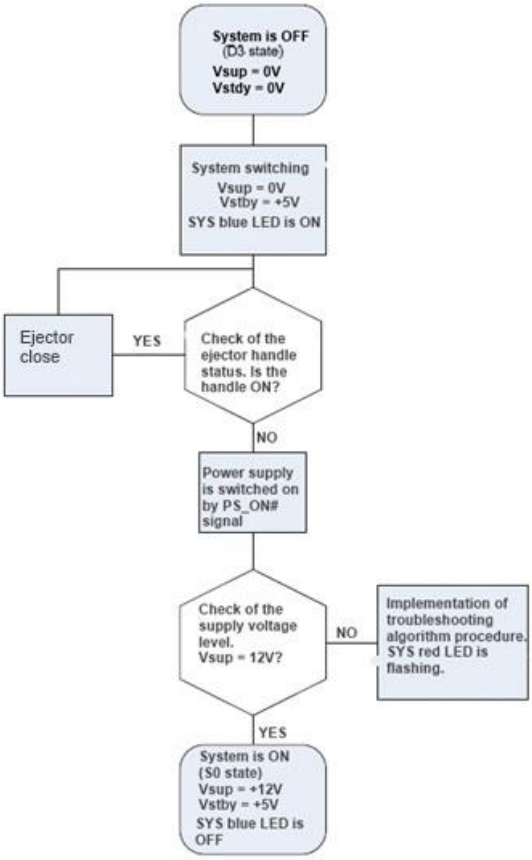
3.1.2 Interaction with power supply unit

CPC510 has a universal power supply circuit that enables operation with the power supply unit in two modes: with control support of the power supply unit (similarly to the control used in ATX PSU) and without control support. While operating CPC510, each of the specified modes can be used in the system slot of Compact PCI Serial mezzanine board.
Control of the power supply unit is supported in CPC510 only when it is installed in the system slot of the Compact PCI Serial backplane. In which case the PSU should support the control function and should be equipped with:
• Integrated source of standby supply voltage +5V_stby with a minimum load current – from 1 A.
• “Switch on” input (PS_ON#).

Logic of the PSU control is determined by FPGA microcode of CPC510. The control can be carried out by any of the following methods: button

The Power Button located on the control panel of 19” chassis, programmable by the ejector handle button (see section BIOS Description) or ACPI program module of the used OS.
The Power Button is connected to the Utility, which is located on the Compact PCI Serial backplane. This connector is also used for the PSU control input (PS_ON#), as well as external Reset button.

Fig. 3-4: Algorithm of the initial system start-up from “Physical switching-off” position (D3)



The initial start-up algorithm from a fully release condition (D3) (see. Fig. 3-4) of the system is similar for all the types of CPC510 application. If the PSU does not support control and therefore has no +5 V_stby, power source, the specified voltage is generated in a standard way directly on CPC510. The diagnostics procedure mentioned in the algorithm is designed for detecting non-operating PSUs both external and integrated into CPC510 board. The diagnostics results are indicated in accordance with the number of SYS red LED

flashes. After diagnostics, the main power supply from CPU board is switched off and only LED indication system will operate.

Final system switching off (both CPU board and peripheral modules) is possible only for power supply units supporting control of the relevant setting in BIOS menu (only CPC510 board can be switched off, if necessary). If PSU doesn't support the control function, only CPU board will be switched off (S5 mode). The switching-off procedure can be activated by the ejector handle button, if the relevant settings have been made in BIOS menu, programmable switching-off is via ACPI OC (see Fig. 3-5) or Power Button (see Fig. 3-6).

Fig. 3-5: Algorithm of system soft off.

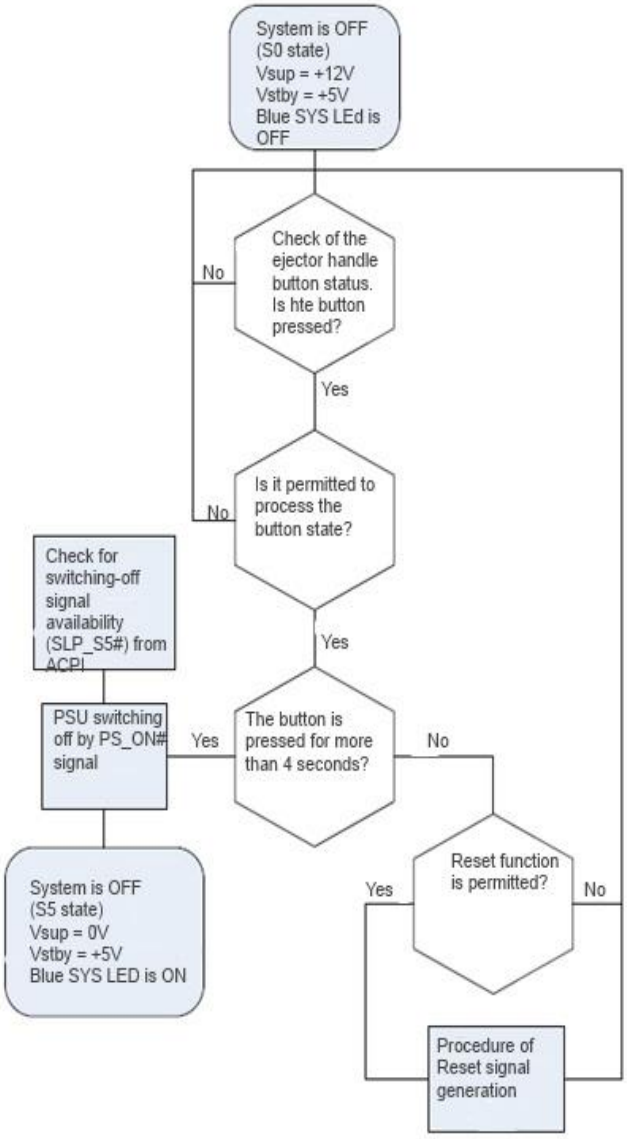
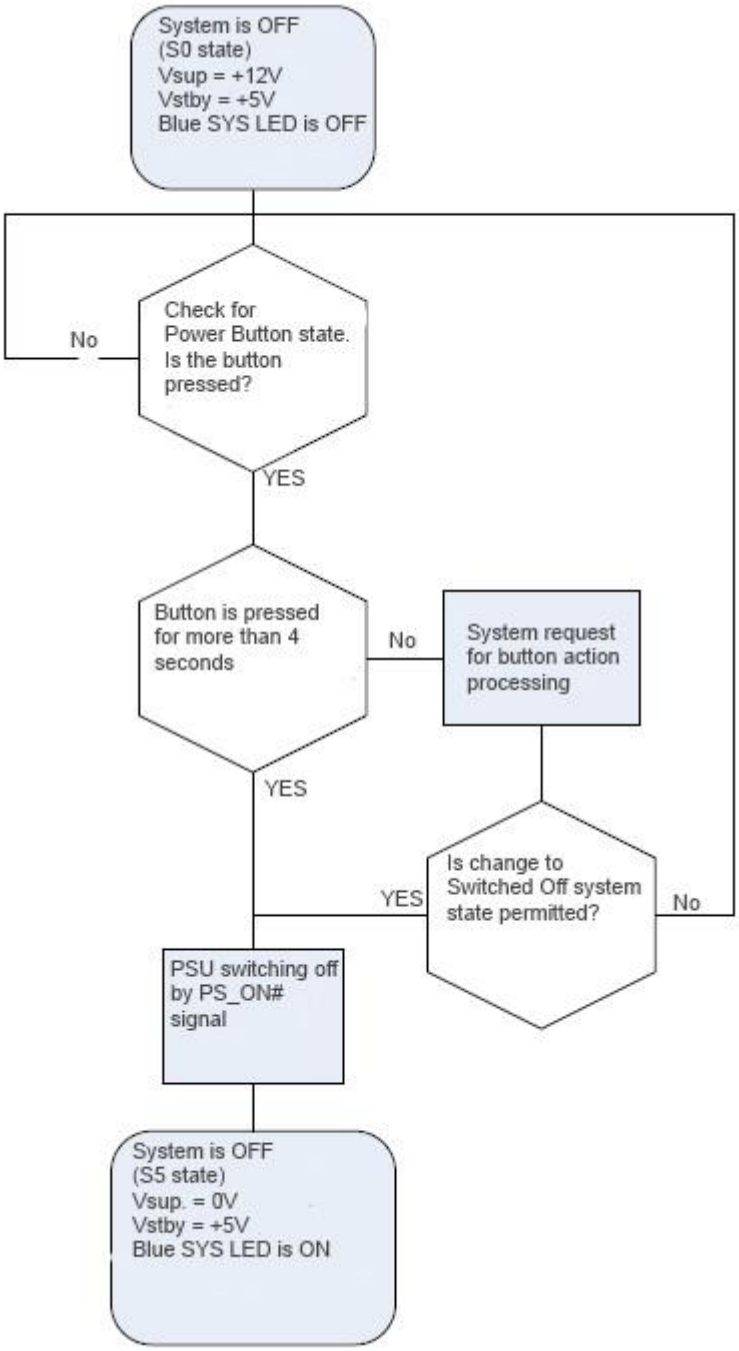
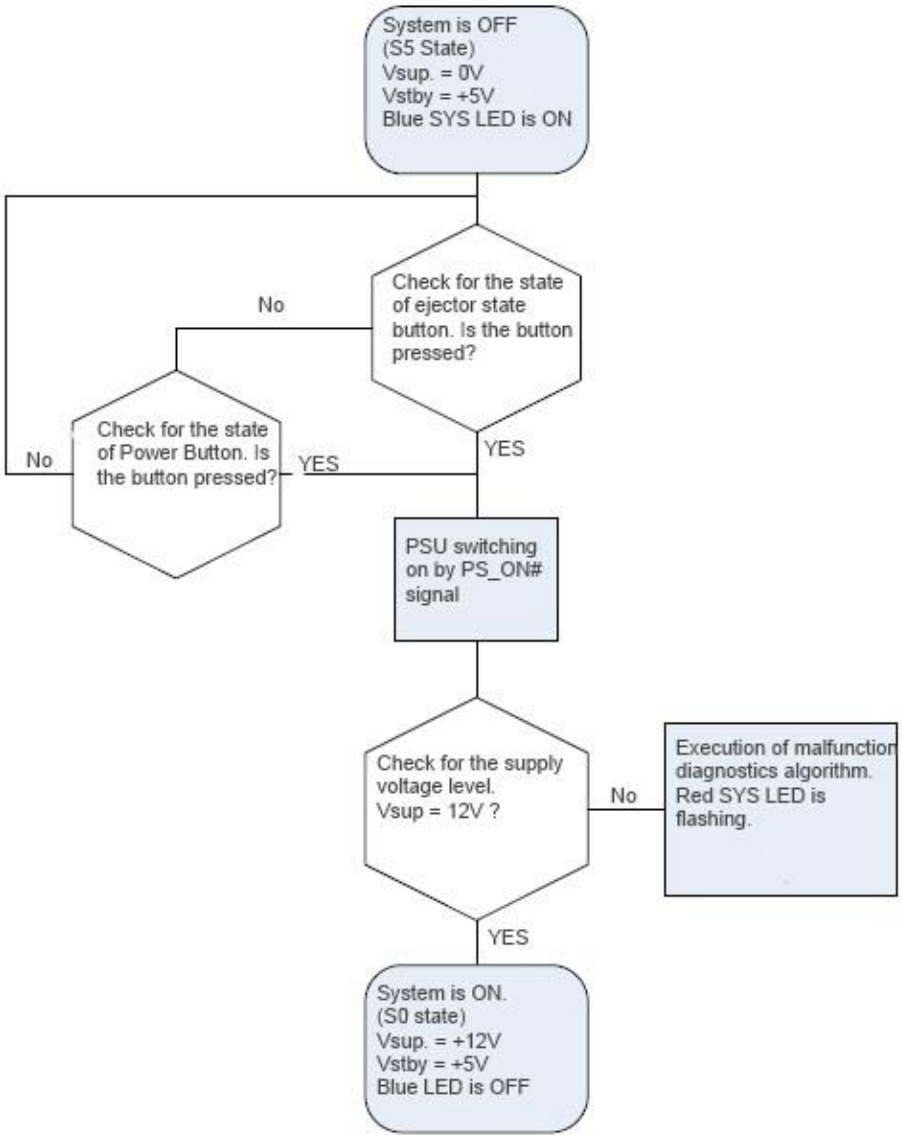


Fig. 3-6: System switching-off algorithm by Power Button



After algorithm execution, system (or CPC510 CPU board only) changes its state to Soft OFF or S5). From the state, there are two states available: - complete shutdown “Manual switching off” state (D3) or, on the other hand, complete OFF position (S0).
Change to the S0 position is carried out by pressing the ejector handle button or Power Button (see Fig. 3-7).

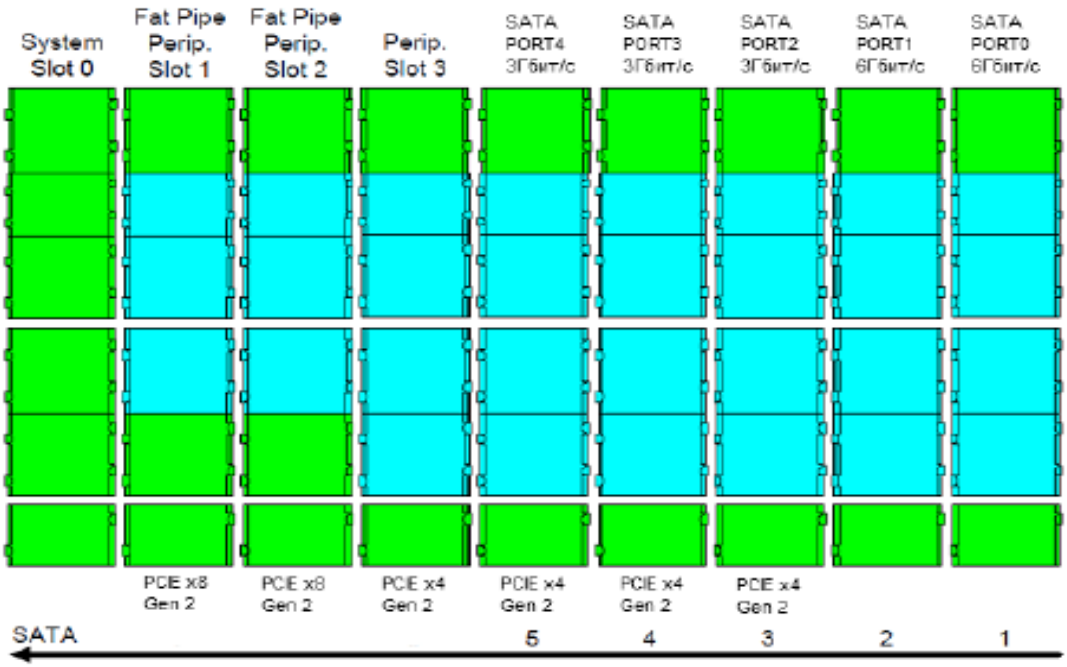
Fig. 3-7: Algorithm of system switching-on from Soft ON (S5) state.



3.1.3 Peculiarities of information storage system

According to the [1] specification, CPC510 supports operation of information storage devices installed into the backplane extension slots (see Fig.1).
The storage devices are numbered from the rightmost slot (see Fig 3-8).
As it has been already mentioned, CPC510 board can simultaneously support up to six SATA storage devices (from 0 to 5). In which case, SATA port #5 is permanently rooted for the use on MIC584, and SATA-port #4 can be switched between slot #4 of the mezzanine board and SATA-interface of MIC584. SATA port #4 can be switched to MIC584 automatically using CPC510 board in the peripheral slot or software-based from the BIOS menu (By default, port #4 is connected to the mezzanine board) during installation of CPC510 in the system slot. Other SATA ports ## 0-3 are routed to the Compact PCI Serial mezzanine board. The rest of the mezzanine board slots do not support operation with SATA storage devices.
In terms of speed performance, there are ports supporting transfer speeds up to 6 Gb/s (SATA ports ## 0 and 1) and ports supporting transfer speeds up to 3 Gb/s (SATA ports ## 2-5).

Fig. 3-8: Backplane SATA-interfaces supported by CPC510

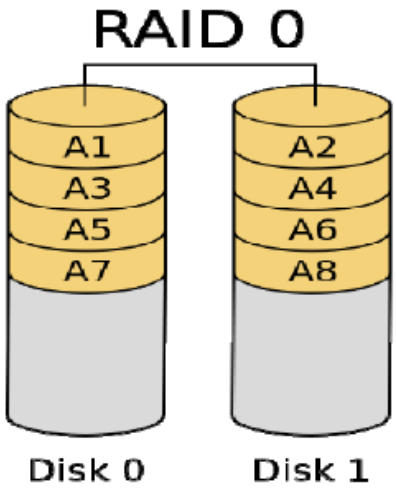


Intel® BD82QM77 PCHs installed on board of CPC510 makes it possible to work with both stand-alone storage devices and generate the so called RAIDs. Operation mode can be set via BIOS menu: “Advanced”-“SATA Configuration”- “SATA Mode Selection”. The following versions are available:

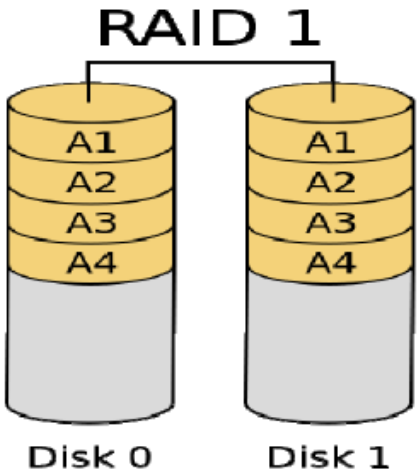
• AHCI – connection of storage devices via Serial ATA protocol;
• IDE – connection of storage devices via ATA-compatible protocol;
• RAID – connection of the storage devices via Serial ATA protocol with a possibility to arrange the storage devices into an array.

In AHCI mode (by default) all the storage devices connected to ## 1-6 ports are available. All functions of the Serial ATA protocol are supported: NCQ, Link Power state etc.
The transfer speed corresponds to the declared one.
IDE mode is meant for using in old versions of OS (Legacy) that do not support Serial ATA protocol. This mode supports only the storage devices, connected to SATA ports ## 1-4. Therefore, presence of two IDE controllers with four storage devices is simulated. In which case the operation speed of SATA storage devices is independent of the simulated UDMA-mode and can reach up to 3 Gb/s.
Hardware of BD82QM77 controller (Rapid Storage Technology) enables to build a data storage array using the storage devices connected to SATA ports.
RAID building available options:
• RAID 0 (Striping). This version makes it possible to write/read simultaneously to all RAID discs (support up to 6 storage devices), therefore, increasing the storage system performance by several times. In which case the total array capacity will be equal to the double volume of array disc with

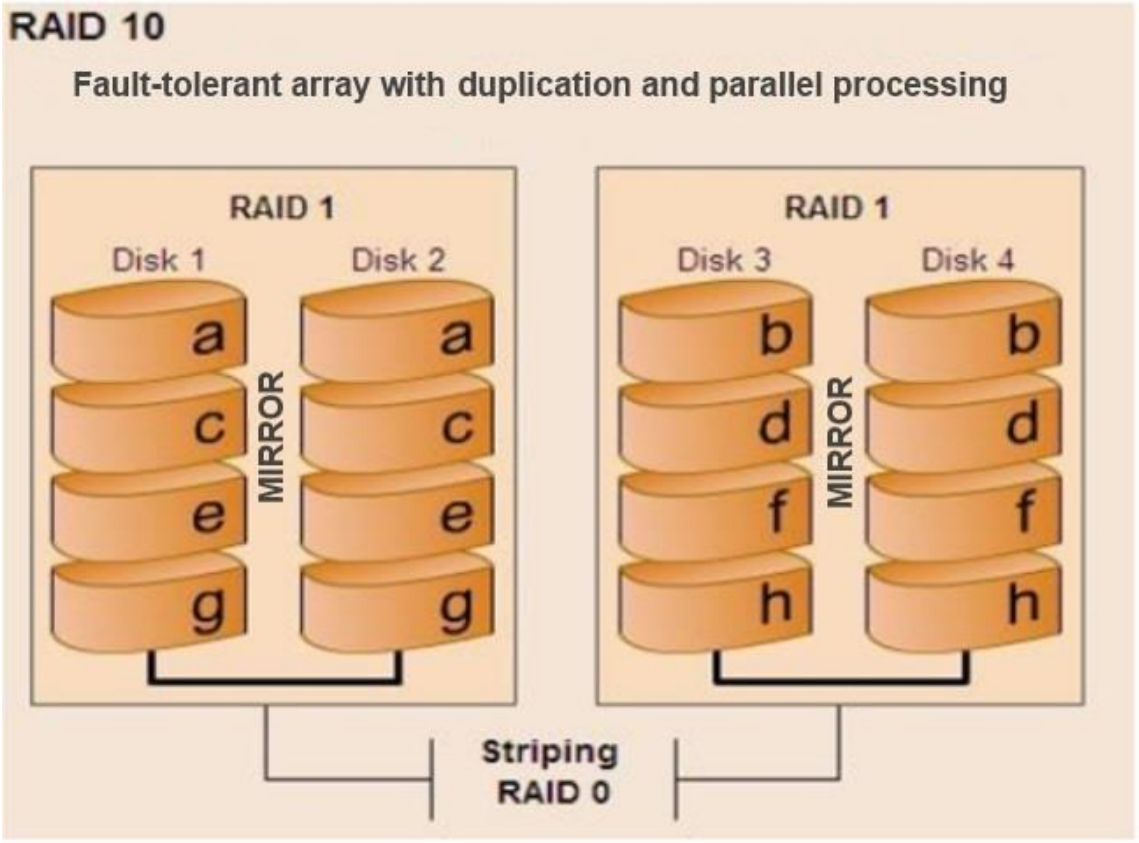
the minimum capacity. In which case fault tolerance remains at a low level.



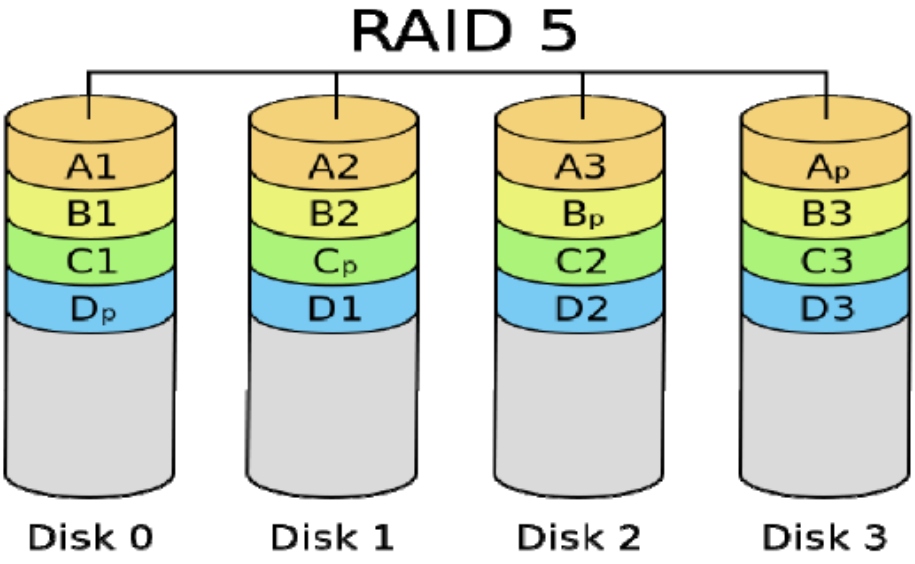
• RAID 1 (Mirroring). This RAID type enables to improve data storage reliability via mirror writing of data to the second array disc. Performance of the information storage system in this case is lower and general RAID volume is equal to the one of RAID disc which has minimum capacity.



- RAID 10 - is a nested RAID system, combination of RAID 1 and RAID 0. The combination is known as a “stripe of mirrors”, which provides serial data writing to several discs, as in RAID 0. This architecture represents an array similar to RAID 0, where the segments are not separate discs, but RAID 1 arrays. RAID 10 requires a minimum of four SATA- drives.



• RAID 5. This type provides a high-efficient storage retaining fail-safety for 3 or more discs. Data blocks and check sums are cyclic written to all the RAID discs. Capacity of RAID5 is calculated using the formula: (n-1)*hddsize, where n — number of discs in RAID and hddsize — size of the disc with minimum capacity. Operation of recording information to RAID 5 volume requires additional resources and the efficiency falls since additional calculations and write operations, but during the reading process (as compared to a separate storage device) there is time gain, since data flows from several array discs can be processed in parallel. RAID 5 is good for applications that require large volume of data storage retaining fail-safety.



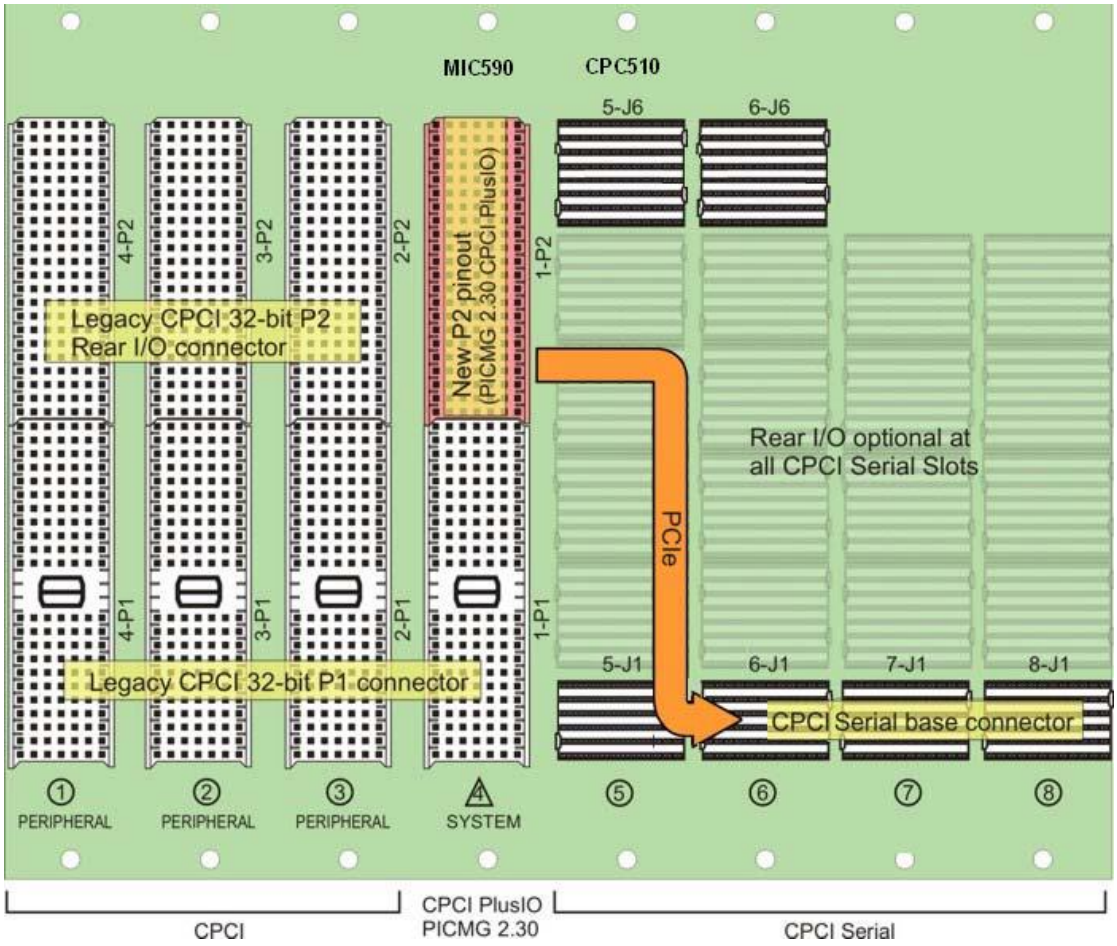
** More detailed information on operation of RAID based on Intel chipsets can be found in the document Intel Rapid Storage Technology. User Guide. Rev.1.0*

KIC550-01 or its equivalent can be used as a board-carrier for SATA storage device.
If it is used as the storage system of KIC550, for transferring data it is possible to simultaneously use both SATA and PCI Express interfaces. In which case one of the storage devices installed on KIC550 is available by using SATA and the other one – by PCI Express interface via PCI Express-SATA bridge installed on KIC550. It is possible to increase a total number of the storage devices by reconfiguring of KIC550 for operation only with PCI Express interface. In which case, both storage devices on KIC550 become available via PCI Express interface. Then the storage devices on KIC550 boards in peripheral slots 8 and 7 will have only SATA interface, in slots from 6 to 4 – hybrid PCI Express+SATA interfaces, and in slots 3 to1 – only PCI Express interface. The backplane slots in which PCI Express interfaces are available, supported by CPC510, are shown on Fig. 3-8.
More detailed information on operation with KIC550 is available on www.fastwel.com.

3.2 Compact PCI Plus I/O system

Using CPC510 in hybrid system makes it possible in additional peripheral Compact PCI Serial modules, to use 32-bit Compact PCI modules.
For operation with PICMG 2.30 backplane only CPC510-02 version can be used – assembly of CPC510 and MIC590.
The system, based on CPC510-02 CPU board and PICMG 2.30 backplane combines a high-performance computing device with Intel Core technology with a wide range of peripheral modules. The use of a common backplane makes the system highly compact and reduces a set of the components used. Apart from that, the CPC510-02 makes it possible to perform a gradual transition from the standard Legacy or PICMG 2.30 systems to the new Compact PCI standard with minimum material expenses.
CPC510-02 board is installed in two slots: The board itself is installed in the backplane slot #5, while MIC590 is installed in the system slot #4 (red) of PICMG 2.30, respectively.

Fig. 3-9: Installation of CPC510-02 into two slots



Attention!

Installation of Compact PCI Serial connectors of CPC510 board always should be carried out into the relevant Compact PCI Serial backplane connectors. Otherwise the connectors could be deactivated due to mechanical damages.

Below is the list of interfaces available in the PICMG 2.30 system with CPC510-02 CPU Board:
• Up to 3 devices on 32-bit Compact PCI bus, 33 MHz or 66 MHz, supporting 3.3 V or 5V VIO (slots 1 to 3).
• Up to 3 devices on PCI Express bus x1 Gen 2 (slots 6 to 8).

Fig. 3-10: Example of system generation on the basis of PICMG 2.30 backplane (Plus I/O) and CPC510-02 CPU board

Fig. 3-10 shows an example of the implementation of PICMG 2.30 system PICMG 2.30 with CPC510-02 CPU board.
Components used in the system (left to right):
• Shielded 19” chassis 24579-405, 4 U, 8 slots with rear I/O connectors and power supply unit of 300W, Schroff;
• cPCI-3544-001 4-Port RS-422/485 Isolated Serial Communications Card, AdLink;
• CP346 4-Port RS-232, RS-422/485 Serial Communications Card, Kontron;
• cPCI-7841 NulPC (Dual CAN interface Module), AdLink;
• 3U, CPCI Serial CPC510-02 CPU board, Fastwel;
• MIC584-01 mezzanine I/O board, Fastwel;
• G211 - 3U CompactPCI® Serial Quad Gigabit Ethernet Interface, MenMicro;
• KIC550-01 3U CPCI Serial PCIE/SATA carried for storage devices, Fastwel.

3.2.1 Power supply unit

PICMG 2.30 standard does not support the function of power supply unit control. Therefore, CPC510-02 operates with PSU without the control support (see subsection 3.1.2).

3.2.2 Peculiarities of data storage system implementation

As opposed to Compact PCI Serial version, when PICMG 2.30 backplane is used, SATA-interfaces of CPC510-02 remain unavailable. In which case, in order to store information, the following options are suggested:
• MicroSD storage device installed in CPC510-02;
• SATA-interfaces used, routed via MIC584;
• Use KIC550 in PCI Express mode (see Fig. 3-10).

3.2.3 Using CPC510-01 as additional computing device

If necessary, CPC510-01 can be part of PICMG 2.30 system as additional computing device, installed into the peripheral Compact PCI Serial connector of PICMG 2.30 backplane. In which case, depending on the specific type of backplane, according to specification [2], the width of PCI Express channel can be varied from x1 to x4.

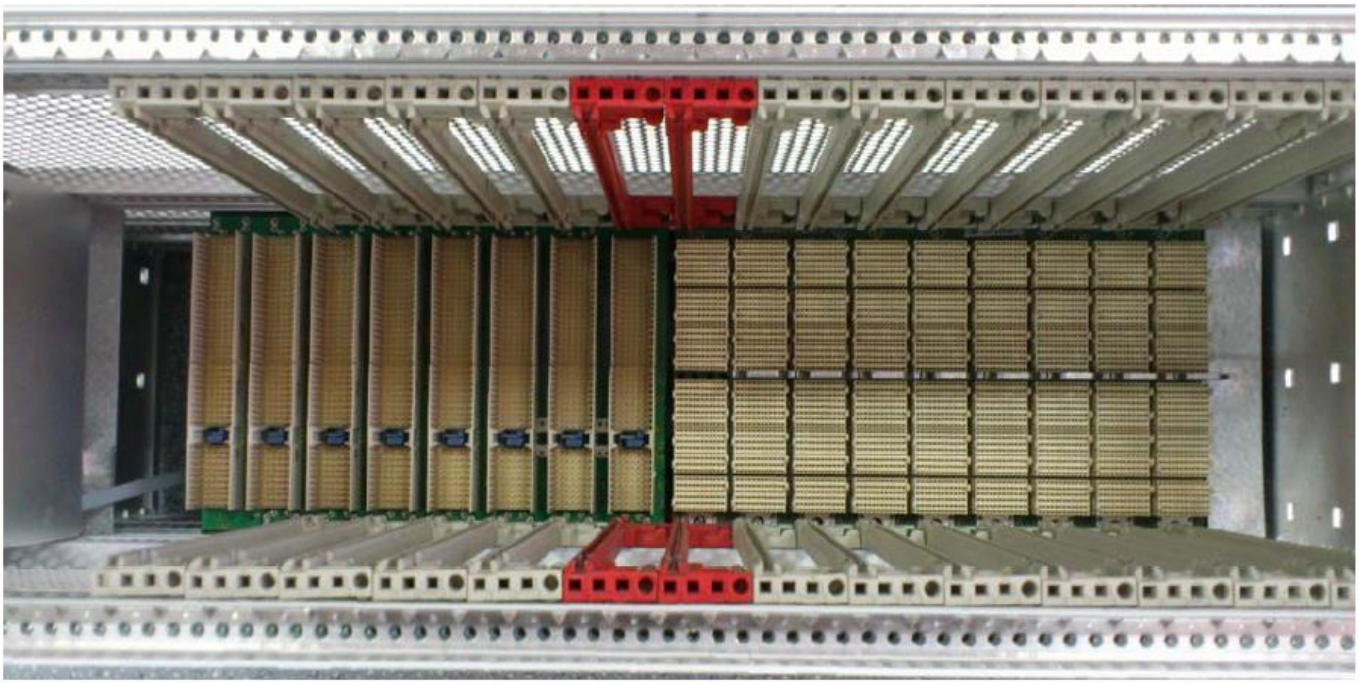
Fig. 3-11: Example of PICMG 2.30 system generation with the main CPC506-03 CPU board and additional on-board CPC510-01 computing device

Fig. 3-11 shows an example of such a system.
Components used in the system (left to right):
• 24579-405, shielded 4U 19" chassis, 8 slots with rear I/O connectors and 300 W power supply unit, Schroff;
• cPCI-3544-001 4-Port RS-422/485 Isolated Serial Communications Card, AdLink;
• CP-341 Dual Ethernet Module, Kontron;
• 3U CPCI Plus I/O CPC506-03 CPU board, Fastwel;
• 3U CPCI Serial CPC510-01 CPU board, Fastwel;
• MIC584-01 mezzanine I/O board, Fastwel;
• 2 x3U boards CPCI Serial PCIE/SATA storage device carrier KIC550-01, Fastwel.

3.3. Extended hybrid Compact PCI Serial system

An extended Compact PCI Serial system is a combination of a full-size 9-slot Compact PCI Serial backplane and 8-slot 32-bit Compact PCI backplane. Unlike PICMG 2.30, the extended system enables Legacy Compact PCI interface retaining advantages of Compact PCI Serial system. The number of slots in each of the backplanes can be reduced depending on the specific requirements to the system. All the components participating in the extended hybrid system are standard ones which makes the system less expensive and system tasks less time-consuming.

Fig. 3-12: Example of the assembled backplanes in the extended hybrid system



In the example shown on Fig.3-12 the following components are used:
• 3U CPCI 32-bit 8-slot backplane, system slot on the right, 23006-300, Schroff;
• 3U CPCI Serial 9-slot backplane, 23007-614, Schroff;
• 24563-473 shielded 3U 19" chassis;
CPC510-02 can be installed into red slots of the backplanes CPC510-02 board can be installed. In which case, the left red slot is used for MIC590, and the right red slot – for CPC510.
Since a standard Compact PCI Serial backplane is used, all functions of board-to-board connections, power control and storage devices for Compact PCI Serial version (see p.1) are supported.
Up to 8 Compact PCI 32-bit devices can be supported.
As compared to PICMG 2.30 system, Compact PCI 32-bit backplane makes it possible to route LVDS interface from MIC590 to the rear I/O board. Switching is performed automatically while the RIO board is installed, corresponding to the relevant slot to the left.

3.4 Additional features of CPC510

CPC510 structure enables to create a wide range of devices with various functionalities. Availability of board-to-board connectors with PCI Express x4, SATA, LPC interfaces makes it possible to design highly reliable and efficient compact systems by designing optional mezzanine boards.

4. Installation

CPC510 can be easily installed. However it is necessary to strictly follow the below rules, warnings and procedures in order to properly install the board, avoid damages to the device, system components as well as personnel injuries.

4.1 Safety requirements

When handling CPC510 you should strictly follow the safety requirements below. Fastwel Group is not responsible for any damages, caused as the result of failure to comply with these requirements.

Caution!
Be careful when handling the board, since the het sink could be too hot. Do not touch the heat sink during the board removal.
In addition to it, do not put the board on any surface or in any packaging until the board and heat sink reach ambient temperature.

Attention!
Switch off the power of CompactPCI system before installing the board into a free slot. Violation of this rule could pose danger to your life and health, as well as lead to system and board damages.

Electrostatic Sensitive Device (ESD)!
CompactPCI board contains elements sensitive to electrostatic charges. In order to avoid board damages, the following safety precautions should be observed:

- Before touching the board, remove static charge from the clothes as well from the tools before using them.
- Do not touch electronic components and connector contacts.
- If your professional workplace has antistatic protection, don’t neglect to use it.

4.2 Installation procedure of CPC510

In order to install CPC510 to the system, follow the below procedure:
1. Make sure that the safety requirements specified in the previous chapter are met.

Attention!
Non-compliance with the following instruction could lead to the board damages and improper operation of the system.

2. Before installation, make sure that the board has configuration, corresponding to application requirements. Information on installation of peripheral and I/O devices is given in the relevant sections of Chapter 4. Information related to the CPU board installation of MIC584 can be found in the User Manual of MIC584.

3. If CPC510 operates with mezzanine board, before installing CPC510 into the system, connect mezzanine board to the relevant connector of CPC510, see subsections 2.5.2 Connector for mezzanine board and 4.5 Installation of MIC584 mezzanine board.

Attention!
The following operations should be performed with care, in order to prevent damaging both CPC510 and other system devices.

4. For CPC510 installation, please do the following:
- Before starting the installation process, makes sure that system power supply is off.

Attention!
While performing the following operation, **do not apply too much force** putting the board connector into the backplane connector.
Use the front panel handle to install the board into the connector.

- Carefully insert the board into the required slot, moving it along the guide rails until it touches the backplane connector.
- Using the front panel handle, push the board into the backplane connector. The board is inserted to the end, when the handle makes the relevant sound. If CPC510-02 board is used, it is necessary that both handles make this sound (see Fig. 1-10: Front panel of CPC510-02).
- Fasten the board by two fixing screws on the front panel of CPC510-01 (see Fig. 1-9: Front panel of CPC510-01). If CPC510-02 board is installed, it is required to fasten it with four fixing screws (see Fig. 1-10).
- Connect all required external interface cables to the board.
- Make sure that both CPC510 and all the connected cables are fixed securely.

CPC510 is ready for work.

4.3 Board removal procedure

In order to remove the board, you should perform the following:

1. Make sure that all the safety requirements of section 4.1. are met. Special consideration should be given to the warning of the heat sink temperature.

Attention!
The following operations should be performed with care to prevent damages to neither CPC510, nor other system devices.

2. Before starting the removal of CPC510, make sure that the system power supply is off.

3. Disconnect all interface cables from the board.

4. Remove the front panel fixing screws.

Attention!
Board handling requires additional care, since cooling heat sink could be heated. Do not touch the heat sink during the board replacement.

5. Unlock the front panel handle by pressing A button and moving it down, remove the board from the backplane connector (see Fig. 1-9 Front panel of CPC510-01). If CPC510-02 is used, it is required to simultaneously press A and B buttons and move the both handles down (see Fig. 1-10).

6. After the board is removed from the backplane connector, drag it from the enclosure along guide rails.

7. It is up to you what to do with the board next.

4.4 Installation of CPC510 peripheral devices

CPC510 is available for connection of many various peripheral devices, which installation methods could vary greatly. The next sections contain only general guidelines for installation, rather than detailed algorithms.

4.4.1 Installation of MicroSD memory cards

CPC510 is equipped with XS10 connector for MicroSD memory card. External view of the Secure Digital connector with the installed memory card is shown on Fig. 2-6.
Carefully insert the properly positioned Secure Digital card into the connector along the guide rails and slightly push on it until the contacts fully fit into the connector.

Notice
We recommend using MicroSD-cards formatted on this device.

Attention!
While replacing MicroSD card, be careful, since the cooling heat sink will be hot.

4.4.2 Connection of USB devices

CPC510 supports the use of any computer peripheral USB-devices Plug&Play (e.g. keyboard, mouse, printer etc.).

Notice
All USB-devices can be connected or disconnected while the power of devices and head system is on.

4.4.3 Battery replacement

Replacement of lithium battery requires the same battery or a battery recommended by the manufacturer for replacement. The most likely match is Panasonic BR2032 or other compatible batteries.

Important notice:
During battery replacement, please follow the battery polarity.
Battery should be replaced with the identical one or the one recommended by manufacturer.
The used battery should be recycled according to the set standards.

An expected period of operation of the battery with capacity of 190 mAh is approximately 5-6 years if operated 8 hours a day at the ambient temperature of 30°C. However, battery life strongly depends on operating temperature, as well as on how long system appears to be off.
It is recommended to change the battery each 4-5 years of operation, before the end of its service life.

4.5 Installation of MIC584 mezzanine board

MIC584 is installed into XS6 connector of CPC510. Sequence of MIC584 installation into the CPU board is demonstrated in the User Manual for MIC584.

4.6 Installation of software

Installation procedure of Ethernet-drivers and drivers of all the installed peripheral devices is described in files supplied with the drivers.
This User Manual does not also contain description of operating system installation procedure. Please refer to the documents, attached to the operating system.

5 System settings

5.1 Operating mode of PCI-Express

Operating mode of PCI-Express 3 x1

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5.2 Reset of BIOS to factory settings and switching over to Transparent mode

If the system fails to boot (e.g. due to improper BIOS configuration or incorrect password), the setting parameters stored in CMOS, can be cleared by SA1 switch located in the top right corner of the board – see. Fig.1-3.

Fig. 5-1: Switch of SA1 operating mode of CPC510

SA1 enables to perform the following actions:

- Reset BIOS Setup to default settings
- Forced change of the board to the Transparent mode.

The switch position is shown in the table:

Table 5-1: Possible options of CPC510 board configuration using SA1 switch

Switch number (shown on the enclosure)	**Switch purpose**	**SA1 switch position (see Fig. 5-1)**	**Function**
1	Reset of BIOS Setup settings to default settings	OFF	Position when delivered
1		ON	Reset of BIOS Setup settings to default settings*
2	Forced change of the board to the Transparent mode	ON	Board automatic change to the Transparent mode (by default)
2		OFF	Forced change of the board to the Transparent mode

* Sequence of BIOS setup settings to factory settings:
1. Switch off the power supply;
2. Remove CPC510 from the sub-rack;
3. Set the SA1.1 operating mode switch to ON position for 5 seconds;
4. Return the SA1.1 switch to OFF position
5. Install CPC510 into the sub-rack
6. Switch on the power.

6. Phoenix® BIOS

Your PC has an adapted Phoenix® BIOS version being a standard system for IBM PC AT-compatible PCs. It supports Intel®x86 CPUs and Intel®x86 compatible CPUs, provides a low-level support for CPU, memory and I/O subsystems.
Using BIOS Setup you can change BIOS parameters and control special PC operating modes. This program is activated by pressing of F2 button and uses menu system for making changes as well as for switching on and switching off special functions. It makes possible for you to change the main system setting parameters. These parameters are stored in a special storage zone of the flash BIOS microchip, which stores information after system power supply is off.

7 Additional information

7.1 Temperature mode control

Intel IvyBridge CPUS operate under severe thermal conditions. This requires special measures for maintaining temperature of the CPU crystal die within the limits of acceptable values.
The following sections provide developers of CPC510-based systems with information required for meeting temperatures standards and requirements
.

7.1.1 Passive temperature control

The structure of CPC510 temperature conditions control can be represented as particular functions, which purpose is to protect CPU and reduce its power consumption. The use of thermal control circuits allows CPU to maintain safe operating temperature without special software drivers and interrupt handling procedures.
CPU thermal protection functions:
1. "Catastrophic shutdown detector" ensures CPU switching off when the crystal die reaches the temperature of about 105°C in case of the cooling system malfunction. This function is always active in order to protect SPU in any case. Temperature controller circuit is not switched off automatically when the temperature goes below the "thermal trip" level: BIOS settings should be reset for system reboot. Reset of BIOS settings is carried out according to the sequence described in section 5.2. When device operates without batteries, it is sufficient only to reboot the power supply unit.
2. Enhanced SpeedStep®: when crystal die core temperature exceeds 100°C, CPU will be dynamically switched to the low power consumption mode with the reduced operating voltage of the core and intrinsic multiplication factor.
3. External temperature monitor (LM87) is designed for collecting information on CPU temperature and board surface temperature. An additional temperature monitor controls the temperature of memory chips. This information could be used by control program in order to take the necessary measures.
If CPC510 operates under CompactPCI normal operating conditions with the sufficient air circulation, there is no need for the temperature control function. However, in cases where environmental parameters are not the best possible ones for the board based on Intel IvyBridge, temperature control functions are activated to ensure operation stability. Thermal mode control makes it possible for the developers to create cheap solutions, not compromising on system reliability and integrity.

Attention!!!
While carrying out supervisory tasks and performance tasks all thermal control functions should be disabled. Otherwise, erroneous results can be obtained.__

7.1.2 Heat dissipation by heat sink and system enclosure

Specially developed cooling heat sinks ensure the best basis for stable operation and long-term reliability. When they are used together with the system enclosure which provides opportunity to control airflow parameters, the controlled dissipation of heat energy is guaranteed.
All CPC510 versions are equipped with the optimally designed cooling heat sinks. Their size, form and structure ensure the best thermal resistance values (Rth). Furthermore, they are designed for heavy use of the forced-air system of enclosures of the modern CompactPCI systems.
While designing solutions for CPC510, the developer should take into account system thermal performance in general. He/she should use such system enclosure which meets heat removal requirements. During thermal calculations it is required to consider the role of peripheral devices in the general system heat dissipation.
The peripheral devices, in turn, should be equipped with thermal performance characteristics corresponding to the operating temperature range of the board and system in general.

Attention!!!
Since Fastwel Group will not be responsible for damages to CPC510 and other equipment, caused by CPU overheating, system developers and end users are strongly recommended to make sure that peripherals of CPC510 do meet the imposed temperature requirements.

7.1.3 Board cooling recommendations

- For all the boards, the forced-air cooling function extends the temperatures range where CPU operates with maximum efficiency.
Therefore, those who use systems based on CPC510 are strongly recommended to use sub-racks with integrated internal air cooling.
- We do not recommend using the boards with R1 heat sink (4HP) without air cooling. Since, if such boards are used in the sub-rack without cooling, theses boards tend to self-heating due to the lack of convection between flared fins of the heat sink with a fine pitch. In which case even a minimum air cooling is able to significantly expand the operating range of ambient temperature values.
- It is not recommended to use the board with 2.5 GHz without air cooling. High CPU capacity heats up both the heat sink and PCB itself, which has a negative impact on operation of all the components installed on the board.
- It is recommended to use standard Schroff sub-rack fans for the use in systems based on CPC510 CPU boards.

7.2 Power consumption of CPC510

Supply voltage +5V_STBY,+12V.
Consideration should be given to the specified requirements essential to ensure stability and reliability. The below table contains values of the maximum permissible voltages on power lines, exceeding of which could lead to the board damages. Power supply units which will be used with CPC510 should be tested with respect to compliance with such requirements.

Table 7-1: Power consumption parameters of CPC510

Voltage (V)	Minimum (V)	Maximum (V)	Current consumption MAX (V)
CPCI			
+5V_STBY	4.75	5.25	2
+12	11.4	12.6	6

If the supply voltage exceeds the specified limits, board functionality cannot be guaranteed.
The backplane should ensure an optimum allocation of the supply voltages. It is recommended to use only those backplanes which should have two power rails for each of the voltages.
Connection of power lines and backplane should guarantee minimum losses and stable performance capabilities. Long feeding lines, small section conductors and high-resistant connections should be avoided.
It is recommended to use power supply units with voltage control function. It could also require the use of relevant backplane.
The load-supplying capacity should be sufficient for considering possible deviations of electronic component characteristics.

7.3 Compliance with safety requirements for CPC510

CPC510 complies with the general safety requirements for information technology equipment as defined in IEC 60950-2002 standard (for the equipment connected to electric mains, voltage up to 600V).

7.4 Operating conditions

lDevice ensures safe operation in case of the following climatic and mechanical effects:

Table 7-2: Parameters of the climatic and mechanical parameters (CPC510)

Type of effect	Parameter name	Parameter value	Document
Change of temperatures	Low temperature	- 40°C (0*)	IEC 60068-2-14
	High temperature	+ 85°C (+70*)	
Humidity	Relative humidity	Up to 80%,non-condensing	IEC 68-2-14-84
Damp heat (+55°)(for coated equipment)	Relative humidity	Up to 93%	IEC 68-2-30-82
Sinusoidal vibration	Range of frequencies (Hz)	10…500	IEC 60068-2-6
	Acceleration, g	5	
Single shocks	Peak acceleration	100	IEC 60068-2-27
Multiple shocks	Peak acceleration	50	IEC 60068-2-29
	Number of shocks	1000	

**For commercial version*

Note
The tested devices comply with the declared mechanical load requirements provided that the followings conditions are met:
Additional fixing of USB devices is required (e.g. fixing with mastic adhesive).

7.5 Cooling system requirements

The board should be able to operate within the declared temperature ranges with the forced air cooling as part of its structure. The total maximum output dissipated by CPU and South Bridge amounts to: ~50W. In addition to it, heat sink removes heat from the network controller and two PCI Express Switches. It is recommended to make preliminary thermal calculation of the cooling system.

Chip	Dissipated heat (W)	Maximum temperature
IvyBridge	CPU 17(25)(45)(*)	100(**)
PCI-E Switch	2x 5	125
Gigabit Ethernet Controller	2	100
PantherPoint PCH	4.5	100
DDR3-1600 8GB ECC	12	(Tcase = +85)***

**The capacity is specified at maximum frequency and maximum CPU load*
***The maximum crystal die temperature is specified before SpeedStep is switched on.*
****When the temperature rises (Tcase +70°), CPU performance is reduced.*

Annex A

A MIC590 Board

A.1 Introduction

MIC590 board is designed to be used jointly with CPC510 CPU board and serves to extend basic functions of the specified CPU board. MIC590 is intended for the systems, used under harsh conditions.
MIC590 is contained in CPC510-02 CPU board (see Fig. 1-7 and Fig. 1-8).
CPC510 versions are shown on Fig. 1-1. In terms of design, MIC590 is installed to the left from CPC510 CPU board and is fed from the backplane. MIC590 board is implemented in 3U Eurocard format.
The board has the following structure of I/O channels:
- 32-bit PCI/PCI-X Bus, clock frequency of 33/66 MHz, Master mode.
Support for up to seven Bus Mastering devices;
- Display Port interface;
- Dual channel LVDS interface, compatible with ANSI/TIA/EIA-644 specification.

A.2 MIC590 functional capabilities

- **Video outputs:**
- DisplayPort connector (resolution up to 2560x1600@60 Hz) routed to the front panel;
- Dual channel LVDS interface (25 MHz-112 MHz, up to 224 Mpx/s), switchable between the onboard connector and via RIO backplane;
- Support for TFT-panel power control with the supply voltage of 3.3 V and lighting circuits of 5 V or 12 V (XP3 connector).

- **CompactPCI bus:**
- 32-bit, clock frequency of 33/66 MHz;
- Operation mode – System Master, support for up to seven Bus Mastering devices;
- Support for PCI Local Bus Rev. 3.0 specification;
- Support for 3.3V and 5V VIO;
- Left-sided location of board makes it possible to connect standard Compact PCI backplane for the creation of hybrid systems.

- **PCI Express bus**
- 3x ports x1 (transit of PCI Express PCH ports of CPC510);
- Complies with the PCI Express 1.0a specification;

- Complies with the PICMG 2.30 Compact PCI PlusIO Specificaton;
- Allows for a module binding CPC510+MIC590 installation into a hybrid backplane, complies with the PICMG 2.30 specification. In which case a simultaneous support for four Legacy CompactPCI peripheral devices and three Compact PCI Serial peripheral devices is provided. Though, SATA and USB interconnects, which are parts of the PICMG 2.30 Specification, are not available).

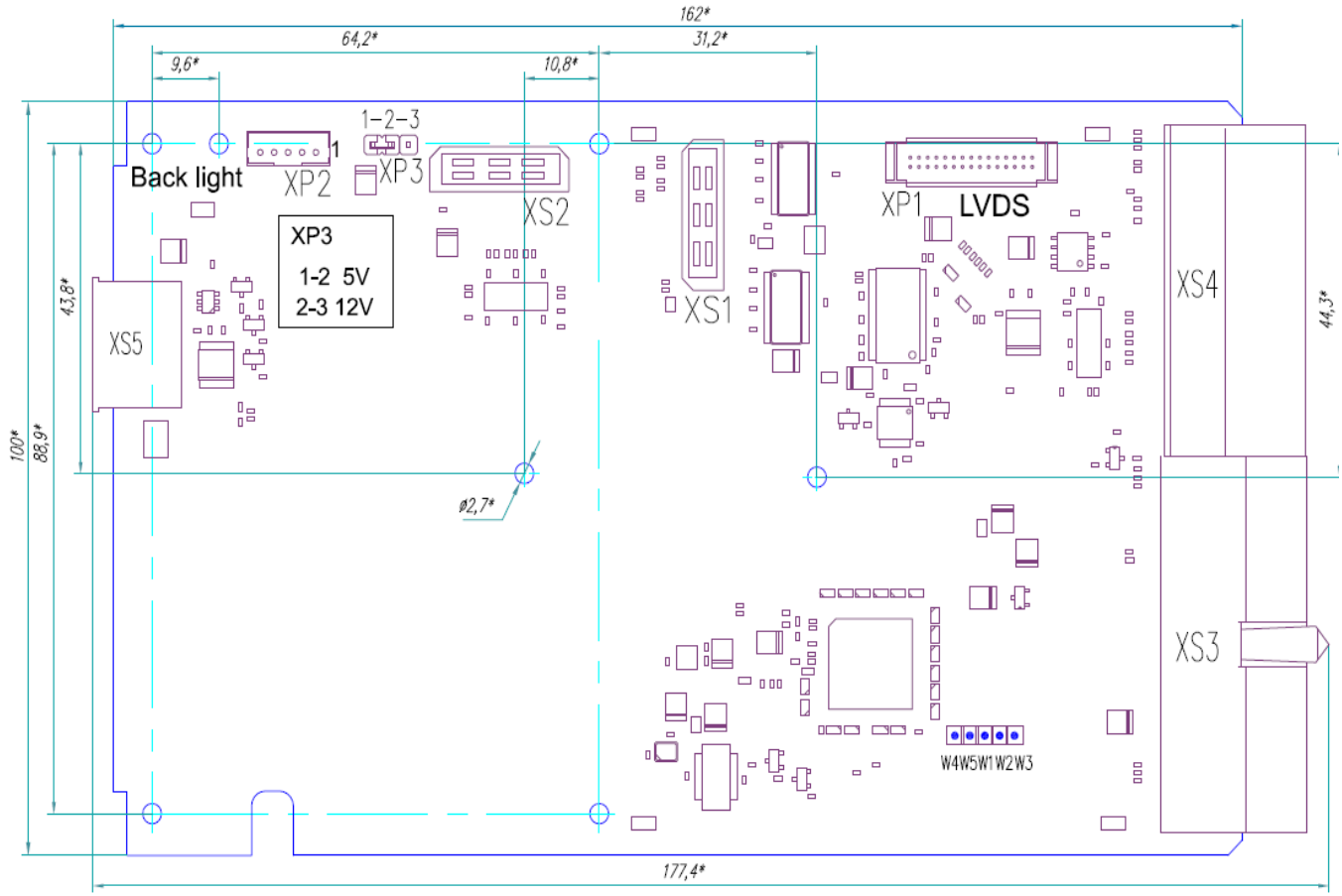
- **Power supply:**
- The MIC590 board power consumption is 2 W without regard to the consumption of the TFT panel and the illumination invertor;
- The maximum power consumption of a TFT panel connected to the MIC590 module is 6 W, and that of the illumination circuits is 10 W (for Upow = 5V) or 30 W (for Upow = 12V);
- The module does not utilize the voltage generated at the Compact PCI backplane for feeding its internal circuits.

- **Compatibility with OS:**
- MIC590 is compatible with the software which is designed for joint operation with CPC510 CPU board.

A.3 External view of MIC590 mezzanine board

External view of MIC590 is shown on the following figure:

Fig. A-1: MIC590 board (side that faces CPC510)

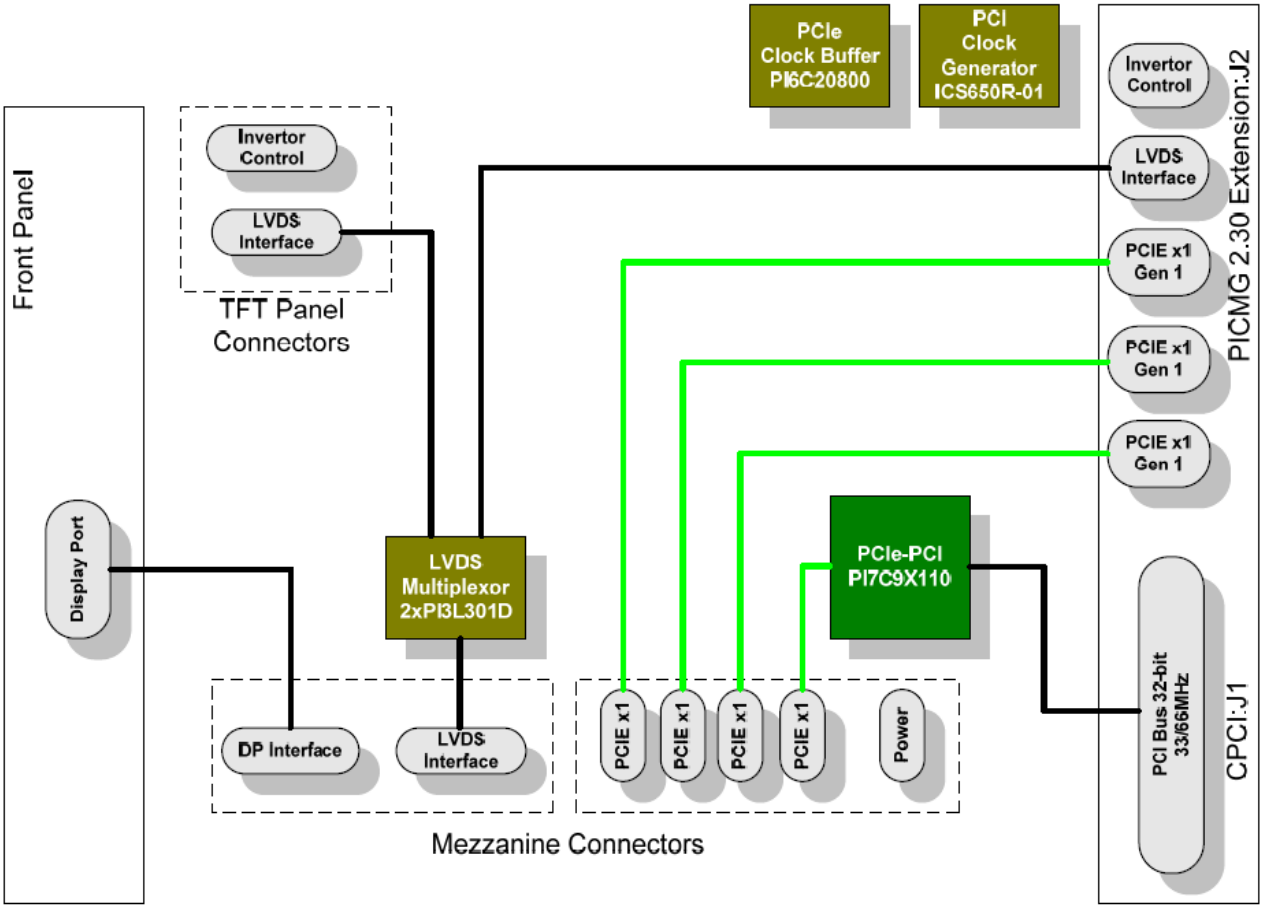


When CPC510-02 CPU board is delivered to consumers, XS1 and XS2 connectors of the MIC590 board are installed into XS8 and XS9 connectors of the CPC510 CPU board (see Fig. 1-4: Location of major components of CPC510 (bottom view)).

A.4 Functional units of MIC590

The block diagram of the device is shown on the following figure:

Fig. A-2: Block diagram of MIC590



• Display Port
The port is designed for connection of a digital display with the DisplayPort interface or for the further conversion to other video standards. Maximum resolutions supported (2560x1600@60 Hz). One port is routed to the front panel of the board.

• LVDS Port. LVDS Multiplexor PI3L301D
The port is designed for the connection of a digital TFT-panel with dual channel LVDS interface. Maximum resolution supported (1600x1200 @ 60 Hz). For universal applications, both in rear I/O systems (32-bit Legacy Compact PCI backplanes) and in systems with no rear I/O, an automatic I/O direction selector switch of LVDS interface is provided. Direction of LVDS interface output to the RIO is set automatically during installation of RIO board.
Control circuits of illumination control and power supply sequence are supported.

On MIC590, the LVDS-port is routed to the XP1 signal connector of Hirose DF13-30DP-1.25V type; XP2 connector of JST B 5B-PH-KL-LF-SN type for invertor connection. For utilizing LVDS-interface on RIO, the contacts of UHM-S110B3-5AP1-TG30 type connector are used (PICMG 2.30).

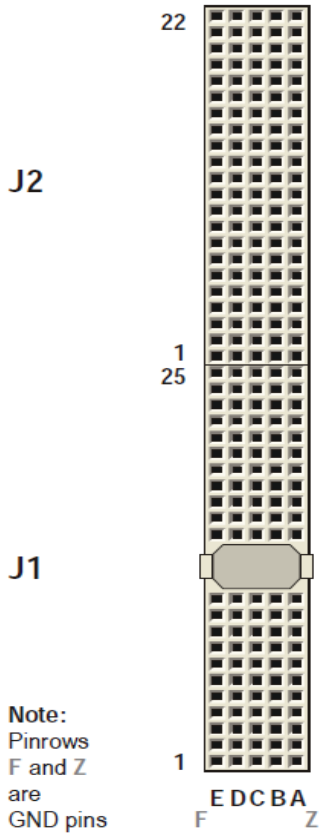
• **Compact PCI interface. PCI-E to PCI Bridge PI7C9X110.**
Compact PCI interface is designed for the connection of Legacy devices, corresponding to PICMG 2.0 specification. Compact PCI interface is generated via Pericom PCI Express-PCI PI7C9X110 bridge. The primary interface is a PCI-E Gen1 x1 channel generated on CPC510. The PCI-interface enables operation of up to seven 32-bit peripheral Bus Mastering boards with operating frequencies 33/66 MHz.

• **PCI Express interface.**
PCI Express interface is designed for the connection of high-speed peripheral devices and corresponds to the PCI Express Specification Rev. 1.0a. 3x PCIExpress ports x1 Gen 1 are generated in PCH microchip of CPC510 transit via the MIC590 board, routed to the UHM-S110B3-5AP1-TG30 type connector. Type and connector pin assignment corresponds to the requirements of PICMG 2.30 specification which enables to implement hybrid system with 3 peripheral boards of the Compact PCI PlusIO specification or Compact PCI Serial and 4 peripheral Legacy Compact PCI boards.

A.5 CompactPCI connector of MIC590 board

MIC590 is designed in correspondence with the CompactPCI bus architecture. MIC590 Uses two connectors of CompactPCI interface: J1 and J2 (they are numbered in accordance with international specification). The CompactPCI standard is electrically identical to the local PCI bus, but it had some improvements which make it possible to use them under harsh operating conditions with the increased amount of extension slots.

Fig. A-3: J1 and J2 CompactPCI connectors



On MIC590, CompactPCI connectors are indicated as follows:
XS3 (corresponds to J1 connector of the CompactPCI specification) and XS4 (corresponds to J2 connector of the CompactPCI 2.30 specification).

MIC590 connectors (XS3 и XS4) are indicated as shown on Fog. A-1.

Annex B

B Useful Abbreviations, Acronyms and Short-cuts

Abbreviation	Meaning
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
AGTL	Advanced Gunning Transceiver Logic
BIOS	Basic Input-Output System
BMC	Baseboard Management Controller
CRT-display	Cathode Ray Tube Display
DAC	Digital-Analog Converter
DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory
DMA	Direct Memory Access
DMI	Direct Media Interface
DVMT	Dynamic Video Memory Technology
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface (Universal Serial Bus specification)

Abbreviation	Meaning
EIDE	Enhanced Integrated Drive Electronics
EOS	Electrical Overstress
ESD	Electrostatically Sensitive Device Electrostatic Discharge
FSB	Frequency System Bus
FWH	Firmware Hub
GMCH	Graphics and Memory Controller Hub
I_2C™	Inter Intergrated Circuit
LCD	Liquid crystal display
LPC	Low Pin Count
LVDS	Low Voltage Differential Signal
MDI	Media Dependent Interface
PC	Personal Computer
PIO	Programmed Input/Output
PLCC	Plastic Leaded Chip Carrier
PM	Peripheral Management Controller
POST	Power On Self Test
PSB	Processor System Bus

Abbreviation	Meaning
PWM output	Pulse-Width Modulation
RAMDAC	Random Access Memory Digital-to-Analog Converter
RTC	Real Time Clock
SMB	System Management Bus
SMBus	System Management Bus
SODIMM	Small Outline Dual In-Line Memory Module
SoM	System on a module
SSD	Solid State Disk
TFT	Thin Film Transistor
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver-Transmitter
UHCI	Universal Host Controller Interface
USB	Universal Serial Bus
UTP	Unshielded Twisted Pair