CPC512

3U CompactPCI Intel IvyBridge (2/4 Cores) CPU board

User Manual

-

August 2016

Version 1.1

Product Title: **CPC512**
Document name: **CPC512 User Manual**
Manual version: **1.1**

Revision Record

This User Manual covers CPC512 (version with forced air cooling) and CPC512RC (version with conduction cooling).

Revision No	Brief description of changes	Board index	Revision date
1.0	Initial version	CPC512/ CPC512RC	August 2016

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Ownership Rights

Notation Conventions

Warning, high voltage!

This sign and inscription warn you about the dangers associated with electric discharges (> 60 V) at the time you touch the device or its parts. Noncompliance with the safety precautions, mentioned or prescribed by the rules could endanger your life or health, or lead to product damages. We also recommend you to familiarize with the below subsection dedicated to the high voltage safe handling rules.

Warning!
ESD Sensitive Device!

This symbol draws your attention to the information related to electro static sensitivity of your product and its components. To keep product safety and operability it is necessary to handle it with care and follow the ESD safety directions.

Warning! **Hot surface!**

This sign marks warnings about hot surfaces. The surface of the heatsink and some components can get very hot during operation. Take due care when handling, avoid touching hot surfaces!

Warning!

Information marked by this symbol is essential for human and equipment safety.
Read this information attentively, be watchful.

Note

This symbol and title marks important information to be read attentively for your own benefit.

Safety requirements

This product is designed and tested for the purpose of ensuring compliance with the electric safety requirements. Its design guarantees long-term failsafe operation. Life cycle of the device can be sufficiently reduced due to improper handling during unpacking and installation. Therefore, for your own safety and in order to ensure the proper operation of the device, you should observe the below recommendations.

High Voltage Safe Handling Rules

Warning!

All the works that involve this device should be carried out by the appropriately qualified personnel.

Warning, high voltage!

Before installing the board into the system make sure that the mains supply is switched off. This also applies to the installation of extension boards.

During installation, repairs and maintenance of the device there is a real danger of exposure to electric shock, therefore you should always disconnect the power supply feeding cable from the socket at the time of works. This also applies to the other power supply feeding cables.

Board Handling Regulations

ESD Sensitive Device!

Electronic boards and their components are sensible to static electricity. This is why you should give special attention to handling
with these devices in order to ensure their integrity and working efficiency.

- - Do not leave the board without protective packaging, when it is not operated.
- - When applicable, always operate the board at the workplace equipped with protection against static electricity. If it is impossible, the user should remove a static discharge before touching the device by hand or using tools. The best way to do it is touch a metal part of system enclosure.
- Observing safety precautions are particularly important during the works associated with replacement of extension boards, memory modules, jumpers etc. If the device is equipped with the batteries for supplying power to memory or real-time clock, do not place the board on such conducting surfaces as antistatic pads or mats. They could cause short-circuit and lead to damages of the battery or board's conductive circuits.

General Board Operation Rules

- To keep the warranty, the product should not be altered or revised in any way. Any alterations or improvements not authorized by Fastwel LLC, except for those specified in this document or obtained from the technical support department of Fastwel LLC as a set of instructions for their implementation, cancel the warranty.
- This device should be installed and connected only to the systems, meeting all the necessary technical and climatic requirements. This above is also true to the operating temperature range of a particular version of the board. You should also consider temperature limitations of the board.
- While performing all the required operations for installation and adjustment, please follow the instructions specified only in this document.
- Keep the original package for subsequent storage of the device and transportation in the warranty event. If it is necessary to transport or store the board, please pack it the same way as it was packed upon delivery.
- Exercise special care when unpacking and handling the device. Act in accordance with the instructions given above and in the paragraph 8 Transportation, unpacking and storage.

MANUFACTURER'S WARRANTIES

Warranty liabilities

The manufacturer guarantees compliance of CPC512 to the requirements of IMES.469555.001 TS technical specifications "Modules in 3U CompactPCI Serial format" (IMES.469555.002 TS "Modules in CompactPCI Serial 3U-RC format" for CPC512RC modules) provided that the Consumer observes operation, transportation, storage, installation and mounting conditions, specified by the accompanying documents. The Manufacturer hereby guarantees that the products supplied thereby are free from defects in workmanship and materials, provided operation and maintenance norms were observed during the currently established warranty period. The Manufacturer's obligation under this warranty is to repair or replace free of charge any defective electronic component being a part of a returned product. Products that broke down through the Manufacturer's fault during the warranty period will be repaired free of charge. Otherwise the Consumer will be invoiced as per the current labor remuneration rates and expendable materials cost.

Liability limitation right

The Manufacturer shall not be liable for the damage inflicted to the Consumer's property because of the product breakdown in the process of its utilization.

Warranty period

The warranty period for the products made by Fastwel LLC is 36 months since the sale date (unless otherwise provided by the supply contract).

The warranty period for the custom-made products is 60 months since the sale date (unless otherwise provided by the supply contract.

Limitation of warranty obligations

The above warranty obligations shall not be applied:

- To the products (including software), which were repaired or were amended by the employees, that do not represent the manufacturer. Exceptions are the cases where the customer has made repairs or made amendments to the devices in the strict compliance with instructions, preliminary agreed and approved by the manufacturer in writing;
- To the products, broken down due to unacceptable polarity reversal (to the opposite sign) of the power supply, improper operation, transportation, storage, installation, mounting or accident.

Procedure of device returning for repairs

Sequence of activities when returning the products for repairs:

- Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization;
- Attach a failure inspection report with a product to be returned in the form, accepted by the Manufacturer, with a description of the failure circumstances and symptoms;
- Carefully package the product in the antistatic bag and carton box, in which the product had been supplied. Then package the product in a safe container for shipping. Failure to package in antistatic material will VOID all warranties.
- The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer.

1 Introduction

CPC512 CPU module is designed for providing consumers with highly integrated solutions in CPCI Serial 3U form factor for the purpose of using in real-time systems, manufacturing control, high-speed acquisition and processing of data. CPC512 is an extension of the range of 3U CPCI modules, manufactured by Fastwel
Ltd. The module is based on Intel Ivy Bridge CPU (2 or 4 cores).

CPC512 uses high speed I/O interfaces (PCI-Express, Gigabit Ethernet), it supports up-to-date video image processing technologies. Modular architecture of the device enables to flexibly adjust the system for particular application areas, thereby optimizing the price/quality ratio.

For extending functional capabilities of CPC512 there is MIC584 mezzanine module, which detailed description is given in the User Manual IMES.421459.584 UM.

CPC512RC CPU Module with the conduction type cooler is developed on the basis of CPC512 module and is designed for building special-purpose high-performance rugged systems.

The main difference of CPC512 module is that CPC512RC is equipped with specially developed heat-spreading cassette in accordance with the CompactPCI Serial Mesh Backplane specification and PICMG 2.20 R 1.0 specification.

1.1 General features of CPC512/CPC512RC module

- **Intel IvyBridge CPU (2 or 4 CPU cores)**
- **RAM**
  - DDR3L SDRAM 1066, 1333 MHz with ECC up to 8 GB soldered, two channel.
- **Video output (simultaneous output to two displays)**
  - Two DisplayPort connectors (resolution up to 2560x1600@60Hz), routed to the front panel.
- **LPC bus (except for CPC512RC and IMES. 421459.512-03)**
  - Routed to mezzanine connector.
- **PCI-E bus**
  - CPU hosts. Support of PCI-E 3.0 (up to 8 GT/s).

  - routed via PCI-E switch Gen 3.0 to J1 and J2 CPCI Serial connectors with support of up to two x8 devices.
  - support of Non-Transparent operation mode for FatPipe#1 x8 port.
  - support of DMA mode for x8 ports.
  - routed to J4 CPCI Serial connector with support of up to two x4 devices.
  - PCH hosts. Support of PCI-E 2.0 (up to 5 GT/s).

  - routed to J4 CPCI Serial connector with support of up to four x1 devices.
- **SMBUS**
  - Compatibility with the 2.0 specification.
  - Speed up to 100 kbps.
- **FLASH BIOS**
  - 2 x 32 Mbit SPI-Flash.
- **MicroSD interface**
  - Support of SDHC 2.0 specification.
  - Connected to USB 2.0 interface.
- **SATA II interface**
  - Two interfaces for connection of drives are routed to the mezzanine connector and J3 CPCI Serial connector.
  - Interface routed to J3 CPCI Serial connector can be switched to mezzanine connector (see 2.5.11 SATA interface)
- **SATA III interface**
  - Two interfaces for connection of drives are routed to J3 CPCI Serial connector.
- **Two LAN 10/100/1000 Mb ports on PCI-E x4 Gen2**
  - Two ports are routed to the front panel connectors
  - Implementation of the server network adapter.
- **One LAN 10/100/1000 Mb port with AMT support**
  - Routed to J6 CPCI Serial connector.
- **USB ports**
  - 13 ports USB 1.1 (12 Mb/sec), USB 2.0 (480 Mb/sec) and 4x ports USB 3.0 (4.8 Gb/sec).
    - 2x USB2.0 ports are routed to the front panel connectors
    - 2x USB2.0 ports are routed to mezzanine connector.
    - 8x USB2.0 ports are routed to CPCI Serial connector.
    - 1x USB2.0 port is used for implementation of MicroSD interface.
    - 4x USB3.0 ports are routed to CPCI Serial connectors.

- **FRAM**
  - 32 KB, 1 KB of them represent a closed area for storing Bios Setup settings.
  - Implemented on SPI FPGA bus.
- **Real-Time Clock**
  - Powered from a lithium battery CR2032 (3 V).
- **Audio support (except for CPC512RC and IMES.421459.512-03).**
  - HD Audio interface is routed to mezzanine connector.
- **Watchdog**
  - Internal watchdog with program control capability
- **SGPIO interface**
  - Signaling support in accordance with the SFF-8485 specification.
- **Hardware monitor**
  - Implemented via SMBUS interface.
  - Monitoring of three power supply voltages.
  - Monitoring of CPU temperature.
  - Monitoring of PCB temperature.
- **Indication**
  - LED of board start diagnostics/Hot Swap indication.
  - LED of addressing to SATA drives.
  - Led of indication of module temperature mode.
  - LED of NT port state of PCI Express interface.
  - Two software-controlled LEDs (user LEDs).
- **Software compatibility with OS**
  - Windows 7 Embedded.
  - Linux 2.6.
  - QNX 6.5.0.
- **Power supply requirements**
  - Power supply voltage +12 V, +5 V_ working voltage.
- **Operating temperature of CPC512**
  - Industrial version: from -40°C to +85°C.
  - Commercial version: from 0°C to +70°C.
- **Operating temperature of CPC512RC**
  - Version CPC512RC-01: from -50°C to +90°C.
  - Version CPC512RC-02: from -50°C to +85°C.
- **Humidity**
  - Up to 80%, no condensation.
  - Up to 98%, no condensation for option /Coated.
- **Resistance to vibration/single shocks**
  - 2g/50g for CPC512.
  - 6g/75g for CPC512RC.
- **MTBF:**
  - no less than 100 000 hours.
- **Module weight:**
  - CPC512-01 with R1 heatsink – no more than 550 g.
  - CPC512-01 with R2 heatsink – no more than 700 g.

- CPC512-01 with R1 enhanced area copper heatsink – no more than 950 g.
- CPC512RC – no more than 950 g.

1.2 Differences between the main features of CPC512RC

The main features of CPC512RC correspond to the ones of CPC512 (given in the subparagraph 1.1). Specifics of CPC512RC are as follows:

- A conduction heat-spreading cassette is used instead of the finned heatsinks.
- XS6 mezzanine connector is not available.
- Installation of MIC584 is not provided.
- XP3 and XP9 industrial connectors are unavailable.
- CPC512RC corresponds to the Technical Specifications IMES.469555.002 TS.

1.3 CPC512 Configuration

CPC512 is currently manufactured according to this table:

Table 1-1.: Version of CPC512

CPC512 CPU Module	IMES.421459.512	CPC512-01-i72C1.7-RAM4096-R1-C	Dual Core CPU 1.7 GHz, 17 W, 4GB RAM, with low heatsink, 4HP. Commercial temperature range.
	IMES.421459.512-01	CPC512-01-i72C1.7-RAM4096-R2-I	Dual Core CPU 1.7 GHz, 17 W, 4GB RAM, with high heatsink, 8HP. Industrial temperature range.
	IMES.421459.512-02	CPC512-01-i74C2.1-RAM8192-R2-C	Quad-core CPU 2.1 GHz, 35 W, 8GB RAM, with high heatsink, 8HP. Commercial temperature range.
	IMES.421459.512-03	CPC512-01-i74C2.1-RAM8192-R1-C	Quad Core CPU 2.1 GHz, 35 W, 8GB RAM, with low copper enhanced-area heatsink, 4HP. Connector for installation of MIC584 mezzanine module is not available. Commercial temperature range.

User can choose the required version, using the ordering template (see Fig. 1-1). Take a look at the note in the end of this subparagraph. Please see also subparagraph 7.1.2 Cooling system of CPC512.

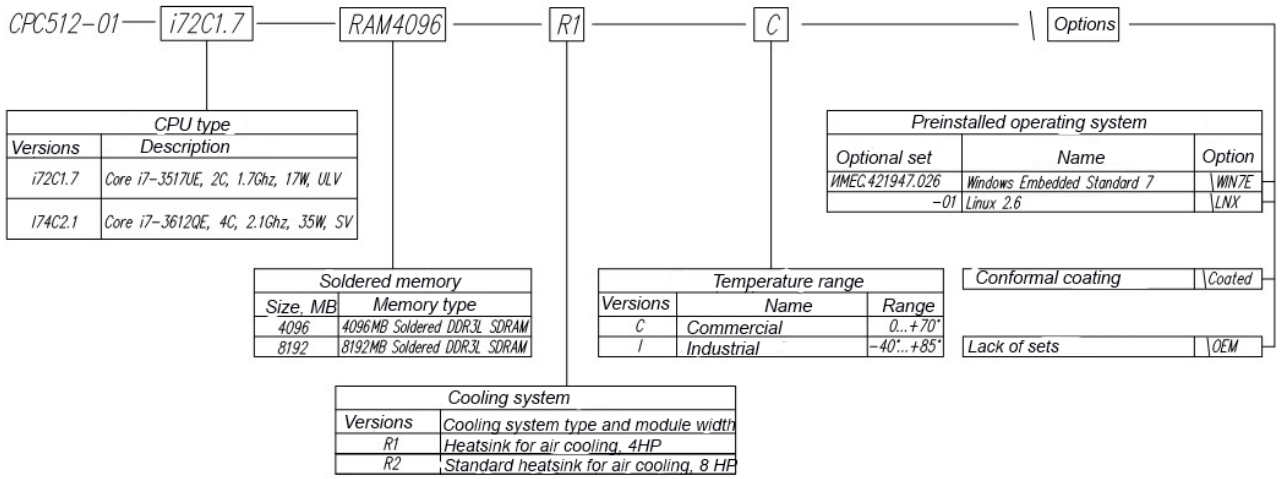


Fig. 1-1: Template for custom versions of CPC512

** For IMES.421459.512-03 R1 copper enlarged-area heatsink.*

Note

1. Version of CPC512 equipped with Intel i7-3612QE CPU 2.1 GHz is manufactured only for commercial range of operating temperatures (from 0 to + 70°C).
2. Version of the module equipped with Intel i7-3612QE CPU with the height of 4HP (IMES.421459.512-03), is manufactured with the low copper enlarged heatsink R1. In this case installation of MIC584 is not available.
3. Version of CPC512 equipped with Intel i7-3517UE CPU for industrial temperature range is manufactured with high R2 heatsink.
4. Forced cooling should be provided for all the versions of CPC512.

R1 heatsink (4HP) is implemented in two versions:

- Aluminum, blackened heatsink for operation with dual core Intel i7-3517UE CPU 1.7 GHz in commercial temperature range (see Fig. 1-2).

Fig. 1-2: CPC512 module with the installed aluminum heatsink R1 (4HP)

- Copper enlarged-area heatsink for operation with Quad Core Intel i7-3612QE CPU 2.1 GHz in commercial temperature range (see Fig. 1-3).

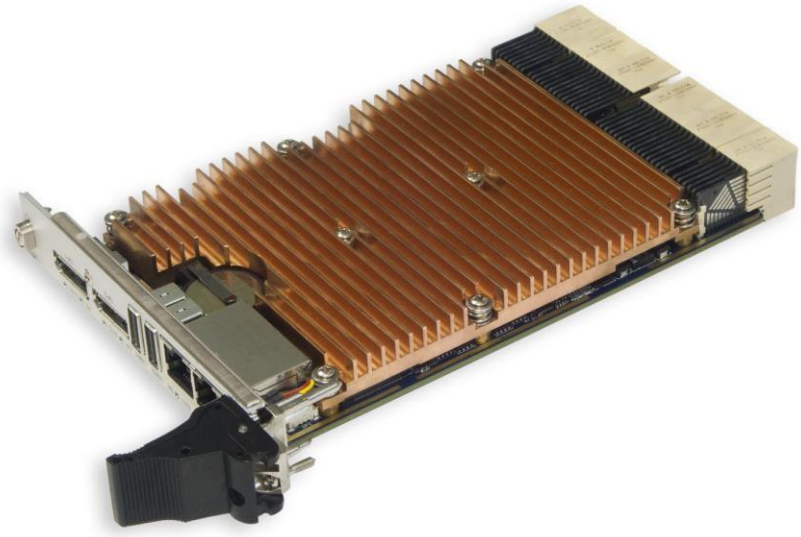


Fig. 1-3: CPC512 module with the installed copper heatsink R1 (4HP)

Note

Heatsink height enlarged in order to improve its cooling capabilities (no more than 15.2 mm from the board level) has no influence on the use of the module in CompactPCI crate.

Aluminum R2 heatsink, blackened (8HP), can be installed on CPC512 modules using both Dual Core Intel i7-3517UE CPU 1.7 GHz for operation in the industrial temperature range and with Quad Core Intel i7- 3612QE CPU 2.1 GHz for operation in the commercial temperature range (see Fig. 1-4).

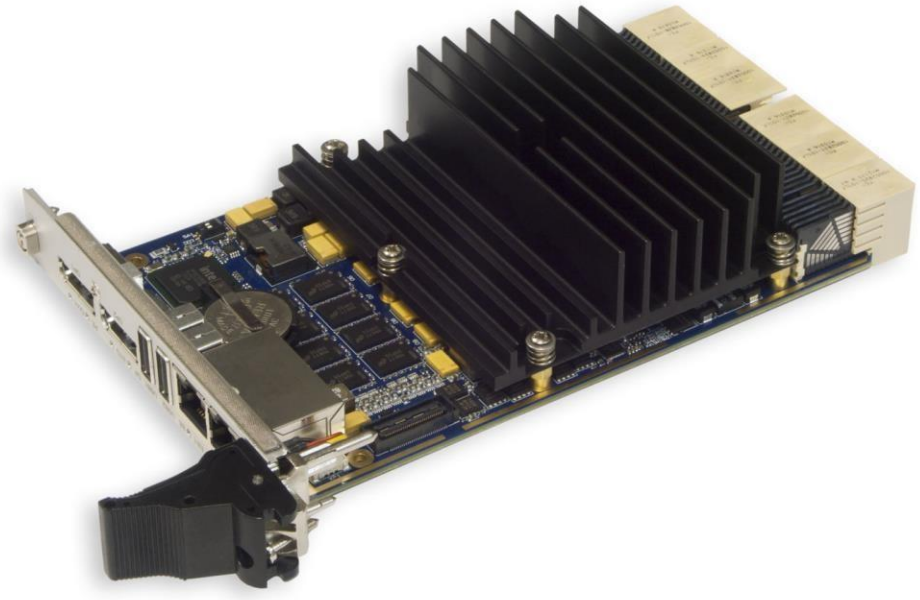


Fig. 1-4: CPC512 with the installed high (8HP) aluminum heatsink R2

1.4 Configuration of CPC512RC

CPC512RC is currently manufactured in accordance with the following table:

Table A-2: Version of CPC512RC

CPC512RC CPU Module	IMES.467449.004	CPC512RC-01	Dual Core CPU 1.7 GHz, 17 W, 4GB RAM, with conduction-type heatsink, 5HP.
	IMES.467449.004-01	CPC512RC-02	Quad Core CPU 2.1 GHz, 35 W, 8GB RAM, with conduction-type heatsink, 5HP.

User can choose the required version, using the ordering template (see Fig. 1-5). Take a look at the note in the end of this subparagraph. Please also see subparagraph 7.1.3 Cooling system of CPC512RC.

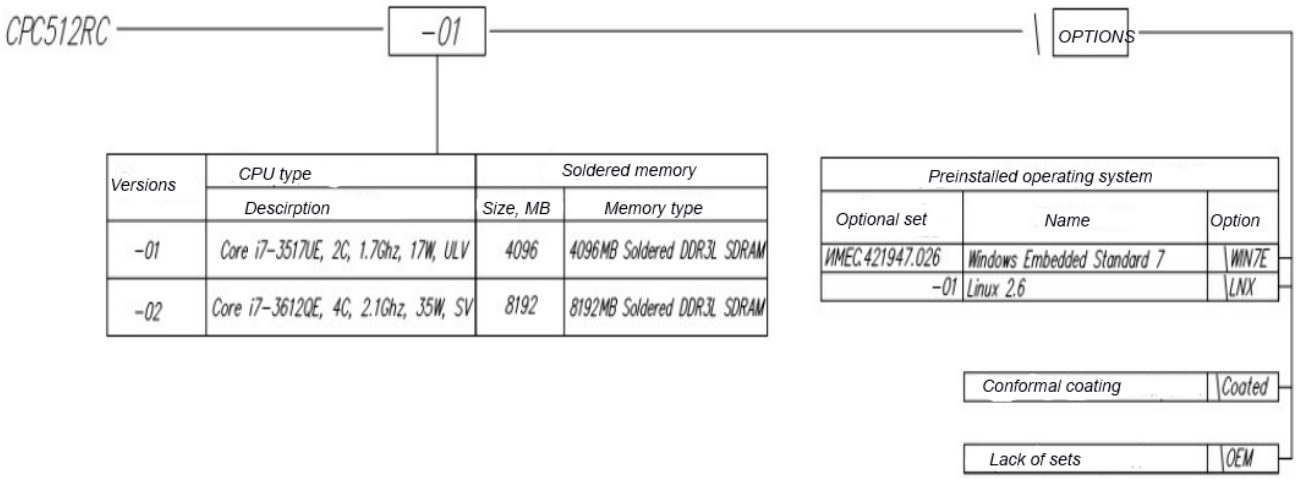


Fig. 1-5: Template for custom versions of CPC512RC

CPC512RC is shown in Fig. 1-12.

1.5 Delivery checklist of CPC512/CPC512RC

Module scope of delivery:

- CPC512 module
- Set of mounting parts (only for the CPC512RC version).
- -
- Packaging.

1.6 Packaging information

CPC512/CPC512RC is packaged in a box, which has the following overall dimensions: 350 x 260 x 70 mm.

Weight of packaged modules, in kg, no more than	CPC512	1.2
	CPC512RC	1.2

Note

Retain the original antistatic and consumer packages of the module till the end of the guarantee service life period.

1.7 Location of elements

Module versions could have slight differences, not shown in diagrams and figures.

1.7.1 Location of main components

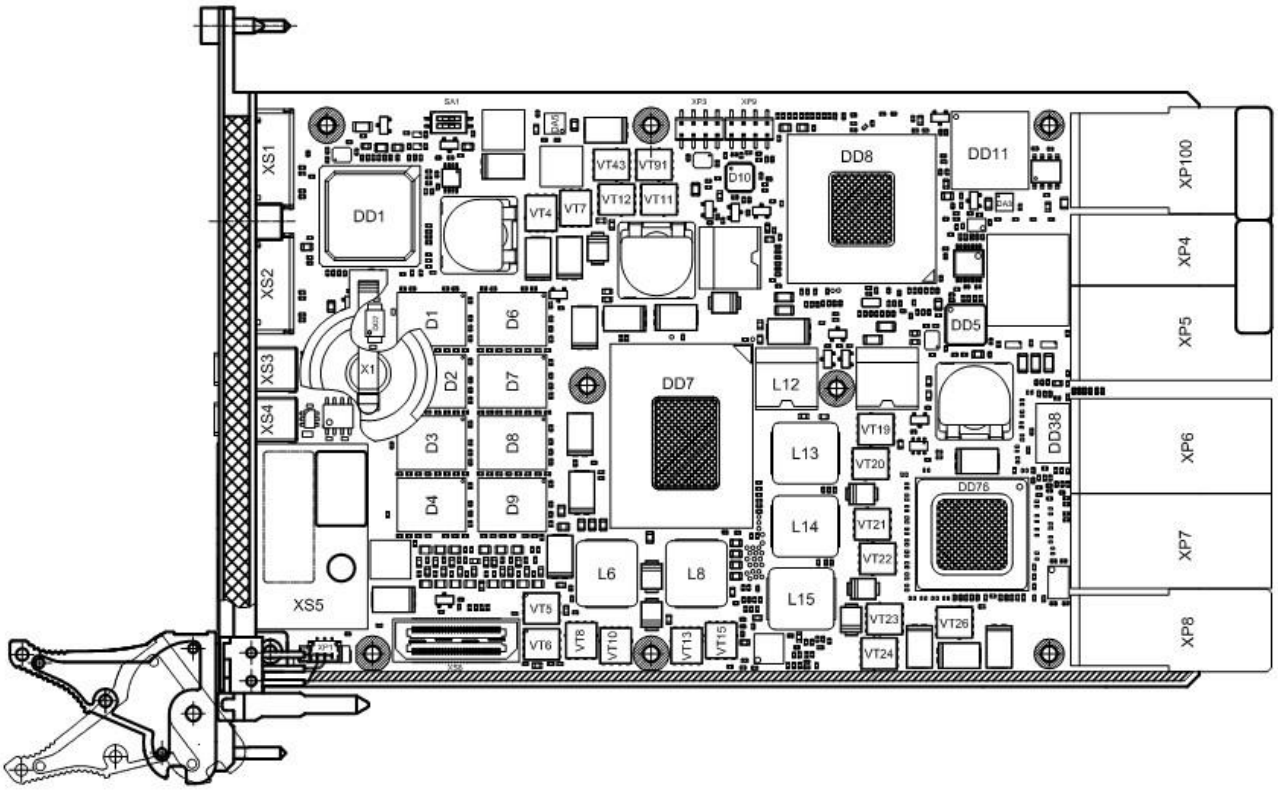


Fig. 1-6: Location of main components of CPC512 (top view)

External view of module versions could slightly differ from the one shown in the Figures.

This figure shows the top side of CPC512. Heatsink is not shown

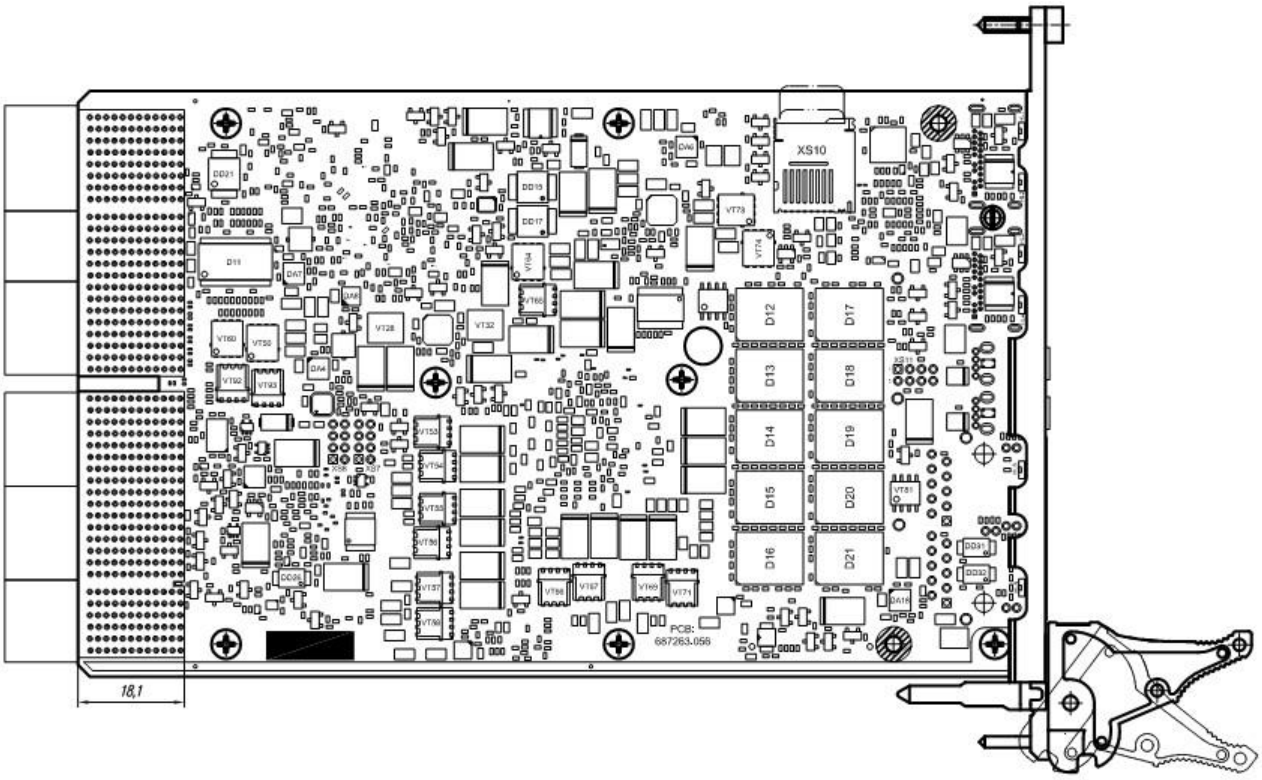


Fig. 1-7: Location of main components of CPC512 (Bottom view)

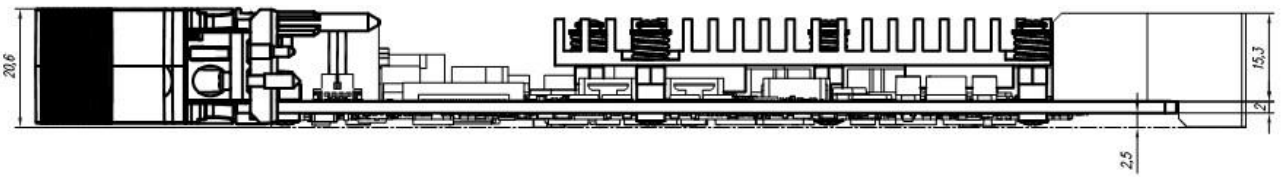


Fig. 1-8: CPC512 module with the installed R1 4HP heatsink (side view)

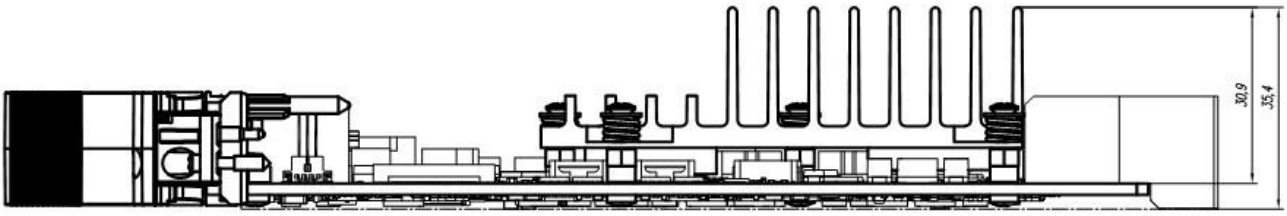


Fig. 1-9: CPC512 module with the installed R2 8HP heatsink (side view)

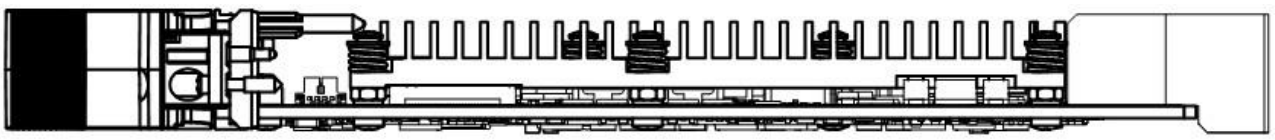


Fig. 1-10: CPC512 module with the installed copper R1 4HP heatsink (side view)

1.7.2 Front panel

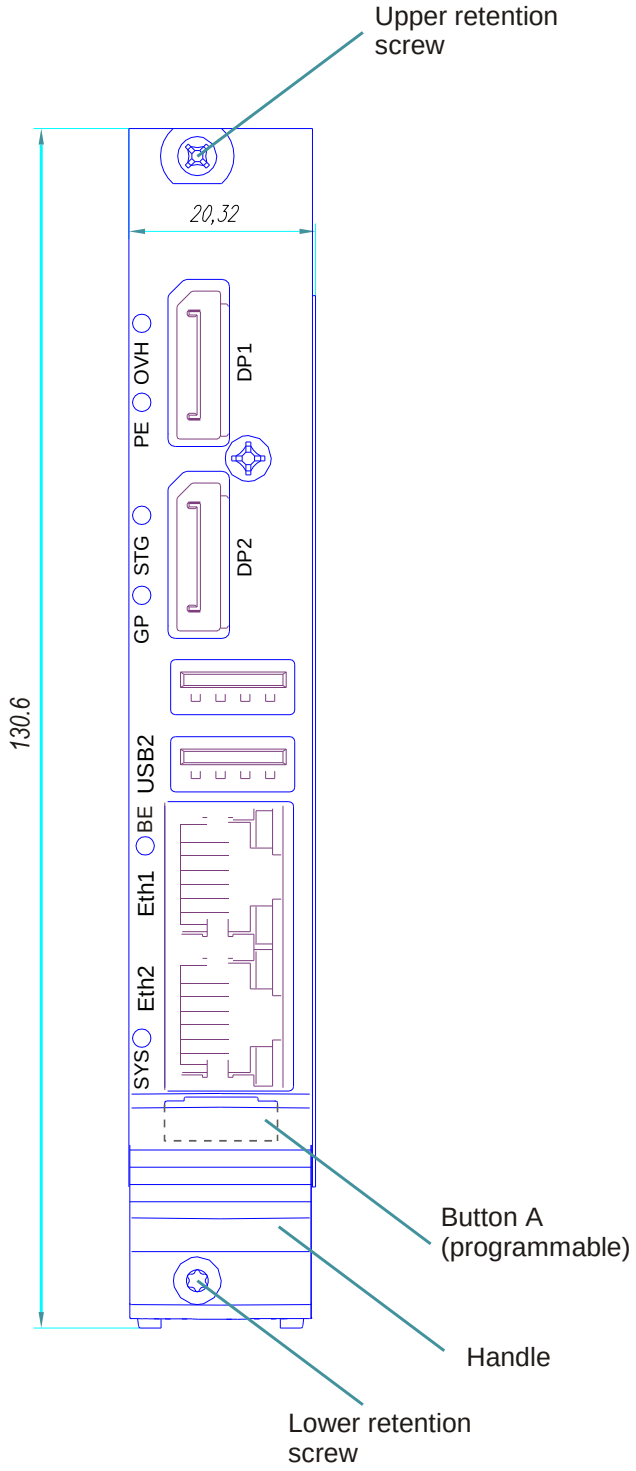


Fig. 1-11: Front panel of CPC512

External view of module versions could slightly differ from the one shown in the Figures.

Ejector button (shown as "button A" in the figure) performs mechanical function: serves for installation and removal of CPC512 (see subparagraph 4.2.1 Procedure of CPC512 installation and 4.2.2 Module removal procedure). In addition, the ejector button is a programmable switch, designed for manual initiation of the system, if necessary.

1.8 Location of CPC512RC elements

The below figures will help you identify components, their configuration and functions.

1.8.1 General view of CPC512RC

Fig. 1-12 shows the image of CPC512RC.

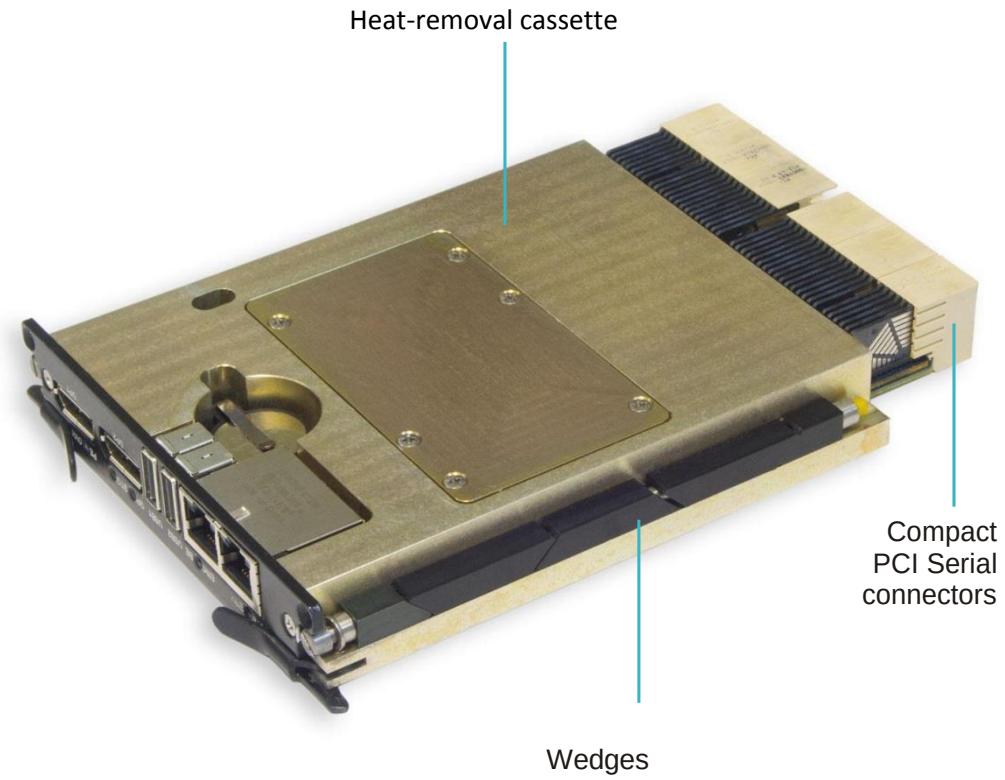


Fig. 1-12: CPC512RC module

External view of module versions could slightly differ from the one shown in the Figures.

Note

Color of the heat-removal cassette ranges from gray-blue to dark-gray with possible splotches, which is conditioned by particular properties of chemical coating.

Below you can see the figures with overall and mounting dimensions of CPC512RC (see Fig. 1-13, Fig. 1-14).

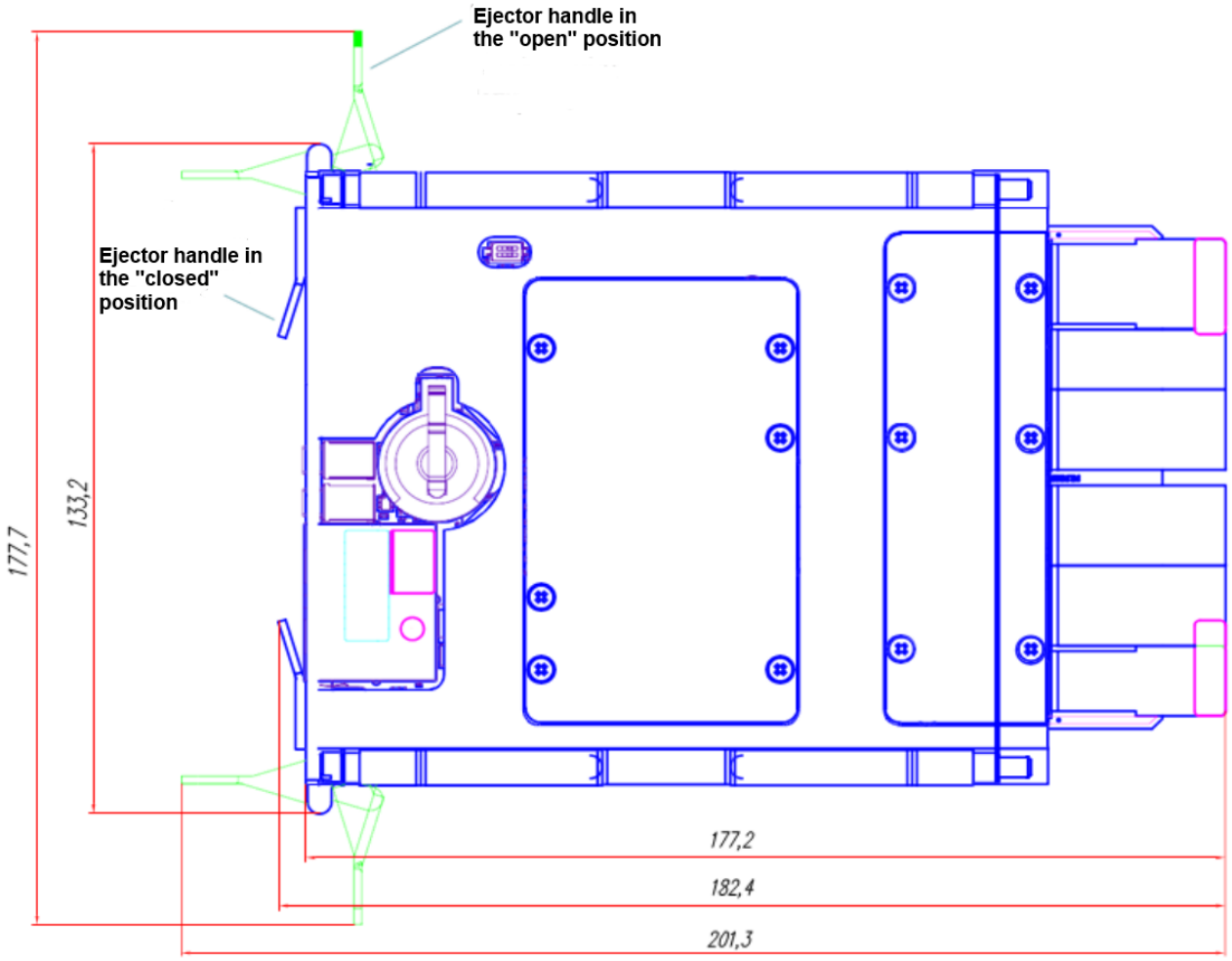


Fig. 1-13: Overall dimensions of CPC512RC

1.8.2 Front panel of CPC512RC

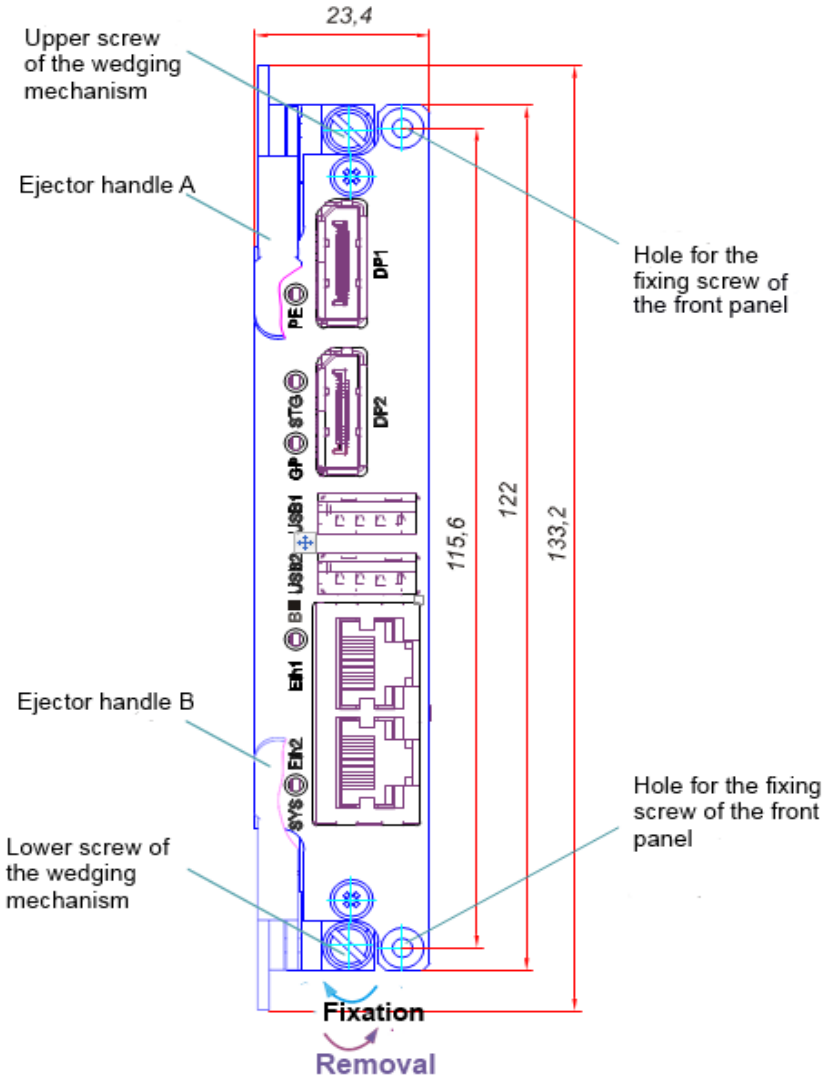


Fig. 1-14: Front panel of CPC512RC

External view of module versions could slightly differ from the one shown in the Figures.

Extractor handles A and B perform mechanical function: they are designed for installation/removal of CPC512RC (see subsection 4.3).

2 Functional description

2.1 Board layout

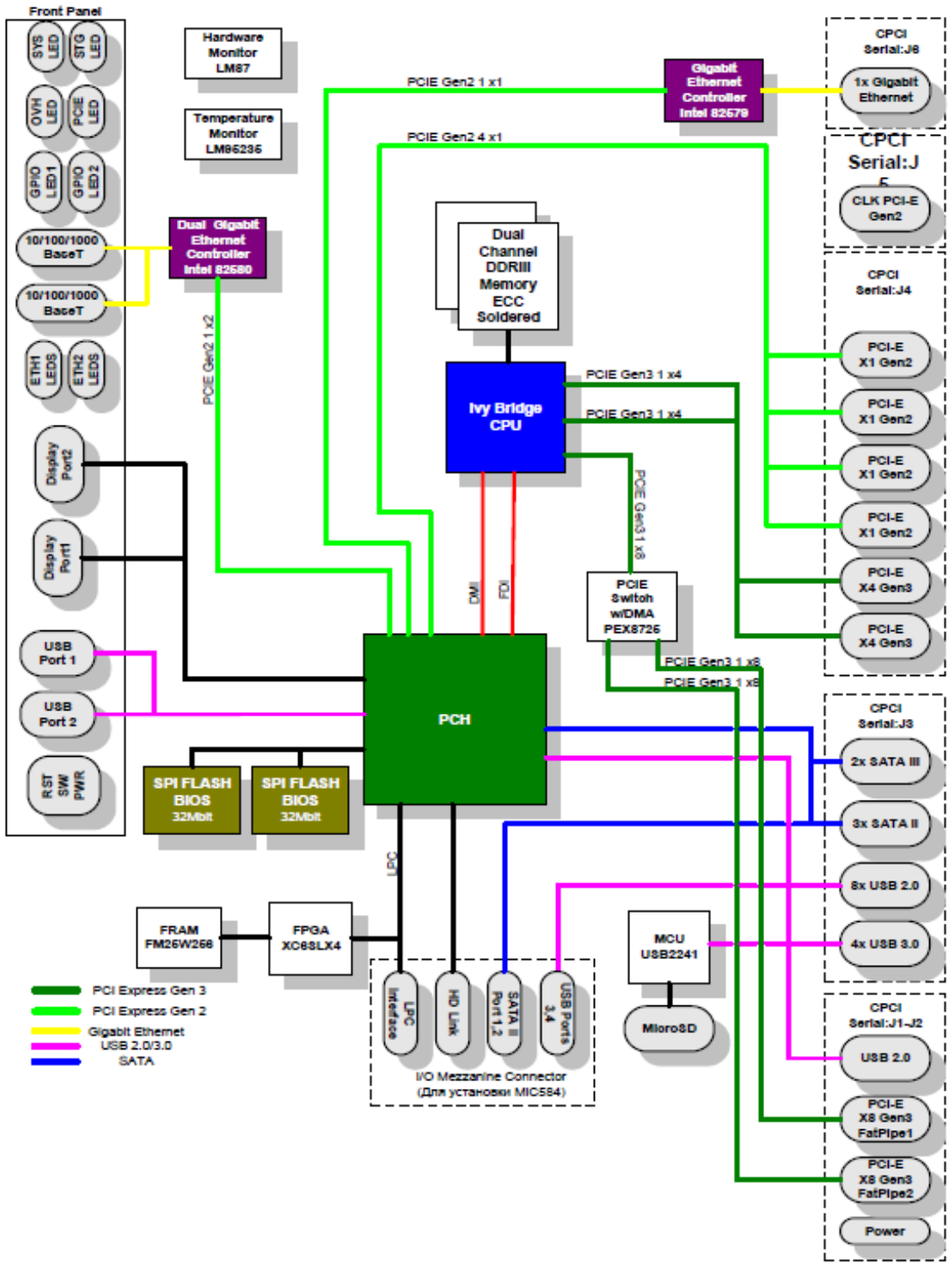


Fig. 2-1: Block diagram of CPC512/ CPC512RC

2.2 Specifics of functional nodes operation

- **Intel IvyBridge CPU.**

32-bit Intel CPU on the improved Nehalem core with 2 or 4 cores and 22 nm technology node. This CPU is highly-integrated solution, combining several CPU cores and a two-channel controller SDRAM/DDR3L with support of ECC memory and graphics adapter with 3D/2D acceleration. The microprocessor is aimed at the embedded systems market and is implemented in BGA. enclosure

- **Panther Point PCH.**

Highly-integrated interface controller that includes a standard periphery of IBM PC AT platform.

- **MEMORY.**

The board could have up to 8 GB DDR3L SDRAM 1066, 1333 MHz soldered on it. Installation of the memory extension module is not ptovided.

- **BIOS.**

For storage of BIOS two Flash 32 Mbit microchips on SPI bus are used.

- **RTC, CMOS.**

Real-time clock are integrated into PCH. Working capacity of the clock while the power is off is ensured by lithium battery, installed on module's board. BIOS Setup configuration is stored in FRAM.

- **FRAM FM25W256.**

Nonvolatile memory 256 Kb can be used for saving user data and storing BIOS SETUP configuration.

- **MicroSD. USB2241 bridge.**

The module has MicroSD interfaces connected to USB 2.0 port.

- **Ethernet controller Intel 82580.**

The module has two integrated Gigabit Ethernet interfaces. Two ports are routed to the front panel connectors. The interfaces are implemented on a high-speed Intel server controller.

- **Ethernet controller Intel 82579.**

Additionally the module is equipped with Gigabit Ethernet interface, implemented on PCH+PHY Intel 82579. Interface is routed to J6 CPCI Serial connector. The specified Gigabit Ethernet controller supports the AMT technology, which makes it possible to monitor and control of module's parameters, which functionally corresponds to IPMI.

- **USB 2.0.**

The module has 13x channels USB 1.1 (12 Mb/sec), USB 2.0:

  - Two of them are routed to USB connectors (type A) of the front panel,
  - eight interfaces are routed to CPCI Serial connectors,
  - two interfaces are routed to mezzanine connector,
  - 1x USB2.0 port is used for implementation of MicroSD interface.

- **USB 3.0.**

The module has 4x channels USB 3.0. They are routed to CPCI Serial connectors. When installing the module into peripheral slot, the USB interface routed to J1 connector, is switched off automatically.

- **SATA II.**

Two interfaces for the connection of drives are routed to mezzanine connector and J3 CPCI Serial connector. In this case the interface routed to J3 CPCI Serial connector can be automatically switched to the mezzanine connector when installing the module into peripheral slot or forcefully switched from BIOS Setup menu. Therefore, the mezzanine can be used for routing simultaneously up to 2x SATA II interfaces.

- **SATA III.**

Two interfaces for connection of drives are routed to J3 CPCI Serial connector.

- **Display Port.**

The ports are designed for the connection of digital monitor equipped with DisplayPort interface or for further conversion into other video standards. Supported maximum resolutions (2560x1600@60Hz).

Two ports are routed to the front panel of the module.

- **PCI-E x4 interface PCI-E lines of Ivy Bridge CPU.**

Two PCI-E Gen3 channels (8 Gb/sec) x4 are routed to the J4 CPCI Serial connector. They enable to connect 3U Compact PCI Serial extension modules with a set of links x1, x2, x4.

- **PCI-E x8 interface (FAT Pipe). PCI-E Switch PLX8725.**

Two channels PCI-E Gen3 x8 are routed to the J1 and J2 CPCI Serial connector. They enable connection of Compact PCI Serial extension modules with a set of links x1, x2, x4, x8 (8 Gb/sec). Support of the NON-Transparent mode (for FatPipe#1 port) in order to implement multiprocessor mode. Support of DMA mode for building HPC systems.

- **4x channel PCI-E interface. PCH Host.**

4x channels PCI-E Gen2 x1 are routed to J4 CPCI Serial connector.

- **SPI.**

The interface is implemented in FPGA on LPC bus. FRAM is supported (located on the board). Maximum clock frequency – 20 MHz.

- **Audio (except for CPC512RC and IMES.421459.512-03).**

Support can be implemented via MIC584 mezzanine board (I/O extension mezzanine board).

- **Watchdog.**

Hardware reset timer is implemented in FPGA on LPC bus.

- **Power supply reset and monitoring.**

CPU reset signal is generated from the following sources:

- from supervisor at power on.
- from the “Reset” button of Utility connector of the backplane
- from the button on the ejector handle of CPU (only for the CPC512 version).
- from watchdog timer.
- from Reset# signal of PCI bus (in the Slave mode).

- **Switches (jumpers).**

The module is equipped with switches of the following functionalities (see pargraph 5):

- BIOS Setup reset to the default settings.
- Peripheral Root mode.

- **Indication.**

LEDs for start diagnostics, drives activities, as well as programmable by the user, are routed to the front panel. Description of LEDs is given in subparagraph 2.6.

2.3 System extension capabilities

For connection peripheral devices to the module, particularly video/ audio interfaces and serial ports, interface modules are used: MIC584 mezzanine boards (I/O extension mezzanine board - available for all the modules, except for CPC512RC and IMES.421459.512-03), KIC550 or KIC550RC interface modules for extension of functional capabilities of the CPU module, see Table 2-1.

MIC584 contains the following set of interfaces:

- 2xUSB 2.0
- 2xSATA
- Audio IN/OUT/MIC
- 4xRS-232
- 2xRS-485
- LPT
- PS/2 keyboard+mouse

KIC550/KIC550RC module contains the following set of interfaces:

- 1xUSB 2.0/3.0
- 2.5” SATA HDD interface
- CFast interface

RIO510/RIO510RC contains the following set of interfaces:

- 1xUSB 2.0/3.0
- CFast interface
- miniPCIe interface
- mSATA interface
- external SATA interface

Table 2-1.: Interface modules used for the extension of I/O capabilities of CPC512

Notation Conventions	Description	Connector
MIC584	Mezzanine extension module (description is given in the User Manual IMES.421459.584 UM).	XS6 connector
KIC550	Interface module for the extension of CPC Module functional capabilities (description is given in the User Manual IMES.421459.550 UM).	Compact PCI Serial connector
RIO510	Rear module - drives adapter.	Compact PCI Serial RIO

Table 2-2.: Interface modules used for extension of I/O capabilities of CPC512RC

Notation Conventions	Description	Connector
KIC550RC	Interface module for the extension of CPC Module functional capabilities (description is given in the User Manual IMES.421459.550 UM).	Compact PCI Serial connector
RIO510RC	Rear module - drives adapter.	Compact PCI Serial RIO connector

2.4 Peripheral devices

CPC512/CPC512RC module is equipped with the following peripheral devices:

2.4.1 Timers

CPC512/CPC512RC is equipped with several types of timers:

- **RTC - Real-Time Clock**

PCH contains real-time clock compatible with MC146818A with 256 bytes of CMOS memory, powered from the battery. Their functions are: timekeeping, alarm-clock function, programmable functional of intermittent interruption delivery and calendar for 100 years.

- **Counter / Timer**

As with PC/AT, the module as three counters/timers of 8254 type, integrated into PCH.

- **Additional timer**

PCH includes an additional programmable timer, which prevents system blocking during its startup process. During the first timer overflow, SMI# signal is generated, which calls a subprogram that makes it possible to end the program hangup process. In case of timer overflow for the second time, system Reset signal is obtained which enables to end the system hardware hangup process.

- **Watchdog Timer**

The watchdog timer is designed for eliminating system blocking both in case of system startup and during operation. When the watchdog timer triggers, Reset signal, interrupt or SMI are generated. Actuation time is set via BIOS Setup menu. At the time of system startup, the watchdog monitors execution of BIOS code.

The watchdog is implemented in FPGA as a device on LPC bus. Timer contains 24-bit counter register [Timer Current Value Register], decremented with the frequency of 32768 kHz and start value register [Timer Initial Value Register]. At resetting the counter register either interrupt or NMI, or automatic board reset are generated. Actuation time can be set from 0 through 512 seconds with a pitch of 30,52 µs.

By default and without preliminary initialization, the actuation delay time of the watchdog timer is at the maximum value and amounts to 512 seconds. Below is the formula for calculation of actuation delay duration T_{WD} (μs) depending on the decimal value in the register Timer Initial Value Register (K_{WD}):

$$T_{WD}\,[\mu s] = K_{WD} * 10^6 / 2^{15}$$

E.g. the decimal value K_{WD} = 1 (000001h) corresponds to actuation delay time of 30.52 μs, and the value K_{WD} = 16777215 (FFFFFFh) – to the delay time of 512 seconds.

Counter reset to initial value can be performed in several ways:

- By writing any number into the counter register [Timer Current Value Register]
- By writing any number into the 80h port (the mode is switched in [Timer Init Register])
- By writing or reading via addresses in two windows (base addresses of windows are specified in the relevant registers [Window Base Address], address mask is specified in the register [Windows 1&2 Address mask register], the mode is selected in [Timer Init Register]). Size of the windows is from 1 to 16 bytes, depending on the value in the mask register.

Access to watchdog timer registers

Device configuration is based on Plug-and-Play architecture. The watchdog timer registers can be accessible via standard I/O registers (of index and data), when entering to the configuration mode.

CONFIG PORT	302h	Write
INDEX PORT	302h	Read/Write
DATA PORT	303h	Read/Write

Configuration mode

The device enters the configuration mode, when the following configuration key is written to the CONFIG PORT:

Configuration key = <46h> <57h>

The device exits the configuration mode, when the following configuration port is written into the CONFIG PORT:

Configuration key = <57h> <46h>

INDEX and DATA ports are available only in the configuration mode.

Device programming

Sequence of actions during programming of the device:

- Enter configuration mode:

```
MOV   DX, 302H
MOV   AL, 46H
OUT   DX, AL
MOV   AL, 57H
OUT   DX, AL
```

- Write to LDN register the number of logical device

(watchdog timer has a logical number 1):

```
MOV   DX, 302H
```

```
MOV   AL, 7
OUT   DX, AL
MOV   DX, 303H
MOV   AL, 1
OUT   DX, AL
```

- Watchdog timer registers are available for writing and reading. E.g. reading the status register 3eh and writing back of its value:

```
MOV   DX, 302H
MOV   AL, 3EH
OUT   DX, AL
MOV   DX, 303H
IN    AL, DX
OUT   DX, AL
```

- Exit configuration mode:

```
MOV   DX, 302H
MOV   AL, 57H
OUT   DX, AL
MOV   AL, 46H
OUT   DX, AL
```

Global configuration registers

INDEX	Type	HARD RESET	Configuration register
7h	R/W	01h	Logical Device Number

Logical Device Number register (index 7h)

Index = 7h		
Bit	**Name**	**Description**
7:0	LDN	Write/Read: Writing to this register selects a logical device

Configuration registers of logical device 1 (WDT)

INDEX	Input/output address	Type	HARD RESET	Configuration register
30h	-	R/W		Activate
38h	Base+0	R/W		Timer current value [7:0]
39h	Base+1	R/W		Timer current value [15:8]
3ah	Base+2	R/W		Timer current value [23:16]
3bh	Base+3	R/W	00h	Timer initial value [7:0]
3ch	Base+4	R/W	40h	Timer initial value [15:8]
3dh	Base+5	R/W	00h	Timer initial value [23:16]
3eh	Base+6	R/W	00h	Status register
3fh	Base+7	R/W	03h	Control register
60h	-	R/W		Base[15:8] - I/O port base address bits[15:8]

61h	-	R/W		Base[7:3] - I/O port base address bits[7:3] Base[2:0] – should be 0;
70h	-	R/W	00h	Primary interrupt select
F0h	-	R/W	00h	Reserved
F1h	-	R/W	00h	Timer Init Register
F2h	-	R/W	00h	Window 1 base address bits[7:0]
F3h	-	R/W	00h	Window 1 base address bits[15:8]
F4h	-	R/W	00h	Window 2 base address bits[7:0]
F5h	-	R/W	00h	Window 2 base address bits[15:8]
F6h	-	R/W	FFh	Window 1 Mask bits [7:4] Window 2 Mask bits [3:0]

Activate register

Index = 30h		
Bit	**Name**	**Description**
7:1	-	Not used
0	Activate	Write/Read: 1 – This logical device is switched on 0 – This logical device is switched off

I/O port base address registers

Index = 60h		
Bit	**Name**	**Description**
7:0	I/O_Base_Adress[15:8]	Write/Read: Bits 15:8 of the basic address of the current logical device
Index = 61h		
Bit	**Name**	**Description**
7:0	I/O_Base_Adress[7:0]	Write/Read: Bits 7:0 of the basic address of the current logical device

Primary interrupt select register (index 70h)

Index = 70h		
Bit	**Name**	**Description**
7:4	-	Not used
3:0	Interrupt_select	Write/Read: 00h – interrupt is switched off 01h – IRQ1 02h – SMI 03h – IRQ3 04h – IRQ4 05h – IRQ5 06h – IRQ6 07h – IRQ7 08h – IRQ8 – (interrupt is switched off) 09h – IRQ9 0ah – IRQ10 0bh – IRQ11 0ch – IRQ12 0dh – IRQ13 (interrupt is switched off) 0eh – IRQ14 (interrupt is switched off) 0fh – IRQ15 (interrupt is switched off)

Timer Init register

Index = F1h		
Bit	**Name**	**Description**
7:5	-	Not used
4	P80E	Write/Read: counter reset when writing to port 80h 1 - is switched on 0 –switched off
3	WND2_WR_EN	Write/Read counter reset at writing cycle to window 2 1 – is switched on 0 – switched off
2	WND2_RD_EN	Write/Read counter reset at reading cycle to window 2 1 – is switched on 0 – switched off
1	WND1_WR_EN	Write/Read counter reset at writing cycle to window 1 1 – is switched on 0 – switched off
0	WND1_RD_EN	Write/Read: counter reset at reading cycle from window 1 1 – is switched on 0 - is OFF

Window 1 port base address registers

Index = F2h		
Bit	**Name**	**Description**
7:0	Window1_Base_Adress[7:0]	Write/Read: Bits 7:0 of the basic address of window 1
Index = F3h		
Bit	**Name**	**Description**
7:0	Window1_Base_Adress[15:8]	Write/Read: Bits 15:8 of the basic address of window 1

Window 2 port base address registers

Index = F4h		
Bit	**Name**	**Description**
7:0	Window2_Base_Adress[7:0]	Write/Read: Bits 7:0 of the basic address of window 2
Index = F5h		
Bit	**Name**	**Description**
7:0	Window2_Base_Adress[15:8]	Write/Read: Bits 15:8 of the basic address of window 2

Windows 1&2 address mask register

Index = F6h		
Bit	**Name**	**Description**
7:4	Window1_MASK[3:0]	Write/Read: Bits 3:0 of window address mask 1
3:0	Window2_MASK[3:0]	Write/Read: Bits 3:0 of window address mask 2

Description of WDT I/O registers of controller

Timer Current Value Register [23:0]

Base+0h		
Bit	**Name**	**Description**
7:0	Timer_Current_Value[7:0]	Write/Read: Bits 7:0 of the current counter value
Base+1h		
Bit	**Name**	**Description**
7:0	Timer_Current_Value[15:8]	Write/Read: Bits 15:8 of the current counter value
Base+2h		
Bit	**Name**	**Description**
7:0	Timer_Current_Value[23:16]	Write/Read: Bits 23:16 of the current counter value

Timer Initial Value Register [23:0]

Base+3h		
Bit	**Name**	**Description**
7:0	Timer_Initial_Value[7:0]	Write/Read: Bits 7:0 of initial counter value
Base+4h		
Bit	**Name**	**Description**
7:0	Timer_Initial_Value[15:8]	Write/Read: Bits 15:8 of initial counter value
Base+5h		
Bit	**Name**	**Description**
7:0	Timer_Initial_Value[23:16]	Write/Read: Bits 23:16 of initial counter value

Status Register

Base+6h		
Bit	**Name**	**Description**
7:3	-	Reserved
2	STM	Write/Read: Second timeout flag Is installed in the "1" under condition of TMF=1 and RSTE=1. Is reset by writing "1" this bit.
1	SME	Read: File of SMI timeout generation. Installed into "1" if SMI mode is selected in the interrupt register (index 70h).
0	TMF	Write/Read: Timeout flag. Installed into "1" when resetting the timer counter. This flag is used for interrupt generation. Is reset by writing "1" to this bit or writing to the port 80h or by addressing to windows 1 and 2 (in case of activation of these modes).

Control Register

Base+7h		
Bit	**Name**	**Description**
7:2	-	Reserved
1	CNTE	Write/Read: Counter 1 decrement is ON 0 - is OFF
0	RSTE	Write/Read: Board reset on timeout 1 – Reset is permitted 0 – Reset is prohibited

2.4.2 Battery

In CPC512/CPC512RC one 3.0 V lithium battery is used for power supply of real-time clock. Use RENATA CR2032 or compatible models (see 4.4.3 Battery replacement). Module operation without battery is possible; without power supply battery, data derived from the real-time clock can be unreliable.

2.4.3 Devices on local SMBus

CPC512/CPC512RC module has SMBus (System Management Bus) that ensures monitoring and system configuration functions. This bus uses two-wire I2C™ interface, it has several serial access devices connected to it (microchips of LM87 temperature monitor, EEPROM memory, clock-generation unit).

Table 2-3.: Addresses of devices on SMBus

No	SMB address	Device
1	0D2H	SLG8SP533V clock generator
2	0A0H and 0A2H	SPD EEPROM memory module
3	5CH	LM87 (PCB & CPU Sensor) temperature monitor
4	4CH	LM95235 temperature monitor (RAM Sensor)

Two temperature monitors control the temperature of the processor chip and memory chip temperature. Upon request, the temperature monitor can provide information to the software means of control of the current system state, this ensures module operation in the safe temperature mode.

2.4.4 Non-volatile memory

2.4.4.1 MicroSD card

The board has an installed XS10 connector for cards of MicroSDHC type (see Fig 1-7 Location of main components of CPC512 (bottom view) and subparagraph 2.5.10 Connector for MicroSD card). MicroSD interface is transmitted to the internal USB 2.0 port.

2.4.4.2 High-speed memory for saving user data (FRAM)

The board is equipped with a nonvolatile rapid-access serial memory FRAM (32 KB) for the storage of service information: 1 KB, used by manufacturer and 31 KB for user's critical data.

Registers and programming of FRAM device are described below.

2.2.4.2.1. FRAM registers (logic device 3)

INDEX	Input/output address	Type	HARD RESET	Configuration register
30h	-	R/W		Activate
	Base+0	R/W	00h	FRAM address value [7:0]
	Base+1	R/W	00h	FRAM address value [14:8]
	Base+2	R/W	00h	FRAM data value [7:0]
	Base+3	R/W	00h	FRAM Control register [7:1] – reserved [0] – autoincrement mode
60h	-	R/W		Base[15:8] - I/O port base address bits[15:8]
61h	-	R/W		Base[7:3] - I/O port base address bits[7:3] Base[2:0] - should be 0;

For working with FRAM it is required to set a base address of the device and activate it (LDN=3) similarly to the watchdog timer. Further operation with FRAM is carried out in the I/O area with regard to the set base address. Bit <0> in the control register (Base+3) activates the address automatic increase mode during read/write of data register (base+2).

2.2.4.2.2. Programming of FRAM device

Sequence of action at system initializing:

- Enter the configuration mode

```
MOV   DX, 302H
MOV   AL, 46H
OUT   DX, AL
MOV   AL, 57H
OUT   DX, AL
```

- Writing to LDN register the number of logical deivce (FRAM has a logical number 3)

```
MOV   DX, 302H
MOV   AL, 7
OUT   DX, AL
MOV   DX, 303H
MOV   AL, 3
OUT   DX, AL
```

- Set the base address of the device in the I/O field (for example 310h):

```
MOV   DX, 302H
MOV   AL, 60H
OUT   DX, AL
MOV   DX, 303H
MOV   AL, 3H
OUT   DX, AL
```

```
MOV   DX, 302H
MOV   AL, 61H
OUT   DX, AL
MOV   DX, 303H
MOV   AL, 10H
OUT   DX, AL
```

- Activate the device:

```
MOV   DX, 302H
MOV   AL, 30H
OUT   DX, AL
MOV   DX, 303H
MOV   AL, 1H
OUT   DX, AL
```

- Exit configuration mode:

```
MOV   DX, 302H
MOV   AL, 57H
OUT   DX, AL
MOV   AL, 46H
OUT   DX, AL
```

Further work with FRAM is carried out in the I/O field using 310h-313h addresses.

- Writing data byte (32h) to FRAM at the address (144h)

```
MOV   DX, 310H
MOV   AL, 44H
OUT   DX, AL
MOV   DX, 311H
MOV   AL, 01H
OUT   DX, AL
MOV   DX, 312h
MOV   AL, 32h
OUT   DX,AL
```

- Reading data byte from FRAM at the address (101h)

```
MOV   DX, 310H
MOV   AL, 01H
OUT   DX, AL
MOV   DX, 311H
MOV   AL, 01H
OUT   DX, AL
MOV   DX, 312h
IN    AL,DX
```

2.5 Module interfaces

2.5.1 CompactPCI Serial connectors

CPC512/CPC512RC module is designed in accordance with the CompactPCI Serial bus architecture. The module uses six connectors of CompactPCI Serial interface (see Рис. 1-2 - Fig. 1-4 and Fig. 1-12).

2.5.2 Connector for mezzanine module

For connection of peripheral devices to the module, interface modules are used, see Table 2-1. Mezzanine module MIC584 is connected from the right from CPC512 CPU module to XS6 connector on the top side of CPC512 (Connector Socket High Speed, 60 pin), see Fig. 1-6: Location of main components on CPC512 board (top view) and Fig. 2-2. Description of MIC584 module is given in the User Manual for IMES.421459.584 UM.

Warning!

MIC584 module can't be used together with CPC512RC modules and CPC512 modules, equipped with R1 copper heatsink of enhanced area (IMES.421459.512-03).

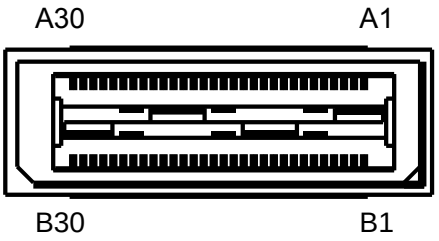


Fig. 2-2: XS6 connector for installation of MIC584 mezzanine module (not available on CPC512RC and IMES.421459.512-03)

Table 2-4.: Purpose of contacts of XS6 connector for installation of MIC584 mezzanine module

Contact	Purpose	Contact	Purpose
A1	+5V	B1	+5V
A2	+5V	B2	+5V
A3	USB_PN0	B3	USB_PN1
A4	USB_PP0	B4	USB_PP1
A5	GND	B5	GND
A6	SATA_TXN0	B6	SATA_RXN0
A7	SATA_TXP0	B7	SATA_RXP0
A8	GND	B8	GND
A9	SATA_TXN1	B9	SATA_RXN1
A10	SATA_TXP1	B10	SATA_RXP1
A11	GND	B11	GND
A12	AZ_BITCLK	B12	LPC_AD0
A13	GND	B13	LPC_AD1
A14	AZ_SYNC	B14	LPC_AD2
A15	AZ_RST#	B15	LPC_AD3
A16	AZ_SDIN	B16	LPC_FRAME#
A17	AZ_SDOUT	B17	GND
A18	+3.3V	B18	SERIRQ
A19	KBRST#	B19	+3.3V
A20	A20GATE	B20	DRQ0#
A21	+3.3V	B21	+3.3V
A22	PLT_RST#	B22	SMB_CLK
A23	GND	B23	SMB_DATA
A24	CLK_33MHZ	B24	GND
A25	GND	B25	USB_OC#0
A26	CLK_14MHZ	B26	USB_OC#1
A27	GND	B27	+3.3VA
A28	CLK_32KHZ	B28	INIT_3V3
A29	GND	B29	BIOS_DIS#
A30	+5VA	B30	+5VA

2.5.3 Keyboard / mouse interface

CPC512 makes it possible to connect keyboard/mouse via USB port on the front panel. In addition to it, PS/2 keyboard/mouse interface is implemented on MIC584 mezzanine via LPC interface and is available through the MIC584 extension module (see description of MIC584 in the User Manual for IMES.421459.584 UM). Connector for keyboard and mouse (PS/2 6-contact MiniDIN) is located on the front panel of MIC584 module.

CPC512 module emulation program of keyboard controller, software-compatible with 8042, implemented on FPGA. This is required for proper and correct operation of the supported operating systems when CPC512 is used without MIC584.

2.5.4 USB interfaces

CPC512/CPC512RC is equipped with the following USB ports:

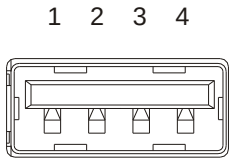
- 13 ports USB 1.1 (12 Mb/sec), USB 2.0 (480 Mb/sec) and 4x ports USB 3.0 (4.8 Gb/sec).
- 2x USB2.0 ports are routed to the front panel connectors
- 2x USB2.0 ports are routed to mezzanine connector.
- 8x USB2.0 ports are routed to CPCI Serial connector.
- 1x USB2.0 port is used for implementation of MicroSD interface.
- 4x USB3.0* ports are routed to CPCI Serial connectors.

** When using USB 3.0 ports, four USB 2.0 ports are utilized by USB 3.0 ports.*

The ports support high-speed, full-speed, and low-speed modes. USB 2.0 in the high-speed mode enables to transfer data with the rate up to 480 Mb/sec, this is 40 times faster than in the full-speed mode (USB 1.1).

Each port allows connecting one USB peripheral device. In order to connect more devices to the module, it is required to use external concentrator.

USB power supply source is protected by an automatic fuse for 500 mA.



The front panel is equipped with two standard USB 2.0 connectors of type A: USB1 и USB2

Fig. 2-3: USB1 and USB2 connectors

Table 2-5.: Purpose of contacts of USB1 and USB2 connectors on the front panel of CPC512/CPC512RC

Contact number	Purpose	Function
1	VCC	VCC signal
2	UV0-	Differential USB-
3	UV0+	Differential USB+
4	GND	GND signal

2.5.5 DisplayPort

DisplayPort connector on the front panel of CPC512/CPC512RC (see Fig. 1-11, Fig. 1-14) is designed for the connection of digital monitors with resolution up to 2560x1600@60 Hz. The output also enables connecting DVI-D monitors via a passive adapter.

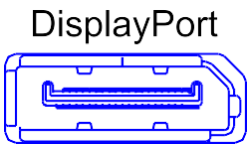


Fig. 2-4: DisplayPort connector

Table 2-6.: Purpose of DisplayPort connector contacts

Contact	Purpose
1	LANE0+
2	GND
3	LANE0-
4	LANE1+
5	GND
6	LANE1-
7	LANE2+
8	GND
9	LANE2-
10	LANE3+
11	GND
12	LANE3-
13	AUX_EN#
14	CONFIG2
15	AUX+
16	GND
17	AUX-
18	HP_DETECT
19	GND
20	+3.3V

2.5.6 Serial interfaces (RS-232 and RS-485)

The serial interfaces (implemented via LPC interface) are available only when MIC584 mezzanine module is sued (see the description of MIC584 in the User Manual IMES.421459.584 UM). MIC584 has six serial ports:

- COM1 (RS232) interface, 9-pin connector D-Sub on the front panel of MIC584 module;
- COM2-COM4 interfaces (RS232) are routed to 10-pin double-row connectors (IDC2-10) XP11-XP13 of MIC584 module;
- COM5, COM6 interfaces (RS485) are routed to 10-pin double-row connector (IDC2-10) XP7 of MIC584 module.

The serial ports are fully compatible with 16C550 controller and include a full set of modem coordination and control signals, support generation of masked interrupts and transfer of data at the rate of up to 460,8 Kb/sec.

2.5.7 Parallel port interface

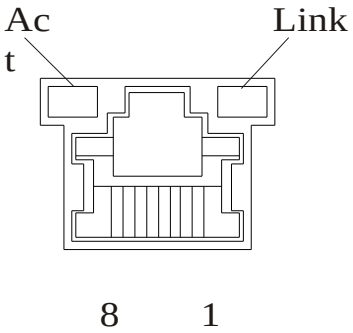
Standard parallel interface (IEEE1284, ECP/EPP/SPP) is implemented on MIC584 mezzanine through LPC interface and is available only via MIC584 mezzanine extension module (see the description of MIC584 in the User Manual IMES.421459.584 UM).

2.5.8 Gigabit Ethernet external interface

The module has two ports 10Base-T/100Base-TX/1000Base-T Ethernet based on a high-speed Intel® 82580 server controller. Controller's architecture is optimized to achieve high performance at minimum power consumption. The controller is connected to the system via high-performance PCI-E bus. Intel® 82580 architecture includes independent receive and transmit queues to limit the traffic over PCI-E bus, as well as PCI-E interface, maximizing the use of packets for efficient bus load.

RJ45 Gigabit Ethernet connectors are located on the front panel of CPC512/CPC512RC and are marked as XS5.

The interfaces ensure automatic determination of transfer rate and switching between data transfer modes 10Base-T, 100Base-TX and 1000Base-T.



The front panel of CPC512/CPC512RC is equipped with two Gigabit Ethernet ports.

Fig. 2-5: External view of RJ45 Ethernet connector

2.5.8.1 Purpose of RJ45 connector contacts

RJ45 connectors enable the use of 10Base-T, 100Base-TX and1000Base-T interfaces from the front panel.

Table 2-7.: Purpose of contacts of RJ45 Gigabit Ethernet connectors

Contact	MDI / Standard Ethernet cable					
	10Base-T		100Base-TX		1000Base-T	
	I/O	Signal	I/O	Signal	I/O	Signal
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX–	O	TX–	I/O	BI_DA–
3	I	RX+	I	RX+	I/O	BI_DB+
4	–	–	–	–	I/O	BI_DC+
5	–	–	–	–	I/O	BI_DC–
6	I	RX–	I	RX–	I/O	BI_DB–
7	–	–	–	–	I/O	BI_DD+
8	–	–	–	–	I/O	BI_DD–

2.5.8.2 LEDs for channel state of external Ethernet interface

Green LED "Line" is on if the line is connected.

Green LED "Act" (Activity) is on, if computer obtains or sends packets via RJ45 connector.

2.5.9 Gigabit Ethernet interface of backplane

CPC512/CPC512RC has an additional 10Base-T/100Base-TX/1000Base-T Ethernet interface on the basis of PCH QM77 Gigabit Ethernet controller integrated into the microchip and external PHY Intel 82579L.

The controller ensures operation in two modes: 10/100/1000 Mb/sec mode and control mode.

In the 10/100/1000 Mb/sec mode (only for S0 system state) controller ensures high-speed Ethernet-interface with initial PCI Express interface and support of the complete mapping in memory or input/output area with 64-bit addressing for systems with physical memory volume, exceeding 4 GB, as well as Direct Memory Access (DMA) mechanism that makes it possible to carry out high-speed data transfer.

The controller is also equipped with two large adjustable transmit and receive FIFO buffer (up to 20 KB each). This enables using an integrated network controller for data transmission with minimum interval between frames (IFS).

Local network controller can operate at several speeds (10/100/1000 Mb/sec) in duplex or half-duplex mode. In the full-duplex mode, network controller operates in accordance with the Specification for flow control of IEEE 802.3x.

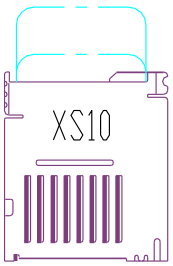
In the control mode (supported for all the Sx states of the system) controller communicates via Ethernet interface at a speed of up to 10 Mb/sec. SMBus will be the primary interface in this case. In this mode, connection is used exclusively for system control. In this case, controller can be supplied with power from a standby power supply source +5 V_standby. Therefore, it is possible to control the system activation remotely from S3-S5 state over Ethernet channel.

2.5.9.1 LEDs for state of Gigabit Ethernet channel of backplane

Two-color orange-yellow LED "BE" (Backplane Ethernet), routed to the front panel is on with green light during transferring data at the sped of 1 Gb/sec or orange light during data transfer at the speed of 100 Mb/sec. During operaion at the speed of 10 Mb/sec, "BE" LED is not activated.

2.5.10 Connector for MicroSD card

CPC512/CPC512RC is equipped with XS10 connector that supports MicroSDHC cards. MicroSD interface is transmitted to the internal USB 2.0 port. MicroSDHC card has a volume up to 32 GB. External view of MicroSD connector with the installed memory card is given below.



MicroSD connector with the installed memory card

Fig. 2-6: External view of MicroSD connector

Warning!

MicroSDHC card installed into the XS10 connector should be designed for operation in the temperature range similar to the one of CPC512/CPC512RC module. Otherwise, proper operation of the module in the temperature range, stated in the technical specifications, shall not be guaranteed.

2.5.11 SATA interface

- **SATA interface:**
  - Support of RAID 0, 1, 5, 10.
  - **SATA II interface:**
    - Two interfaces for connection of drives are routed to the mezzanine connector and J3 CPCI Serial connector.
    - In this case the interface routed to J3 CPCI Serial connector, can be automatically switched to the mezzanine connector when installing the module into peripheral slot or forcefully switched from BIOS Setup menu. Therefore, the mezzanine can be used for routing simultaneously up to 2x SATA II interfaces.

  - **SATA III interface:**
    - Two interfaces for connection of drives are routed to J3 CPCI Serial connector.

It should be noted that Fastwel Group manufactures two versions of MIC584: MIC584-01 and MIC584-02, and both of these versions are compatible with CPC512. MIC584-01 version is equipped with SATA connectors. If user MIC584-02 mezzanine module to CPC512, the CPC512 board will properly operate with MIC584-02, except for two SATA channels that will not be implemented. Detailed description of MIC584 module is given in the User Manual for IMES.421459.584 UM.

2.5.12 HD (high definition) audio (except for CPC512RC and IMES.421459.512-03)

Audio interface is implemented on MIC584 mezzanine:

- linear input/output;
- output to headphones;
- microphone input.

More detailed information on Audio interface is given in the User Manual for MIC584 IMES.421459.584 UM.

2.6 LEDs

The front panel of CPC512/CPC512RC has LEDs, described in the table below:

Table 2-8.: Identification and functions of CPC512 LEDs

No	Mnemonics	Description
1	SYS	Two-color red-blue. Blue – "Power Off" mode. Red – hardware failure. Flashing of red LED serves diagnostics purposes and is also a sign of malfunction.
2	BE	Two-color red-green (used as orange-green). Indicates data transfer over backplane Ethernet channel. Green – data transfer at the speed of 1 Gb/sec, orange – at the speed of 100 Mb/sec.
3	STG	Red – activity of SATA and microSD drives.
4	GP	Two-color red-green. Red – programmable. Green – programmable. At start, the green LED indicates the state of launching process.
5	PE	Two-color red-green. Red – communication error over PCI Express interface. Green steady – indicates a connection over PCI Express interface. Green flashing – indicates that a connection over PCI Express is implemented with limitations. Orange glow of the LED indicates that the module operates in the Peripheral Root mode.
6	OVH	Two-color red-green. Red – overheating of CPU, memory and PCH. Orange glow - overheating of CPU, memory and PCH before critical point (borderline state).

Alarm system is supported according to the SFF-8485 specification.

2.6.1 Registers for configuration and control of GP LED (logic device 5)

Table 2-9.: Registers of configuration and control of GP indicator

INDEX	Input/output address	Type	HARD RESET	Configuration register
30h	-	R/W	00h	Activate. Bit [0] in "1" -LED module is active.
-	Base+0	R/W	01h	LED data value [3:0] The rest bits are not important and are read as "0".
60h	-	R/W	-	Base[15:8] - I/O port base address bits[15:8]
61h	-	R/W	-	Base[7:0] - I/O port base address bits[7:0]

For working with GP indicator it is required to set a base address of the device and activate it (LDN=5) similarly to the watchdog timer or FRAM module. Control of GP indicator operation is carried out via LED register. Modification of the LED register is carried out in the I/O area with regard to the set base address.

2.6.2 Initialization of LED register

Sequence of action at system initialization:

- Enter the configuration mode

```
MOV   DX, 302H
MOV   AL, 46H
OUT   DX, AL
MOV   AL, 57H
OUT   DX, AL
```

- Write to LDN register the number of logical device
  (watchdog timer has a logical number 5)

```
MOV   DX, 302H
MOV   AL, 7
OUT   DX, AL
MOV   DX, 303H
MOV   AL, 5
OUT   DX, AL
```

- Set the base address of the device in the I/O field (for example 31dh):

```
MOV   DX, 302H
MOV   AL, 60H
OUT   DX, AL
MOV   DX, 303H
MOV   AL, 3H
OUT   DX, AL
MOV   DX, 302H
MOV   AL, 61H
OUT   DX, AL
MOV   DX, 303H
MOV   AL, 1dH
OUT   DX, AL
```

- Activate the device:

```
MOV   DX, 302H
MOV   AL, 30H
OUT   DX, AL
MOV   DX, 303H
MOV   AL, 1H
OUT   DX, AL
```

- Exit configuration mode:

```
MOV   DX, 302H
MOV   AL, 57H
```

```
OUT   DX, AL
MOV   AL, 46H
OUT   DX, AL
```

2.6.2.1 Assigning separate bits of LED register

Assigning of separate bits of LED control register is specified in the table below:

Table 2-10.: Purpose of LED control register bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserve bits. To be read as "0".				GP red LED Bit1	GP red LED Bit0	GP green LED Bit1	GP green LED Bit0

GP indicator is a two-color LED and physically contains two independent red and green light emitting diodes. Therefore, green, red or orange color glow is available (red and green are turned on simultaneously) depending on combination of the activated diodes. An independent program control of each of the diodes is supported by the use of the LED register. Each LED state is described by two bits. The following combinations are supported:

Table 2-11.: Combination of control bits of GP indicator

Bit1	Bit0	State
0	0	LED is OFF
0	1	LED is flashing with a frequency of 8 hertz
1	0	LED is flashing with a frequency of 1 hertz
1	1	LED is flashing constantly

3 Use of CPC512/ CPC512RC

CPC512/CPC512RC module is designed for operation as part of Compact PCI Serial systems. The module corresponds to the specifications "CPCI-S.0 R1.0" [1] and "Compact PCI Plus IO R1.0" [2].

Let's consider options of building various systems based on CPC512/CPC512RC.

3.1 Compact PCI Serial system

3.1.1 Inter-modular connections

The Compact PCI Serial system enables implement all the advantages of Intel Core architecture both in terms of its computational power and in terms of high-speed intermodular connections.

According to the specification [1] for a standard 9-slot backplane, the system slot can support the following functionality of inter-modular connections:

- Up to 2x PCI Express x8 interfaces (Fat Pipe)
- Up to 6x PCI Express x4 interfaces
- Up to 8x USB 2.0/3.0 interfaces
- Up to 8x SATA interfaces
- Up to 8x Gigabit Ethernet interfaces

In this case, Gigabit Ethernet interface could have either a "Star" or "Full Mesh" connection types.

From among the mentioned interfaces, CPC512 supports:

- 2x PCI Express x8 Gen 3 interfaces (Fat Pipe) with support of DMA
- 2x PCI Express x4 Gen 3 interfaces – CPU lines
- 4x PCI Express x1 Gen 2 interfaces – PCH BD82QM77 lines
- 8x USB 2.0 interfaces
- 4x USB 3.0 interfaces
- 5x SATA interfaces
- 1x Gigabit Ethernet interface

Set of the supported interfaces makes it possible to create high-performance and compact systems with scaling capability. In addition, the lack of cable inter-modular and inter-instrument connections allows to improve reliability and maintainability.

Standard Compact PCI Serial system includes a single CPU module (host), to be installed into the system slot (System) of red color and a set of peripheral modules, to be installed into peripheral slots (Perip.). Implemented connection circuit of the "star" type

It should be noted that a number of available SATA and USB 3.0 interfaces for CPC512/CPC512RC is less than eight. Therefore, SATA interface is supported in slots from

8 to 4, and USB 3.0 interfaces - from 2 to 4 and in slot 8 (see Fig. 3-1). SATA interface of slot 4 can be software-switched (using system BIOS menu) for the use on MIC584 (for CPC512RC module, SATA interface of slot 4 is constantly connected). In this case, SATA interface will be supported in the slots from 8 to 5.

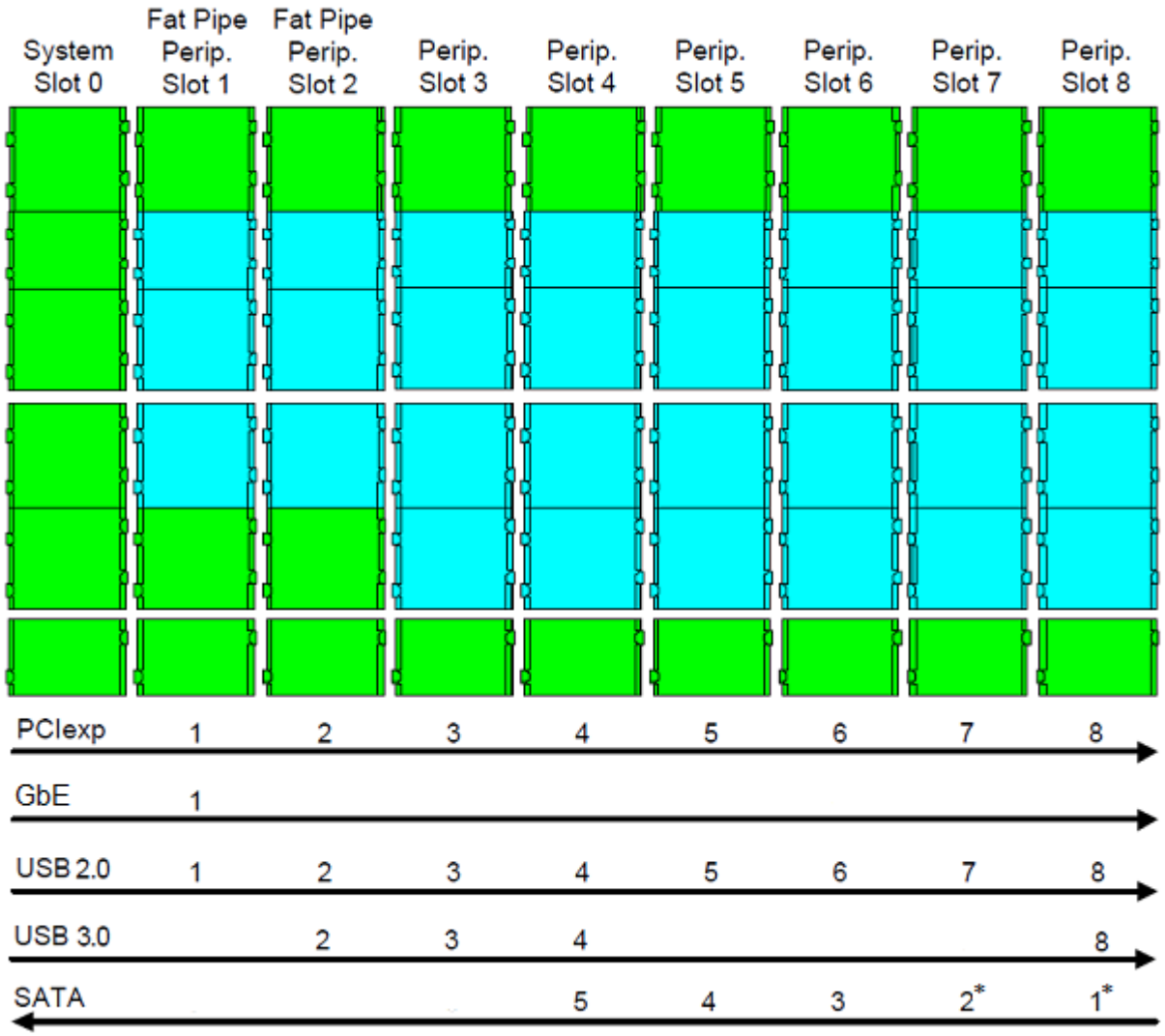


Fig. 3-1: Numbering of interfaces, supported by CPC512/CPC512RC module, on Compact PCI Serial backplane. Asterisks are used for marking SATA ports 6 Gb/sec (SATA III)

In general, the Gigabit Ethernet channel is designed for the use during operation of CPC512/CPC512RC in peripheral slot with Fastwel external Gigabit Ethernet switch of KIC551 or KIC551RC type for conduction version.

Apart from the operation as a system (host) module, CPC512/CPC512RC supports operation in peripheral slot as an endpoint device. PLX switch installed on board of PCI Express module enables to implement the NT-mode for one of the downstream ports (see Table. 5-1). This makes possible to "unbind" the CPU modules from each other over PCI Express connection. Connection of such type enables to build multiprocessor systems - clusters. In the standard 9-slot backplane, CPC512/CPC512RC CPU module being in the system slot, makes it possible to organize

operation of two CPC512/CPC512RC modules (or CPC510-01) with the connection over PCI Express x8 Gen3 bus (64 Gb/sec) (Gen2 for CPC510) with support of DMA and two CPC512/CPC512RC modules (or CPC510-01) with connection over PCI Express x4 Gen3 bus (32 Gb/sec) (Gen2 for CPC510). The rest four peripheral slots with PCI Express x1 Gen2 interfaces can be used for storage system (e.g. KIC550 or KIC550RC for conduction version) or for low-speed peripheral modules. Booting of operating system on peripheral CPU modules can be performed from both an integrated MicroSD memory card and via RIO connector of backplane connector where a rear I/O module RIO510 or RIO510RC for conduction version is available.

In case there is a need for a higher system performance, it is required to use configuration with external PCI Express switch of KIC551/KIC551RC type. In addition to fully support high-speed PCI Express Gen 3 and Gigabit Ethernet interfaces on a standard 9-slot backplane, this configuration makes it possible to carry out system cascading at the level of 19” frames (crates) using a high-speed optical connection (PCI Express Gen3 x8 or 10 Gb Ethernet) between system elements. In addition, remote monitoring and configuration of each frame is supported via a dedicated Gigabit Ethernet channel.

3.1.2 Power supply source interaction

The same way as with CPC512RC, CPC512 has an implemented universal power supply circuit that enables to operate with the power supply source in two modes: with support of power supply source control (similarly to the control applied in ATX power supply source) and without control support. During operation of CPC512/CPC512RC in the system slot of the Compact PCI Serial backplane, any of the specified modes can be used.

Control of power supply source is supported by CPC512/CPC512RC only during installation in the system slot of the Compact PCI Serial backplane. In this case, the power supply source should support control function and be equipped with:

- an integrated source of the standby power supply voltage +5 V_Standby with the minimum load current from 1 A.
- Input "Activation" (PS_ON#).

Power supply source control logic is determined by FPGA microcode of CPC512/CPC512RC CPU Module. Control can be carried out by any of the following methods: by using the "Power Button" on the control panel of 19” frame, by a programmable button of ejector's handle button (only for CPC512) (see the chapter 6 AMI Aptio BIOS Setup) or by ACPI software modules of the used operating system. The "Power Button" is connected to "Utility", which is located on the Compact PCI Serial backplane. This connector is also used for the power supply source control input (PS_ON#), as well as an external "Reset" button.

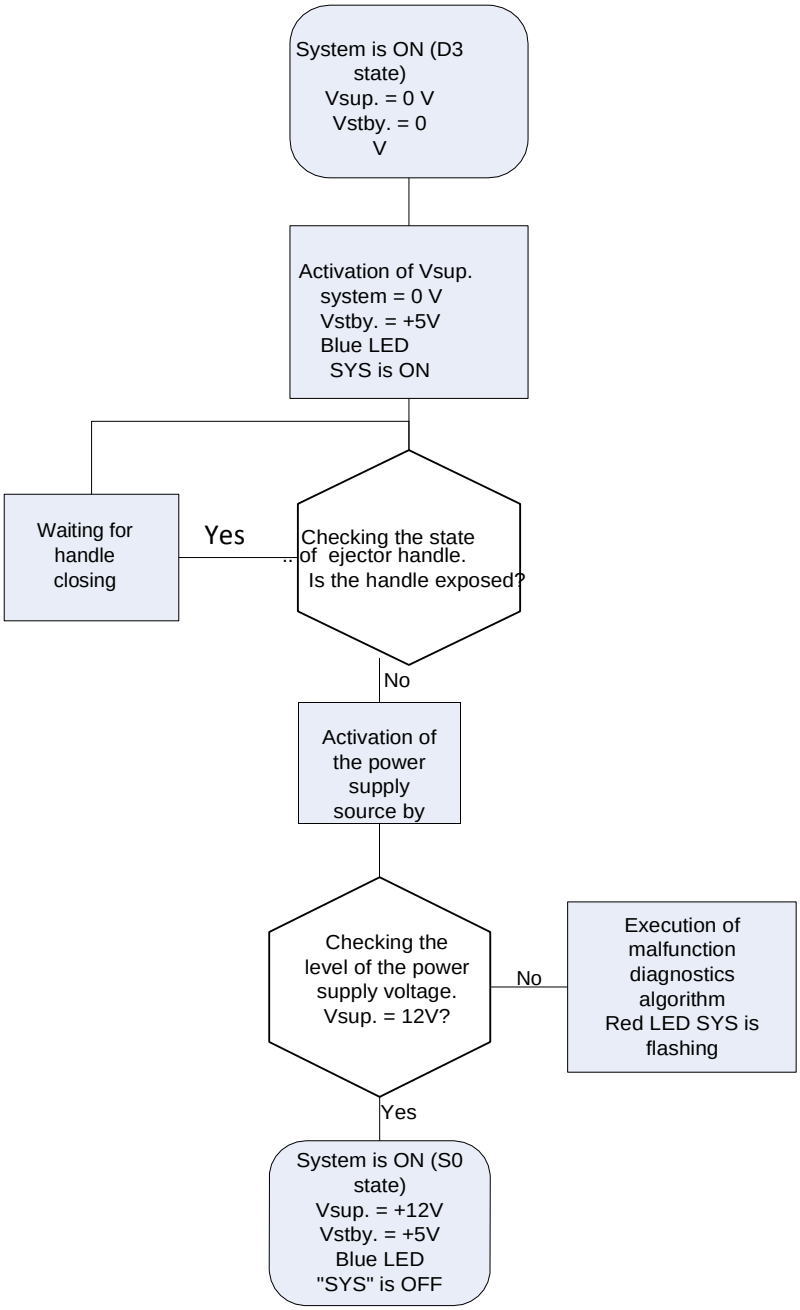


Fig. 3-2: System initial start algorithm from "Mechanical shutdown" (D3) position

Algorithm of Initial activation from the fully de-energized state (D3) (see Fig. 3-2) of the system is similar to all the CPC512 application options. If the power supply source fails to support control and therefore has no source
+5 V_Standby, the specified voltage is generated in a standard way directly on the CPC512 CPU Module. Diagnostics procedure mentioned in this algorithm, is designed for defining a malfunctioning power supply source both external and all those integrated into CPC512 module. The diagnostics result is indicated by a number of flashes of the red "SYS" LED. After diagnostics, main power supply feeding from the CPU Module is turned off and only LED indication system will be active.

Full system deactivation (both CPU module and peripheral modules) is possible only for the power supply source with control support and a relevant setting made in the BIOS menu (if required, only CPC512 module can be deactivated). If the power supply source does not support control, only CPU Module will be deactivated ("S5" mode). Procedure of

deactivation can be triggered by the ejector's handle button, if in BIOS menu relevant settings were made, software disconnect via ACPI OS (see Fig. 3-3) or by "Power Button" (see Fig. 3-4).

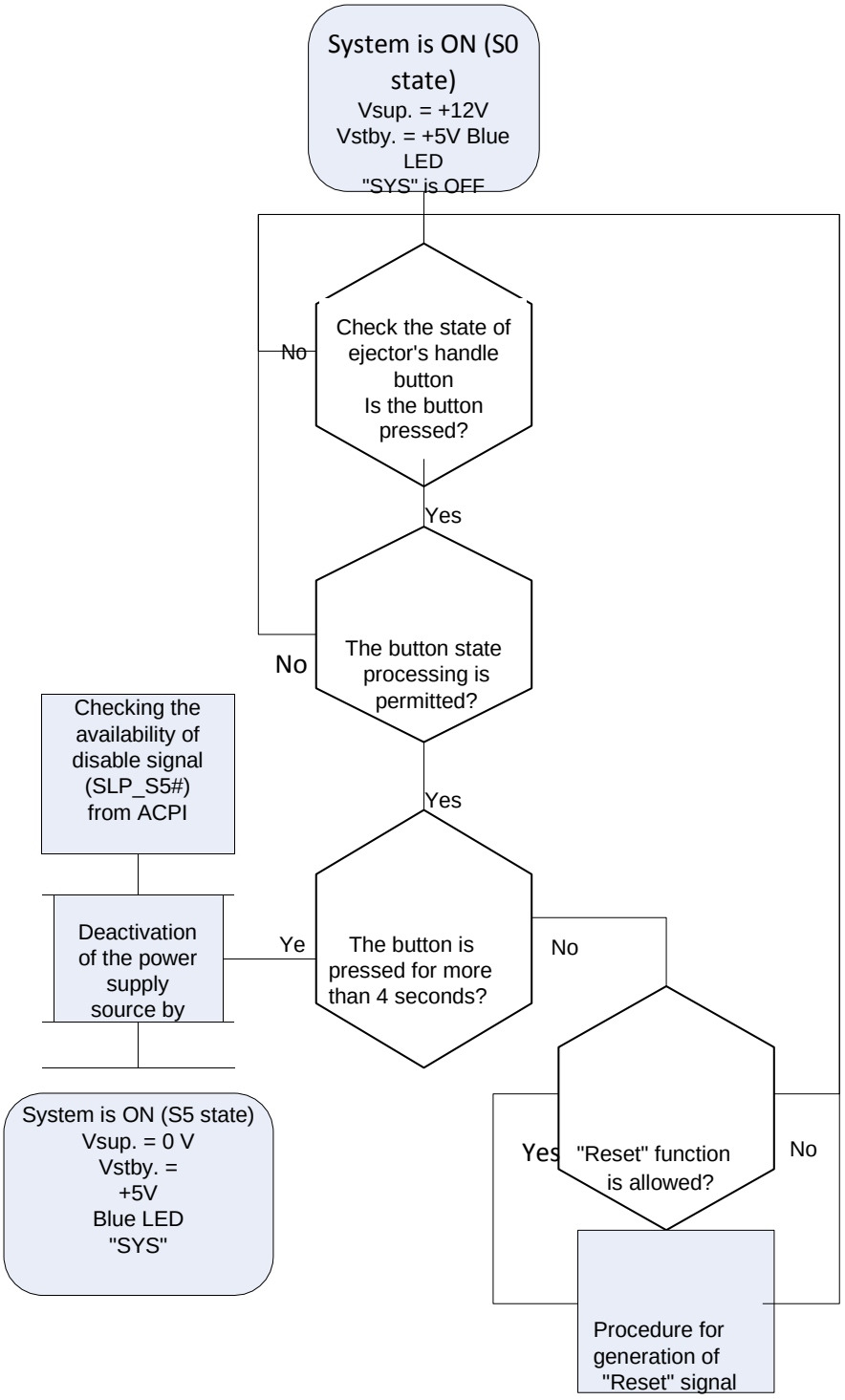


Fig. 3-3: System shutdown algorithm by using ejector handle button or by software via ACPI

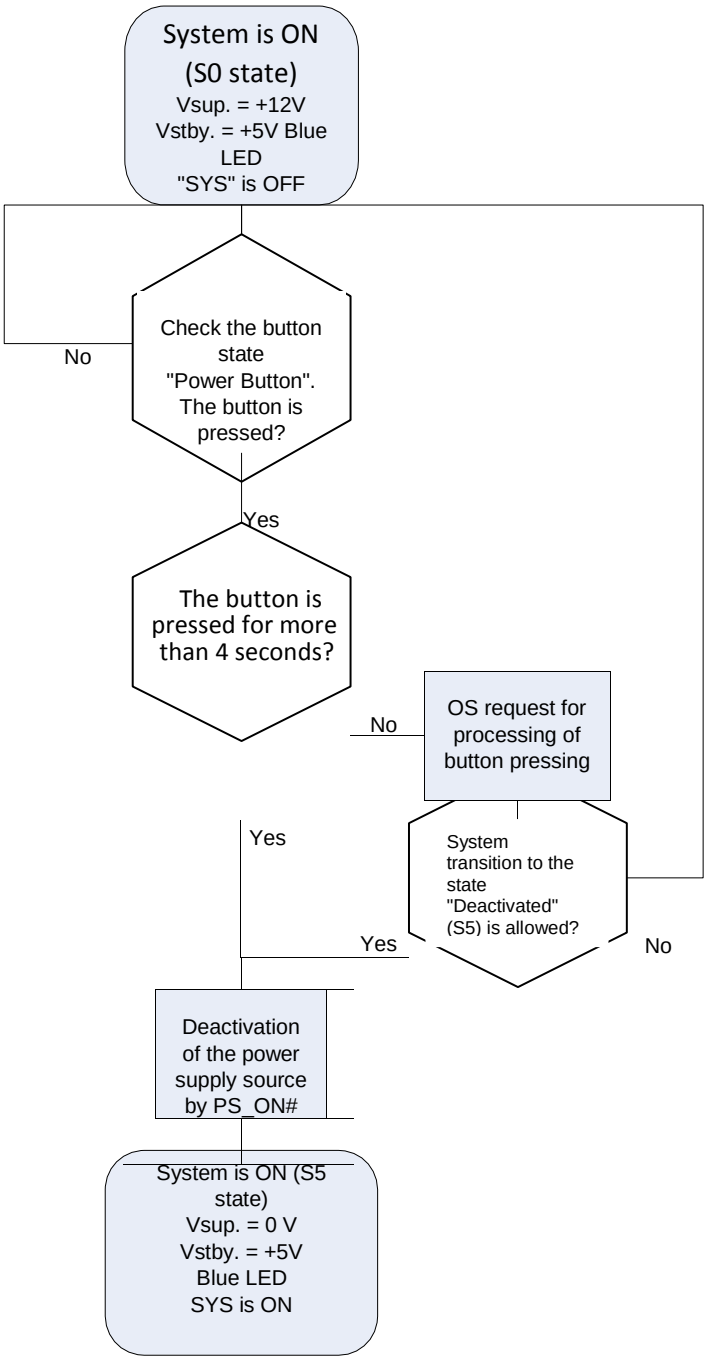


Fig. 3-4: Algorithm of using "Power Button" for system shutdown

After execution of any of the deactivation algorithms, the system (or only CPU Module CPC512) moves to the "Soft OFF" or "S5" state. From this state it is possible to move either to the fully de-energized state -
"Mechanical deactivation" (D3) or by contrast, to the fully activated state (S0). Moving to the S0 state is performed by pressing the ejector's handle button or "Power Button" (see Fig. 3-5).

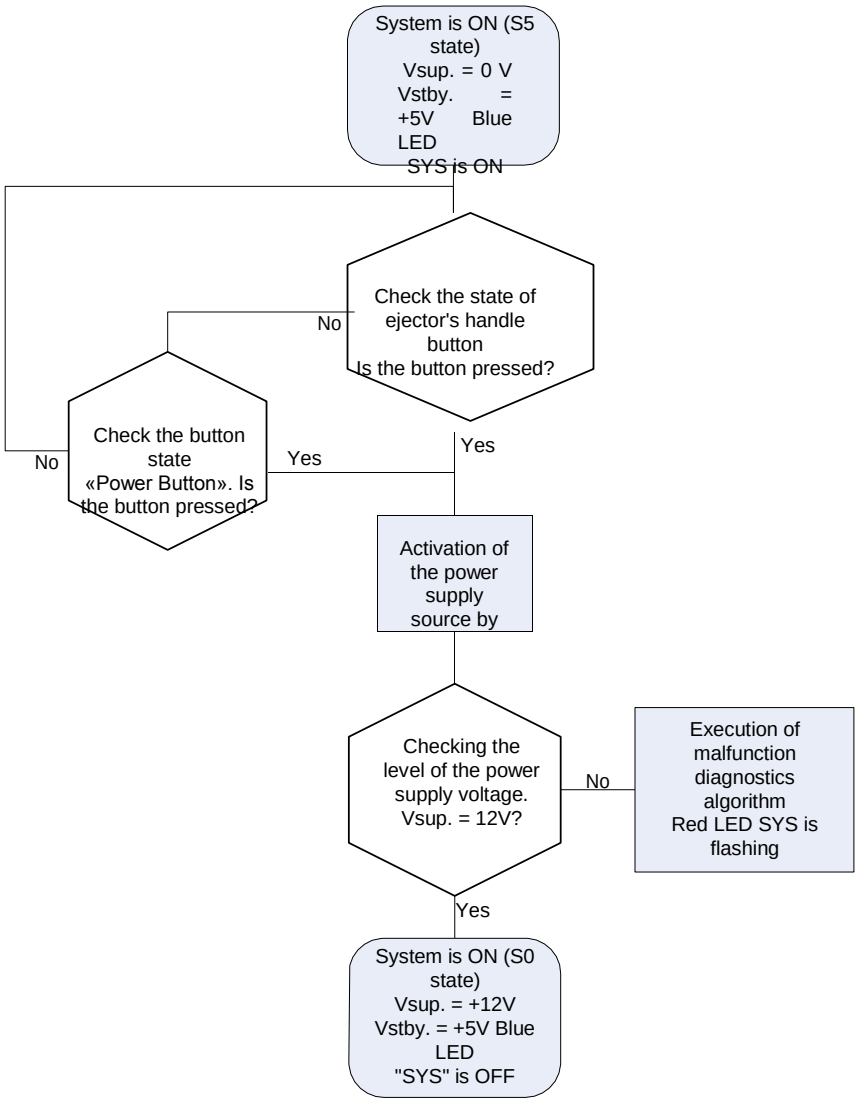


Fig. 3-5: System start algorithm from the "Software disconnect" (S5) position

3.1.3 Specifics of data storage system implementation

According to the specification [1] CPC512 supports operation of data drives, installed into backplane extension slots (see Fig. 3-1). The drives are numbered from the far right slot (see Fig. 3-6).

AS previously stated, CPC512 simultaneously supports up to six SATA drives (from 0 to 5). In this case, SATA port #5 is constantly routed for the use in MIC584 module and SATA port #4 can be switched between the slot #4 of the backplane and SATA interface of MIC584. Switching SATA port
#4 to the MIC584 module is carried out automatically using CPC512 in the peripheral slot or by software from the BIOS menu (by default, port #4 is connected to the backplane) during installation of CPC512 module in the system slot. The rest SATA ports ## 0-3 are routed to the Compact PCI Serial backplane. The other slots of the backplane are not supported for working with SATA drives.

In terms of their speed characteristics, the SATA ports are divided into ports with the supported transfer speed up to 6 Gb/sec (SATA ports ## 0 and 1) and ports with the supported transfer speed of up to 3 Gb/sec (SATA ports ##2-5).

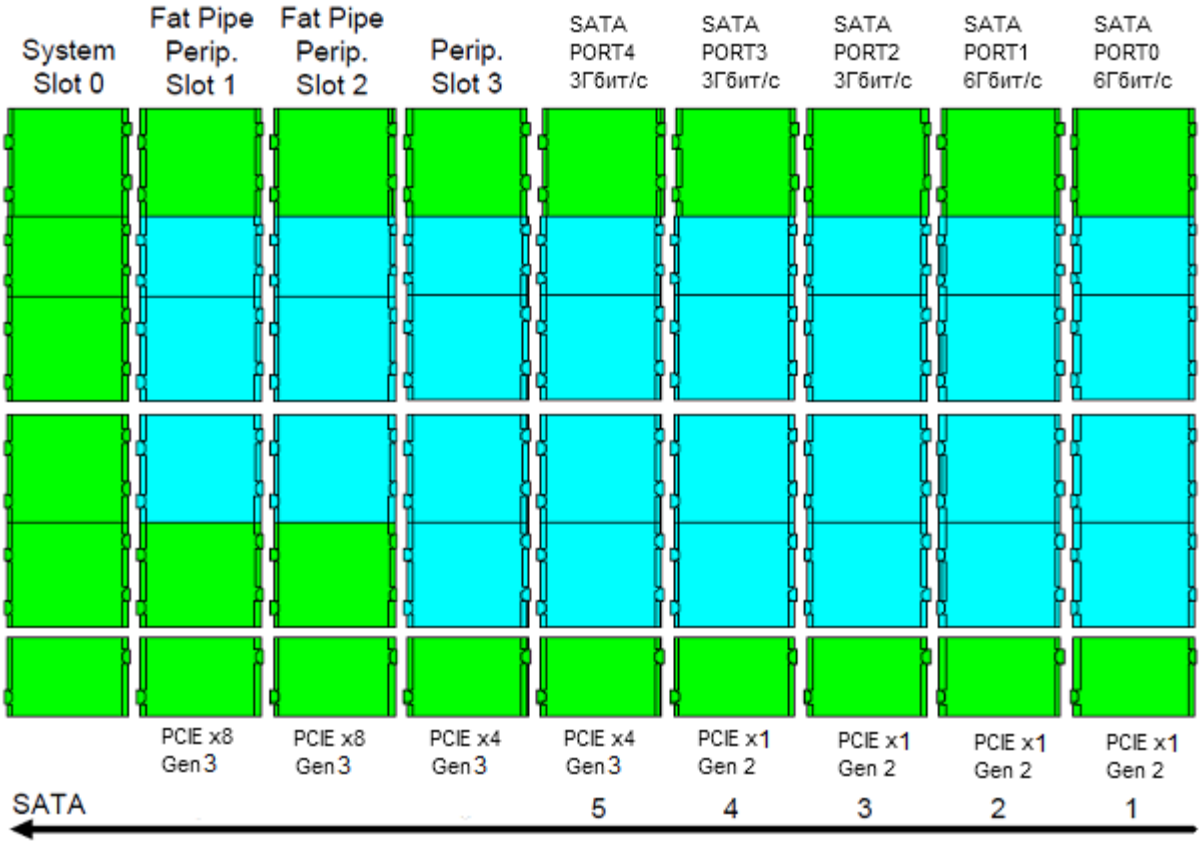


Fig. 3-6: Backplane location of SATA interfaces supported by CPC512 module

BD82QM77 controller installed on the CPC512/CPC512RC board enables operation with both single drives and arrange the so called RAID arrays.

Operation mode can be set via BIOS menu: "Advanced" - "SATA Configuration" - "SATA Mode Selection". The following options are possible:

- AHCI – connection of drives using Serial ATA protocol;
- IDE – connection of drives using ATA - compatible protocol;
- RAID – connection of drives using Serial ATA protocol with a possibility to arrange drives into array.

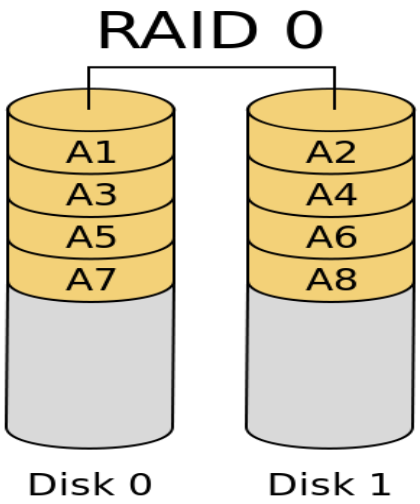
In the AHCI mode (by default) all the drives connected to ports ## 0-4 are available. All the functions of Serial ATA protocol are supported: NCQ, Link Power state etc. Data transfer speed corresponds to the one stated.

IDE mode is designed for being used in legacy operating systems that do not support Serial ATA protocol. This mode enables to use only the drives connected to SATA ports ## 0-3. Therefore, availability of two IDE-controllers with four drives is simulated. What is more, the speed of SATA drives operation does not depend on the emulated UDMA mode and can reach 3 Gb/sec.

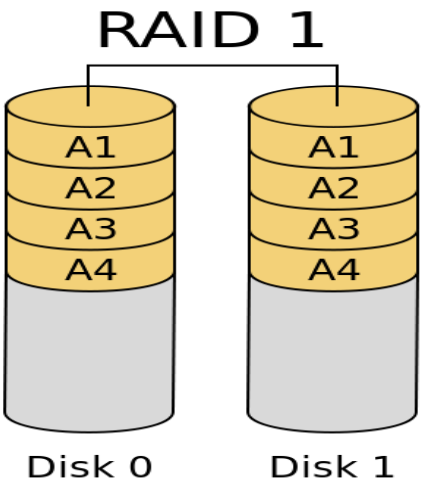
Hardware resources of BD82QM77 controller (Rapid Storage Technology) enables to arrange an array for data storage from the drives connected to SATA ports.

Available options of array arrangement:

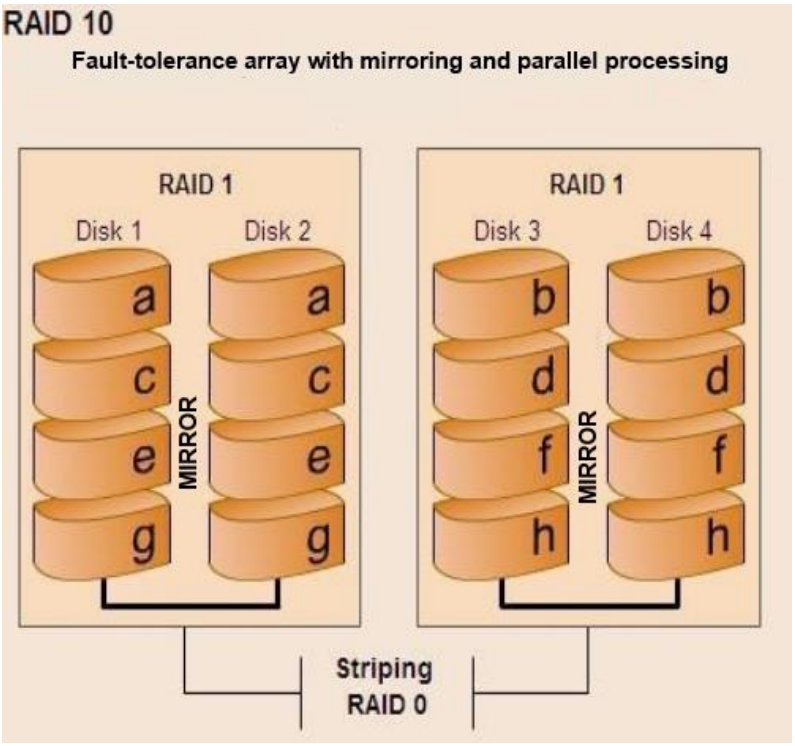
- RAID 0 (Striping). In this option, read/writing is carried out simultaneously to all the drives of the array (up to 6x drives are supported, which makes it possible to increase the performance of storage system by several times. The total capacity of the array in this case will be equal to the doubled capacity of the array drive, which is the smallest in volume. In this case, the fault tolerance remains low.



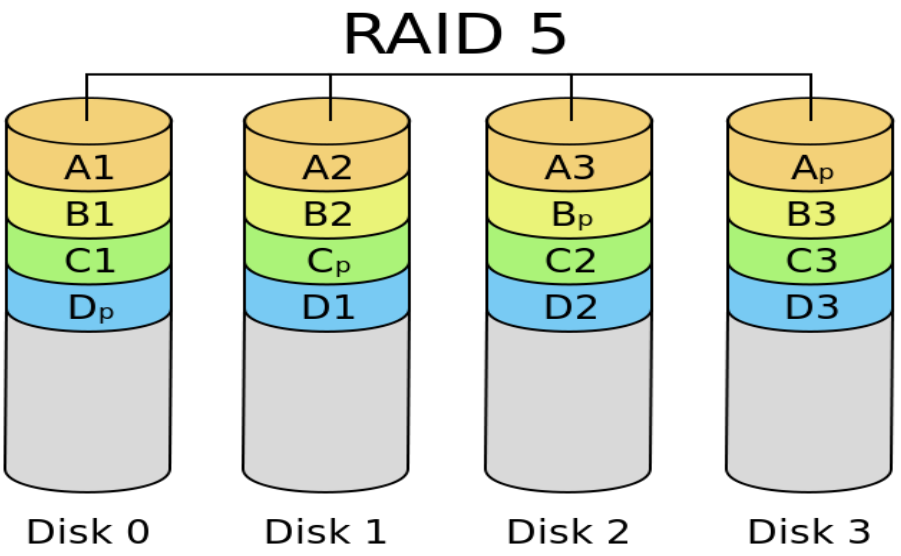
- RAID 1 (Mirroring). This option enables increasing the reliability of data storage by "mirroring" entry of data to the second drive of the array. In this case, performance of data storage system is lower and the total volume of array is equal to the volume of the least drive of the array.



- RAID 10. The mirrored array the data which are consecutively written to several drives, as in RAID 0. This architecture represents an array of RAID 0 type, which segments are RAID 1 arrays instead of single drives. In order to build RAID 10 array, it is necessary to have 4x SATA drives.



- RAID 5. This option ensures high efficiency of storage retaining fault tolerance for 3 or more drives. Data units and control sums are cyclically written to all the drives of the array. The volume of RAID5 is calculated using the formula (n-1) x hddsize, where n — is the number of drives in the array and hddsize — is the size of the least drive. The operation of writing data to RAID 5 volume requires additional resources which results in lowering performance, since additional calculations and writing operations are necessary, on the other hand during reading (compared to with single drive) we have an advantage, since the data flows from several array drives can be processed in parallel. RAID 5 is a good solution for applications which require a large data storage volumes at the same time retaining fault tolerance.



** The more detailed information on RAID array operation on the basis of Intel chipsets can be found in the "Intel Rapid Storage Technology" document. User Guide. Rev.1.0"*

As a carrier-module for SATA drive it is possible to use FastwelKIC550/KIC550RC or similar module.

If the KIC550/KIC550RC module is used for system storage, it is possible to simultaneously use of both SATA interface and PCI Express interface for data transfer. In such a case one of the drives installed on KIC550/KIC550RC is available over SATA and the other drive - over PCI Express interface using the PCI Express-SATA bridge installed on the board of KIC550/KIC550RC. The total number of drives can be increased at the time KIC550/KIC550RC is reconfigured for operation only with PCI Express interface. In this case the both drives on KIC550/KIC550RC become available via PCI Express interface. Hence, the drives on KIC550/KIC550RC in the peripheral slots from 8 to 4 will have hybrid PCI Express+SATA interfaces and in slots from 3 to 1 – only PCI Express interface. Backplane slots, where PCI Express interfaces are available and which are supported by CPC512/CPC512RC, are specified in Fig. 3-6. The mode detailed information on operation with KIC550/KIC550RC can be found in the User Manual for KIC550/KIC550RC, which is available on Manufacturer's and distributor's servers, as well as is obtained upon request by Manufacturer's technical support service.

4 Installation

CPC512/CPC512RC is easy to install. In addition to that, it is necessary to strictly follow the below rules, warnings and procedures in order to properly install the module, avoiding damages to the devices, system components, as well as injures to the staff.

4.1 Safety requirements

When handling KIC512/KIC512RC, the below safety requirements should be strictly followed. Manufacturer shall not be liable for any damages, arising out as a result of non-observance of such requirements.

Warning!

Switch off the CompactPCI system power supply before installing the module into a free slot. Violation of this rule can pose a threat for your health and life, as well as could lead to system or module damages.

Electrostatic Sensitive Device (ESD)!

CompactPCI Module contains components sensible to static electricity. In order to prevent module damages, observe the following precaution measures:

- Before touching the module, discharge the static electricity from your clothes, as well as from the tools before using them.
- Do not touch electronic components and connector contacts.
- If you have a professional workplace equipped with antistatic protection, don't forget to use it.

4.2 Installation and removal of CPC512

Warning!

Be careful when handling the module, since the cooling heatsink can become too hot. Do not touch the heatsink during removal of the module.

Moreover, the module should not be placed on any surface or put in any container until both module and heatsink will have the room temperature.

4.2.1 Procedure of CPC512 installation

In order to install the CPC512 module into the system, follow the procedure below:

1. Make sure that the safety requirements, listed in the previous chapter, have been met.

Warning!

Noncompliance with the following directions could lead module damages and improper operation of the system.

2. Before installation, make sure that the module has configuration corresponding to application's requirements. Information on the installation of peripheral devices and I/O equipment is specified in the relevant sections of this chapter. Information on installation of MIC584 onto CPU module is given in the User Manual for MIC584 IMES.421459.584 UM.
3. If CPC512 is going to work with the mezzanine module, you should connect the mezzanine module to the relevant connector of CPC512 before installation of CPC512, see sub-paragraphs 2.5.2 Connector for installation of mezzanine module and 4.5 Installation of MIC584 mezzanine module.

Warning!

Further operations should be carried out carefully, in order not to damage both CPC512 and other devices of the system.

4. For installation of CPC512 the following actions should be performed:
   - Before start of the installation, make sure that system power supply is switched off.

Warning!

Do not apply force when inserting module's connector into the backplane's connector. For installation of the module into the connector, use the handle on the front panel.

- Carefully insert the module into a necessary slot, moving it along the guide rails until it touches the backplane connector.
- Using the handle on the front panel, push the module into the backplane connector. The module is considered to be fully inserted, when the handle is snapped.
- Fasten the module with two retention screws on the front panel of CPC512 (see Fig. 1-11).
- Connect all the necessary external interface cables to the module.
- Make sure that both CPC512 and all the connected cables are safely fixed.

CPC512 is ready for operation.

4.2.2 Procedure of CPC512 removal

In order to remove the module, the following operations should be performed:

1. Make sure that the safety requirements, listed in chapter 4.1 have been met. Particular consideration should be given to the warning relating to heatsink temperature, which is specified in the beginning of the subparagraph 4.2!

Warning!

Further operations should be carried out carefully, in order not to damage both CPC5112 and other devices of the system.

2. Before starting to remove CPC512, make sure that system power supply is switched off.
3. Disconnect all interface cables from the module.
4. Unscrew the fastening screws on the front panel.

Warning!

Be careful when handling the module, since the cooling heatsink can become too hot. Do not touch the heatsink during removal of the module.

5. Unblock the handle of the front panel by pressing the ejector handle button and moving it down, take the module out of the backplane's connector (see Fig. 1-11). After the module has been taken out the backplane connector, pull it from the slot along the guide rails.
6. Dispose of the module at your own discretion.

4.3 Installation and removal of CPC512RC

Installation of CPC512RC has its own specifics.

When handling CPC512RC, strictly follow the safety regulations, given in subparagraph 4.1. Manufacturer shall not be liable for any damages, arising out as a result of non-observance of such requirements.

Warning!

Be careful when handling the module, since the heatspreading cassette can become too hot. Do not touch the cassette during removal of the module.

Moreover, the module should not be placed on any surface or put in any container until both module and heatsink will be cooled down to the room temperature.

4.3.1 Procedure of CPC512RC installation

Warning!

Noncompliance with the following directions could lead module damages and improper operation of the system.

In order to install the CPC512RC module into the system, follow the procedure below:

1. Make sure that the safety requirements, listed in the previous chapter, have been met.
2. Before installation, make sure that the module has configuration corresponding to application's requirements. Information on the installation of peripheral devices and I/O equipment is specified in the relevant sections of this chapter.

Warning!

Further operations should be carried out carefully, in order not to damage both CPC512RC and other devices of the system.

3. For installation of CPC512RC the following actions should be performed:
   - Before start of the installation, make sure that system power supply is switched off.
   - Make sure that ejector's handles A and B are in the "Open" position (see Fig. 1-13)
   - Make sure that the screws of splitters have been unscrewed and wedges elements have been folded in line. If necessary, the wedges elements can be positioned manually.
   - Carefully insert the module into the required slot.
   - Move the module along the rails until contact with backplane connector.
   - Apply some effort to insert the module into the backplane connector. In this case, the module's front panel will be positioned close by enclosure components.

- Move A and B ejector handles to the "Closed" position.
- Fasten the module on the front panel of CPC512RC by two retention screws from the installation kit (see Fig. 1-14).
- Tighten the splitter screws applying force for the purpose of better thermal contact of the cassette with enclosure coolers.

Warning!

When installing CPC512RC into enclosure don't forget to make the splitters operational. Otherwise, at startup, module is subject to fast overheating and its operability could be compromised.

- Connect all the necessary external interface cables to the module.
- Make sure that both CPC512RC and all the connected cables are safely fixed.

CPC512RC is ready for operation.

4.3.2 Procedure of CPC512RC removal

Warning!

Further operations should be carried out carefully, in order not to damage both CPC5112RC and other devices of the system.

In order to remove the module, the following operations should be performed:

- Make sure that the safety requirements, listed in this chapter, have been met. Pay special attention to the warning related to cassette temperature!
- Before starting to remove CPC512RC, make sure that system power supply is switched off.
- Disconnect all interface cables from the module.
- Unscrew the fastening screws on the front panel.

Warning!

Be careful when handling the module, since the cassette can become too hot. Do not touch the cassette during module replacement.

- Unblock the splitters, turning the screws in a direction for module removal, as far as they turn.
- Simultaneously moving A and B ejector handles in the "Open" direction, pull the module out of the backplane connector.
- Keep pulling by A and B handles and pull the module out of the enclosure along the guide rails.
- Dispose of the module at your own discretion.

4.4 Installation of peripheral devices for CPC512/CPC512RC

CPC512/CPC512RC makes it possible to connect many various peripheral devices to it, which installation methods could significantly differ. The following sections contain only the general installation instructions, instead of the detailed algorithms.

4.4.1 Installation of MicroSD memory cards

CPC512/CPC512RC is equipped with XS10 connector that supports MicroSD card. External view of Secure Digital connector with the installed memory card is shown in Fig. 2-6.

Carefully push the properly positioned Secure Digital card into the connector along the guide rails and slightly press on it to let the contacts fully enter the connector.

Note

It is recommended to use MicroSD-cards, marked and formatted in this device.

Warning!

MicroSDHC card installed into the XS10 connector should be designed for operation in the temperature range similar to the one of CPC512/CPC512RC module. Otherwise, proper operation of the module in the temperature range, stated in the technical specifications, shall not be guaranteed.

Warning!

Be careful when replacing the MicroSD card, since the cooling heatsink can become too hot.

4.4.2 Connection of USB devices

CPC512/CPC512RC supports the use of any computer peripheral USB devices of Plug&Play standard (e.g. keyboard, mouse, printer etc.).

Note

All USB devices can be connected and disconnected when the power of such devices and main system is on.

4.4.3 Battery replacement

In order to replace lithium battery, use a battery of the same type or a battery recommended by manufacturer for such replacement. Among the suitable types – RENATA CR2032 or other compatible models.

Important note:

During battery replacement proper polarity should be observed.

The battery should be replaced with a similar battery or the one, recommended by the manufacturer.

The used battery has to be utilized in accordance with the prescribed standards.

Expected work period of the battery with a capacity of 190 mAh is approximately 5-6 years, based on 8 hours of battery operation at 30°C. However, the battery work period heavily depends on the operating temperature, as well as on the fact how long the system stays in the off position.

It is recommended to replace batteries every 4-5 years of operation. Do not wait for the end of service life period.

4.5 Installation of MIC584 mezzanine module

MIC584 is installed in XS6 connector of CPC512. Sequence of MIC584 installation onto CPU module is given in the User Manual for MIC584 IMES.421459.584 UM.

Warning!

Installation of the mezzanine module is possible to all the convection versions of CPC512 modules except for IMES.421459.512-03. The CPC512RC module is also not equipped with MIC584 mezzanine.

4.6 Software installation

Procedure of installation of Ethernet drivers and drivers of all the peripheral devices installed to the module is specified in files, supplied with the drivers.

This User Manual also contains no description of the Installation procedure of operating systems. Refer to the documents attached to the operating system.

5 System configuration

5.1 Reset BIOS settings to factory settings and switching module to the Transparent mode

If the system fails to boot (e.g. due to improper configuration of BIOS or incorrect password), the settings parameters saved in CMOS, can be cleared using the SA switch1, located in the tope side of the board (see Fig. 5-2).

Fig. 5-1: Switch of SA1 operation mode for CPC512/CPC512RC

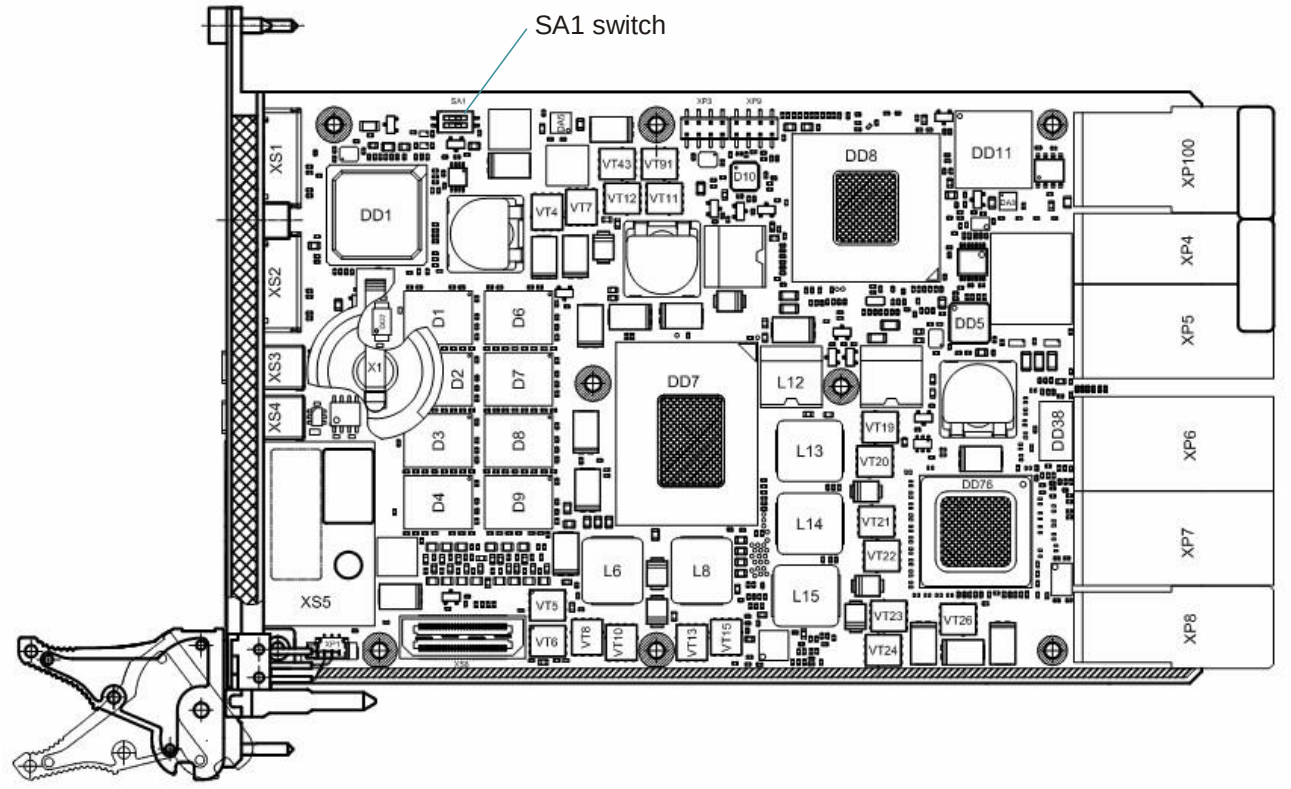


Fig. 5-2: Location of SA1 switch on the board

Using the SA1 switch it is possible to perform the following actions:

- BIOS Setup reset to the default settings.
- Switching the module to the Peripheral Root mode (operates only when CPC512/CPC512RC is installed into peripheral slot)

Switch position is shown in the table:

Table 5-1.: Possible configuration options of CPC512/ CPC512RC using the SA1 switch

Switch # (specified on the enclosure)	**Switch purpose**	**Position of the SA1 switch** (see Fig. 5-1)	**Function**
1	BIOS Setup reset to the default settings.	OFF	Position upon delivery
1		ON	BIOS Setup reset to the default settings.*
2	Switching module to the Peripheral Root mode	ON	PCI Express FAT1 interface operates in the "transparent" mode. "PE" LED - orange.
2		OFF	PCI Express FAT1 interface is in the NT mode. "PE" LED - green.

** Sequence of BIOS settings reset back to factory settings:*

1. Turn off the power supply.
2. Remove CPC512/CPC512RC from the crate.
3. Move the SA1.1 operating mode switch to the ON position for 5 seconds.
4. Put the SA1.1 switch back to the OFF position.
5. Install CPC512/CPC512RC module into the crate.
6. Turn on the power supply.

6 AMI Aptio BIOS Setup

6.1 Launch and update of BIOS Setup program

Your computer has an installed adapted version of AptioTM TSE (Text Setup Environment) BIOS, which is a standard system for IBM PC AT-compatible computers. It supports Intel®x86 and Intel®x86-compatible CPUs, ensures low-level support for CPU, memory and I/O subsystems.

Using BIOS Setup program you can change BIOS parameters and control special computer operation modes. It enables to change basic parameters of system configuration. These parameters are stored in the non-volatile memory.

6.1.1 Start of BIOS Setup program

In order to start BIOS Setup program during the POST (Power On Self Test) procedure, it is required to press "F2" or <DEL> key on the keyboard or console PC keyboard (when "Hyperterminal" program is used as the terminal).

Pressing of "F2" key calls a menu of the BIOS Setup program with the "Main" active tab.

6.1.2 Navigation keys

Selection of BIOS menu items is carried out using keyboard and the following keys:

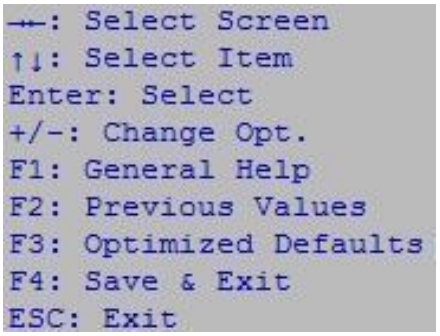


Fig. 6-1: Assignment of navigation keys

Key	Purpose
ENTER	Using "ENTER" key enables the user to choose the value for the editable option or to move to the submenu.
→←	"Left" and "Right: keys make it possible to select an Aptio™ TSE screen (used for moving through the tabs). E.g. "Main", "Advanced" etc.

↑↓	"Up" and "Down" keys enable to move to the submenu line (used for moving through the menu items).
+ −	"+" and "-" keys on the numeric part of keyboard enable to change any values in the selected menu tab. E.g. "Date" and "Time".
Tab	"Tab" key enables to choose the field of values of Aptio™ TSE.
F1	This key calls the main help window.
F2	This key enables the user to load the previous value to the TSE.
F3	This key enables the user to load optimal default settings to the TSE.
F4	This key enables the user to save current settings and exit the TSE.
ESC	<ESC> key enables to discard the changes made and exit Aptio™ TSE. Press <ESC> key to exit Aptio™ TSE without saving. The next screen will show message: Press <Enter> to discard changes and exit. You can also use arrow keys in order to choose "Cancel" option with subsequent clicking the <Enter> key to exit this menu item and to go back to the previous screen.
Function keys	When additional functional keys become available, they are displayed in the help window according to their functions.

Note

This algorithm of operations with menu covers all other tabs of the BIOS Setup program.

6.1.3 BIOS update

BIOS update is carried out using the Flash Programming Tool utility (is available on network file-servers of the manufacturer and official distributor).

Actions for updating BIOS

1. Boot MS-DOS;
2. Execute command fpt.exe -F <bios image file name> -BIOS

6.2 Main

This screen of the BIOS Setup program is a title entry screen. The menu of this tab is used for configuration of the system clock and data, as well as switching menu tabs for assigning module settings, as well as information on BIOS program is routed.

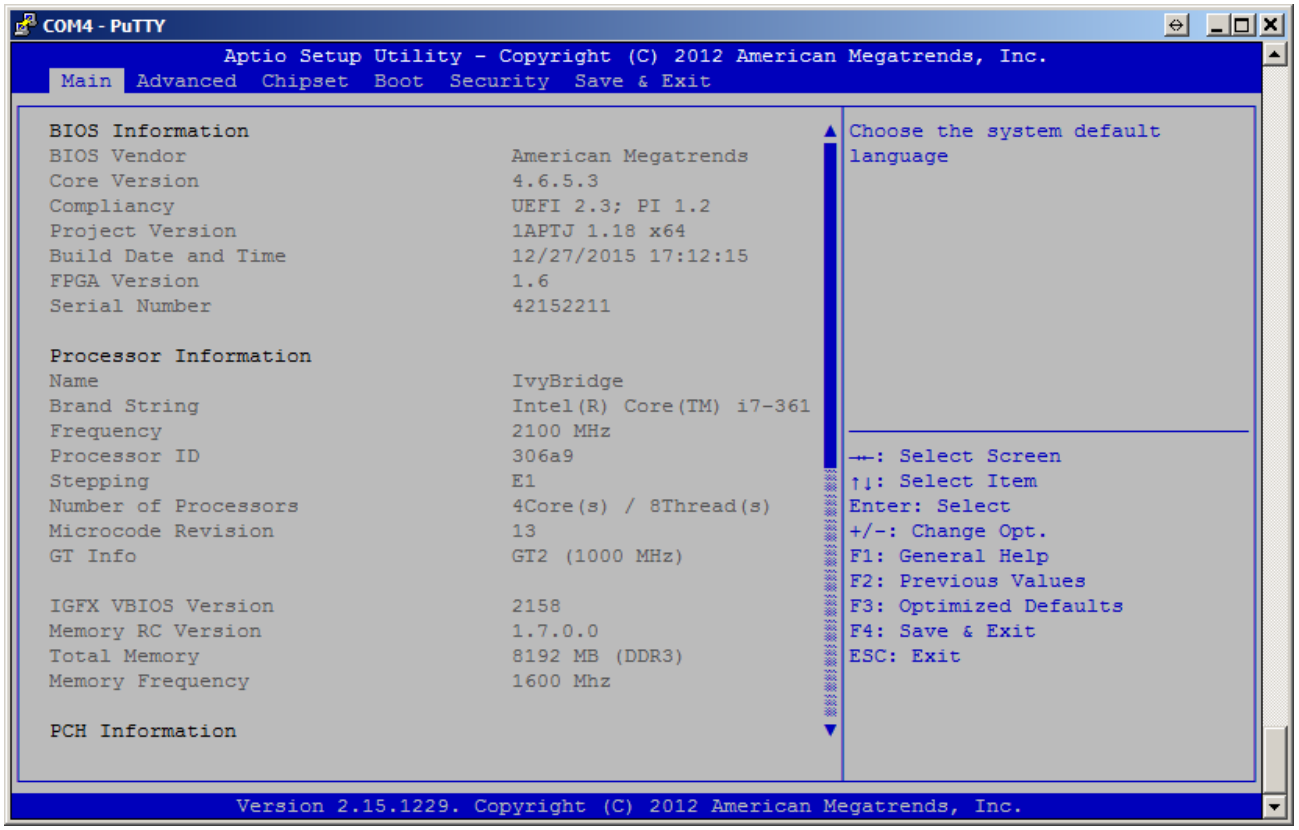


Fig.6-2: View of the "Main" menu tab

Function	Purpose
Project Version	BIOS version.
FPGA Version	FPGA version.
Processor Information	CPU information.
PCH Information	Chipset-related information.

Note

Time is set in the 24-hour format.

6.3 Advanced

This tab enables to perform additional module settings. The figure below shows the view of the "Advanced" menu tab.

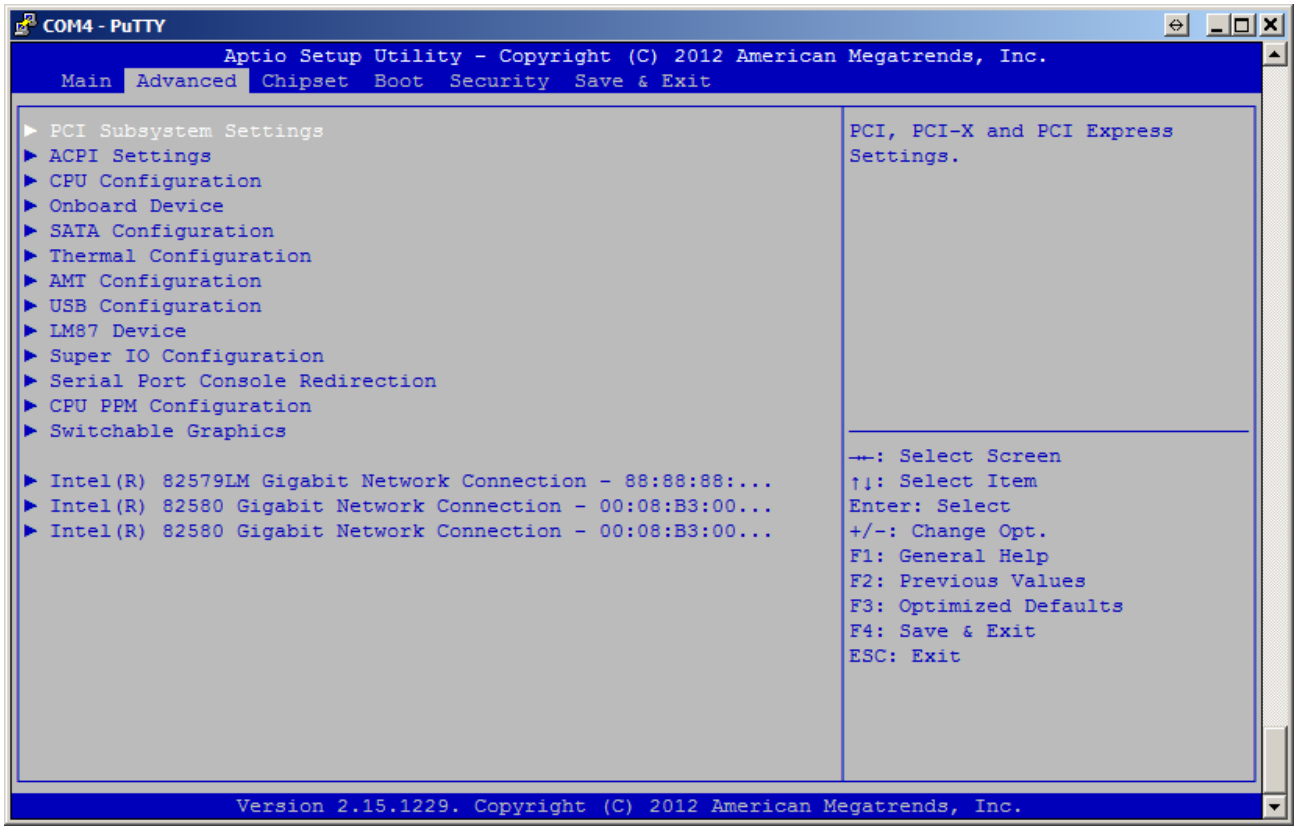


Fig. 6-3: View of the "Advanced" menu tab

Function	Purpose
PCI Subsystem settings	Settings of PCI and PCIE bus.
ACPI Settings	Setting for the ACPI - compatible operating systems.
CPU Configuration	CPU configuration.
Onboard Device	Configuration of module's equipment.
SATA Configuration	Configuration of SATA-controllers and drives.
Thermal Configuration	Configuration of the parameters that depend on temperature.
AMT Configuration	Configuration of Intel AMT technology.
USB Configuration	USB configuration.
LM87 Device	Monitoring of temperature and voltage
Super IO Configuration	Configuration of devices available on RIO board.
Serial Port Console Redirection	Redirection of serial port.
CPU PPM Configuration	Configuration of CPU power preservation mode.
Switchable Graphics	"Switchable Graphics" mode.
Intel (R) 82580 Gigabit Network Connection	Information on network controllers.

The below subsections contain description of the opened sub-menus.

6.3.1 Onboard Device Configuration

This submenu determines configuration of devices on the board. View of the submenu is shown in the figure below.

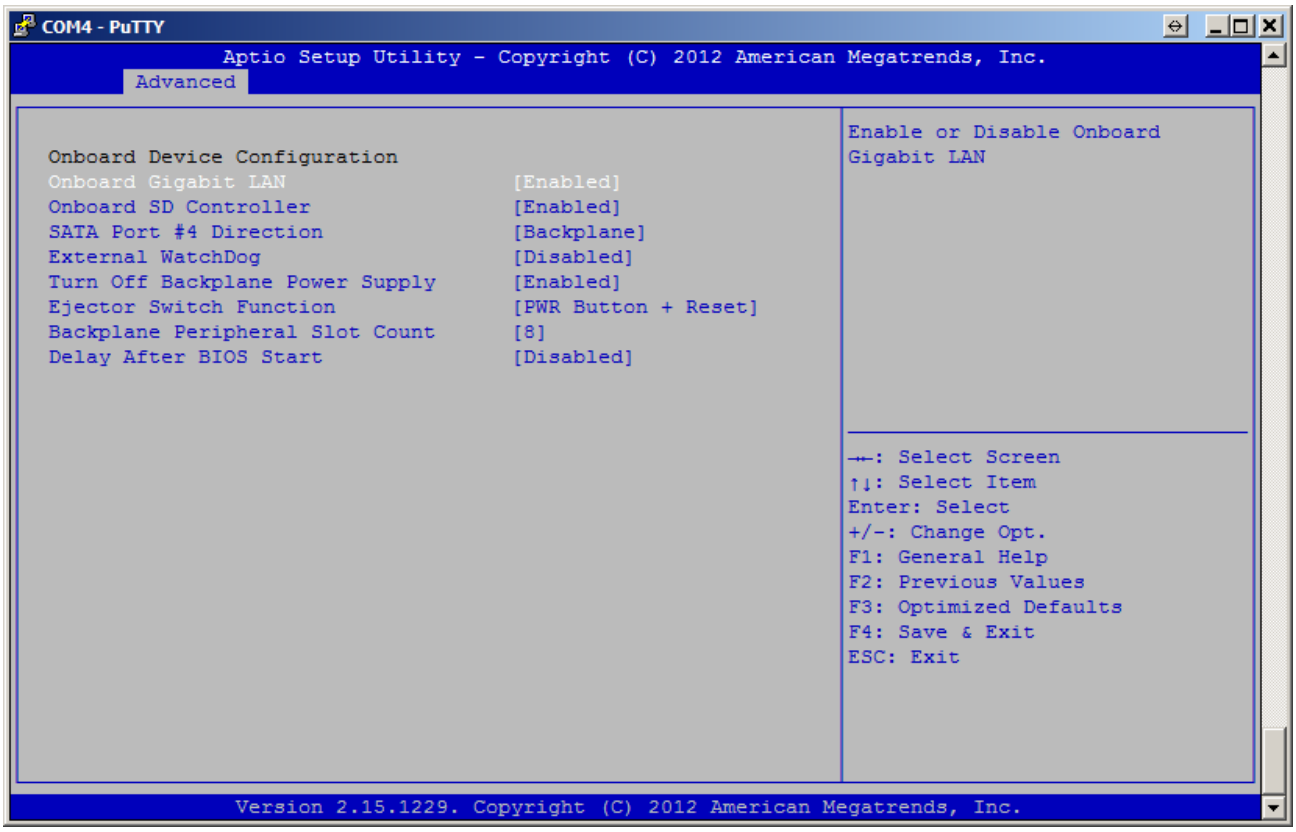


Fig. 6-4: View of the "Onboard Device Configuration" submenu screen

Function	Purpose	Default value
Onboard Gigabit LAN [**Enabled**/Disabled]	Onboard Gigabit LAN card	**Enabled**
Onboard SD Controller [**Enabled**/Disabled]	Possibility to disable the SD-controller.	**Enabled**
SATA Port #4 Direction	SATA direction of the port #4.	**Backplane**
External WatchDog [Enabled/**Disabled**]	Possibility to enable Watchdog timer with 0x308 base address in the I/O space.	**Disabled**
Turn Off Backplane Power Supply	Turn Off Backplane Power Supply	**Enabled**
Ejector Switch Function [**PWR Button+Reset**/ PWR Button/Disabled]	Operation mode of the board's ejector switch.	**PWR Button+Reset**
Backplane Peripheral Slot Count	Backplane Peripheral Slot Count (from 2 to 8)	**8**
Delay After BIOS Start	Delay after BIOS start	**Disabled**

6.3.2 PCI Subsystem settings

The "PCI Subsystem settings" submenu is used for configuration of PCI and PCIE bus.

Fig.6-5: View of the "PCI Subsystem settings" menu tab

Function	Purpose	Default value
PCI Bus Driver Version	PCI Bus driver version.	V 2.05.02
PCI 64bit Resources Handling	Assigning resources in the 64-bit address space.	-
Above 4G Decoding	Activation of 64-bit addressing.	**Disabled**

6.3.3 ACPI Settings

The "ACPI settings" submenu is used for configurations for the ACPI - compatible operating systems.

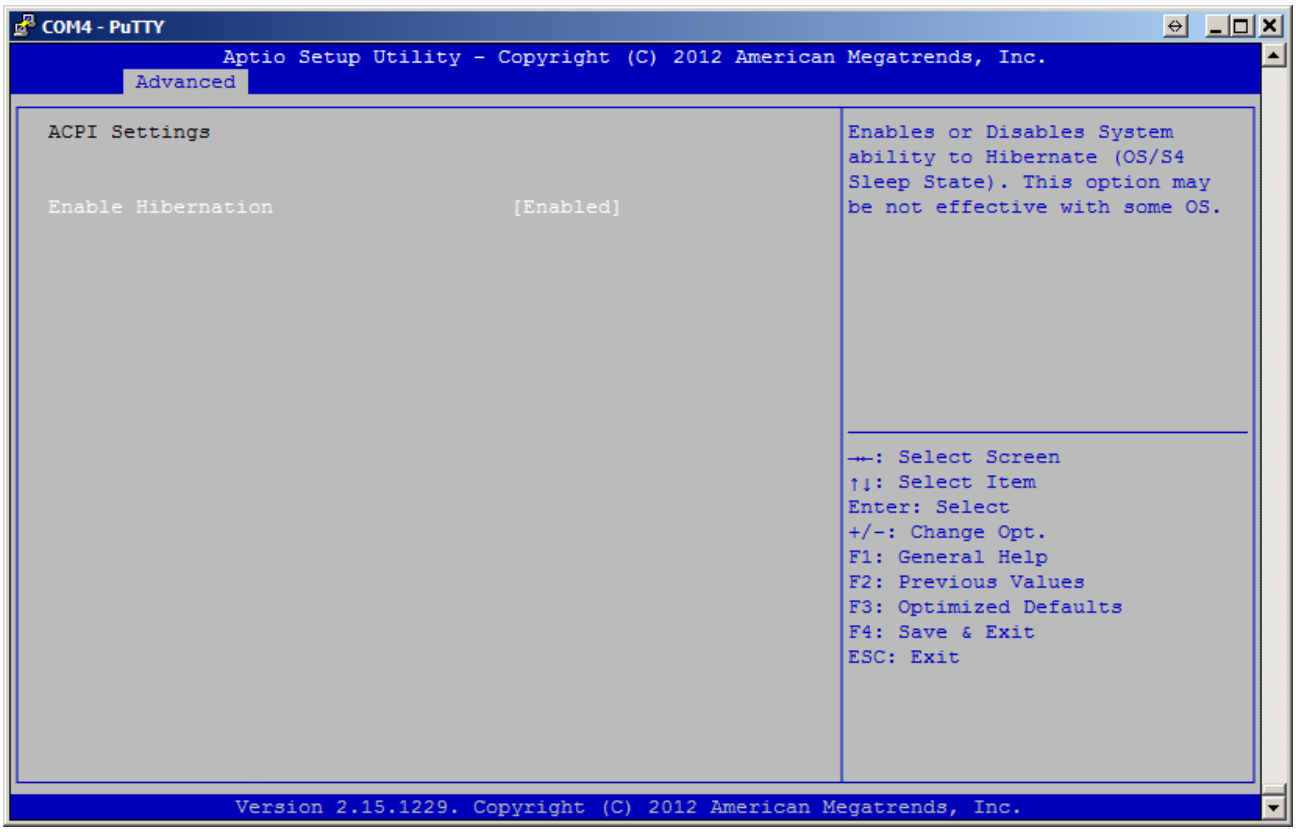


Fig.6-6: View of the "ACPI settings" menu tab

Function	Purpose	Default value
Enable Hibernation [**Enabled**/Disabled]	System hibernation capability.	**Enabled**

6.3.4 CPU Configuration

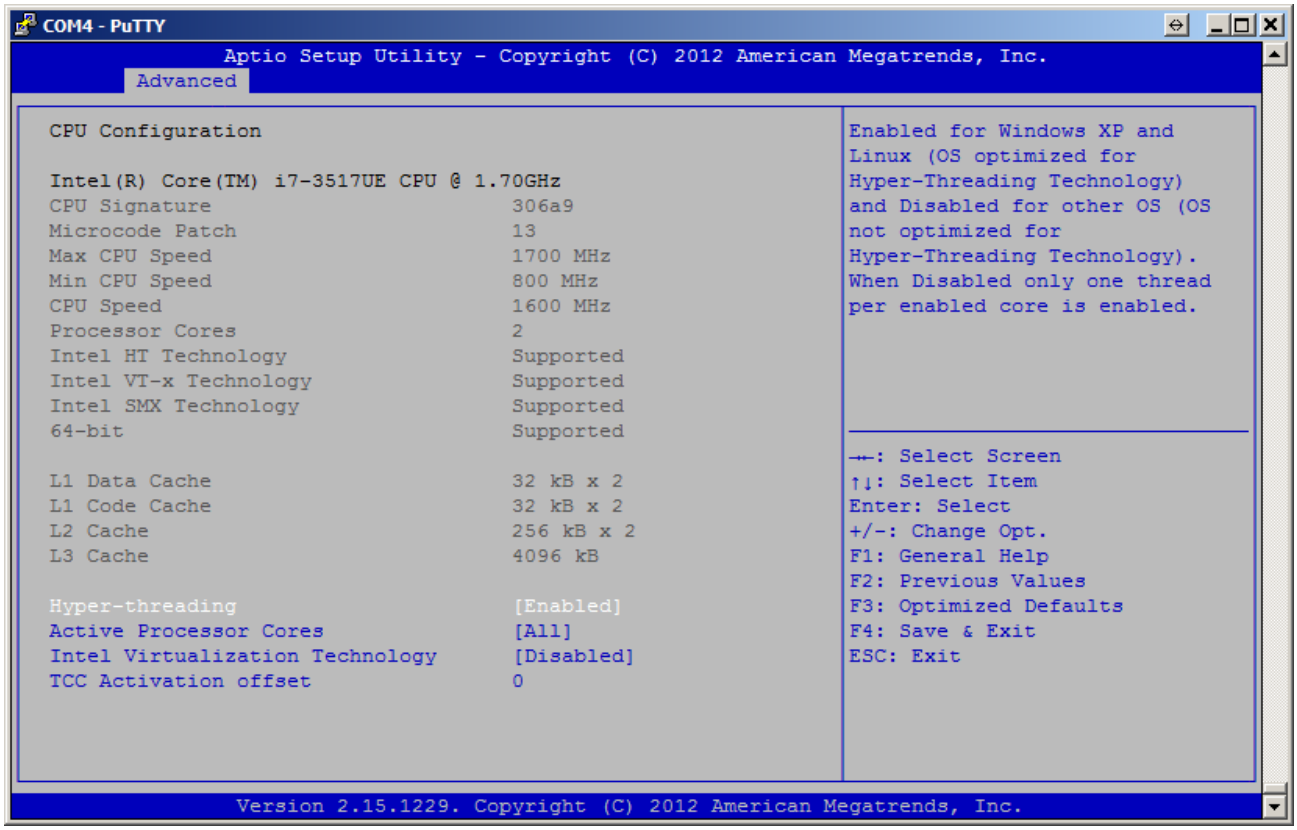


Fig.6-7: View of the "CPU configuration" menu tab

Function	Purpose	Default value
CPU Signature	Type of the CPU	-
Microcode Patch	Version of microcode.	-
Max CPU Speed	Maximum CPU speed.	-
Min CPU Speed	Minimum CPU speed.	-
CPU Speed	Processor speed.	-
Processor Cores	Number of CPU cores.	-
Intel HT Technology	Support of Hyper- Threading technology	-
Intel VT-x Technology	Support of virtualization technology.	-
Intel HT Technology	Support of SMX technology.	-
64 bit	Support of 64 bit architecture	-
L1 Data Cache	Memory capacity of L1 data Cache	-
L1 Code Cache	Memory capacity of L1 Cache of program codes	-
L2 Cache	Memory capacity of L2 Cache	-
L3 Cache	Memory capacity of L3 Cache	-

Hyper-threading [**Enabled**/Disabled]	Enabling the Hyper- Threading technology.	**Enabled**
Active Processor Cores [**All**/1]	Number of active CPU cores.	**All**
Intel Virtualization Technology [Enabled/**Disabled**]	Possibility to enable the VT-d virtualization technology.	**Disabled**
TCC Activation offset	Offset of CPU temperature, at which reduction of CPU frequency is activated with regard to the one set by the manufacturer (100^{o}C).	**0**

6.3.5 SATA Configuration

Configuration of SATA-controllers and drives.

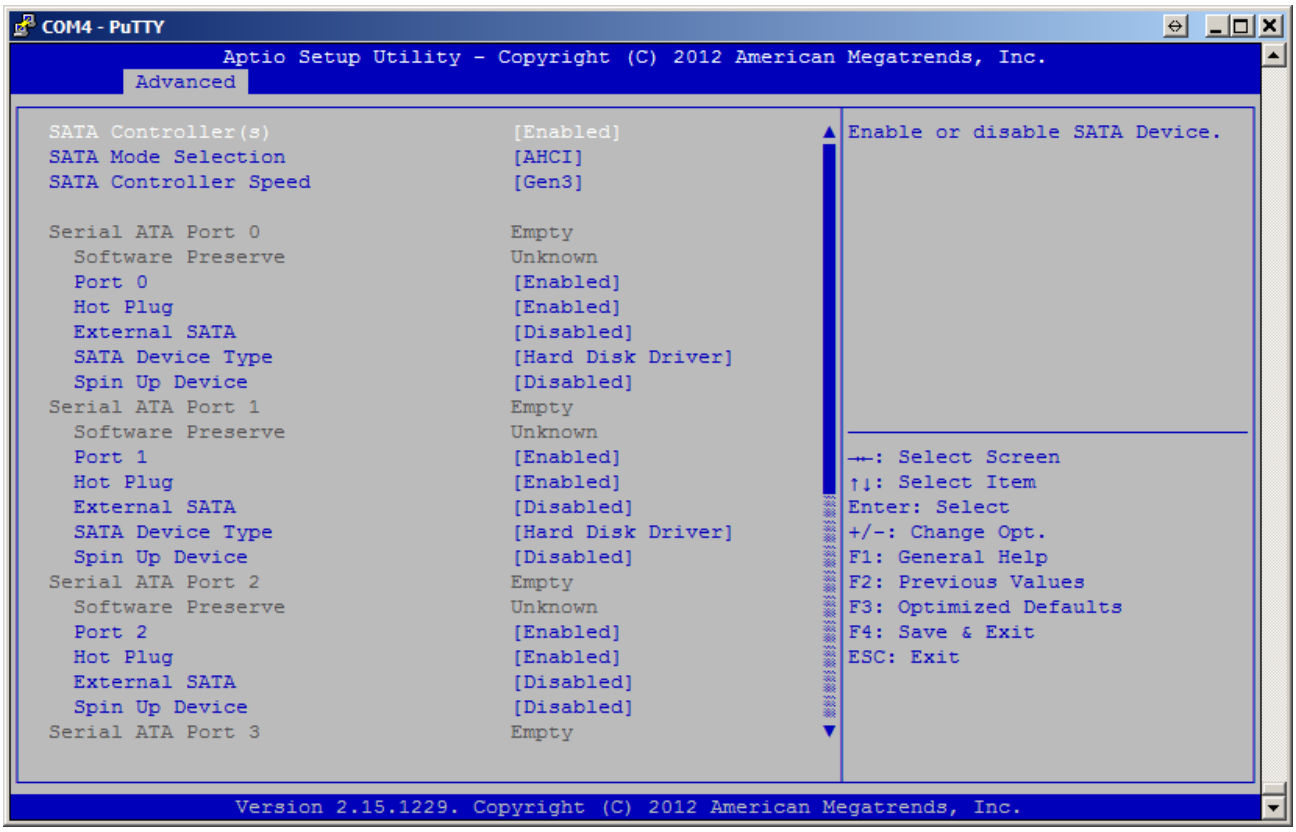


Fig.6-8: View of the "SATA configuration" menu tab

Function	Purpose	Default value
SATA Controllers(s) [**Enabled**/Disabled]	Possibility to disable the SATA-controllers.	**Enabled**
SATA Mode Selection [IDE/**AHCI**/RAID]	Mode of the SATA-controller.	**AHCI**
SATA Controller Speed	Operation mode of the SATA-controller.	**Gen3 ***
Serial ATA Port 0/1/2	Identifier of the connected device.	**-**
Software Preserve	Support of Software Preserve.	**-**
Port 0/1/2 [**Enabled**/Disabled]	Possibility to disable the port.	**Enabled**
Hot Plug	Support of the Hot Plug	**Enabled**
External SATA [Enabled/**Disabled**]	Possibility of connect SATA drives with a cable length up to 2 meters.	**Disabled**
SATA Device Type [**Hard Disk Driver**/Solid State Drive]	Type of the installed hard disk drive.	**Hard Disk Driver**
Spin Up Device	Function activating expectation of HDD spinning up to the operating mode.	**Disabled**

** Gen3 mode is supported only for 0 and 1 SATA ports.*

6.3.6 Thermal Configuration

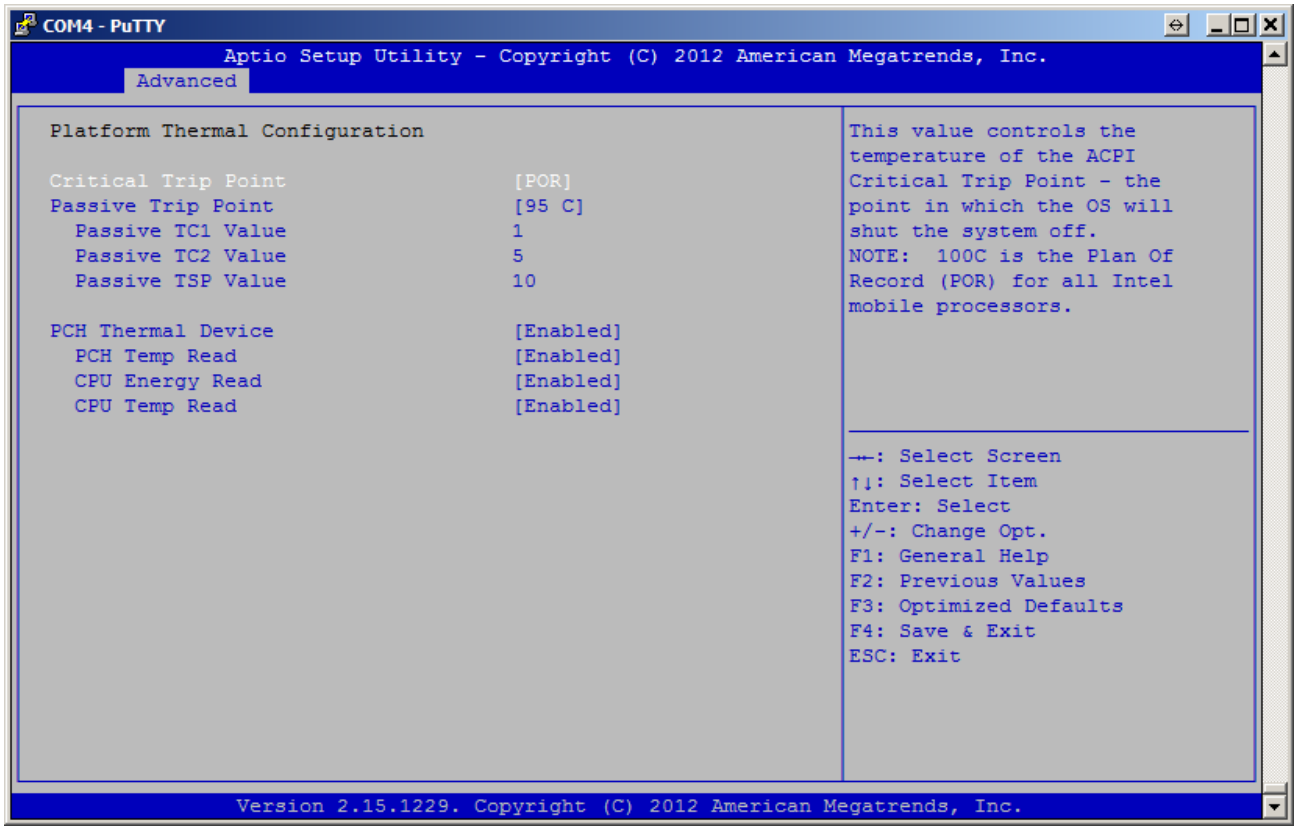


Fig.6-9: View of the "Thermal configuration" menu tab

Function	Purpose	Default value
Critical Trip Point [**POR**/15 C/23 C/31 C/39 C/47 C/55 C/63 C/71 C/79 C/87 C/95 C/103 C/111 C/119 C]	Temperature which, if reached, automatically disables operating system. POR=100° C.	**POR**
Passive Trip Point [Disabled/15 C/23 C/31 C/39 C/47 C/55 C/63 C/71 C/79 C/87 C/**95 C**/103 C/ 111 C/ 119 C]	Temperature, which if reached actuates CPU passive cooling circuit: Thermal Throttling.	**95 C**
Passive TC1 Value Passive TC2 Value Passive TSP	Description and calculation of values of TCxx values can be found in ACPI specification http://acpi.info/DOWNLOADS/ACPIspec40a.pdf.	**TC1=1** **TC2=5** **TSP=10**
PCH Thermal Device [**Enabled**/Disabled]	Enabling thermal sensors, integrated into system logic microchips.	**Enabled**
PCH Temp Read [**Enabled**/Disabled]	Activation of Southbridge sensor.	**Enabled**
CPU Energy Read [**Enabled**/Disabled]	Consumed power of CPU.	**Enabled**
CPU Temp Read [**Enabled**/Disabled]	CPU temperature.	**Enabled**

6.3.7 USB Configuration

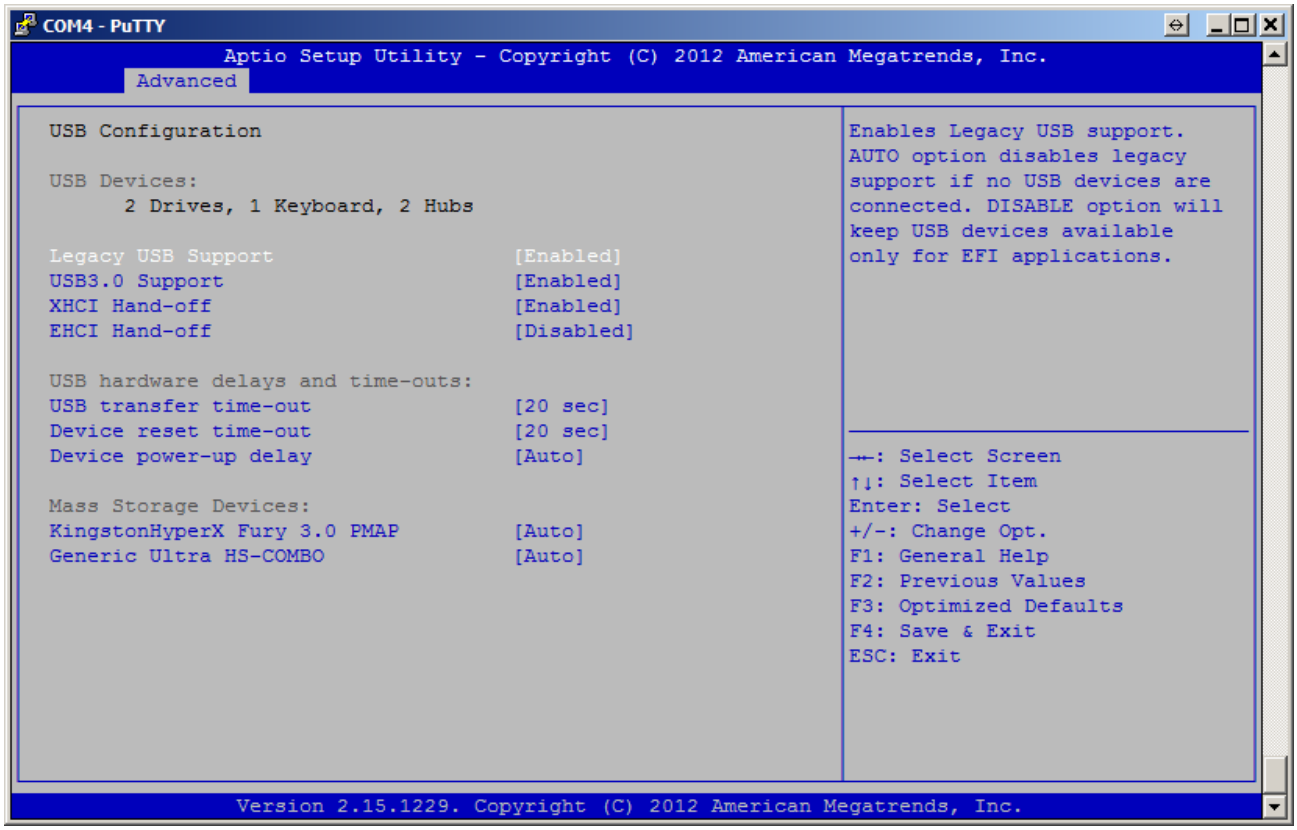


Fig.6-10: View of the "USB configuration" menu tab

Function	Purpose	Default value
Legacy USB support [**Enabled**/Disabled/Auto]	Support of USB for legacy operating systems. Auto – disables support of legacy USB, if there are no connected USB devices.	**Enabled**
USB Devices: 2 Drives, 1 Keyboard, 2 Hubs	USB devices: 2 drives, 1 keyboard, 2 hubs	-
USB 3.0 Support	USB 3.0 Support	**Enabled**
XHCI Hand-off [Disabled/**Enabled**]	Mechanism for control of two and more USB 3. 0 devices.	**Enabled**
EHCI Hand-off [**Disabled**/Enabled]	Mechanism for control of two and more USB 2.0 devices For XP SP2 and above should be disabled.	**Disabled**
USB hardware delays and time-outs	Delays of operation of the stack of USB protocols.	-
USB transfer time-out [1 sec/5 sec/10 sec/**20 sec**]	Maximum available timeout with USB transactions.	**20 sec**
Device reset time-out [10 sec/**20 sec**/30 sec/40 sec]	Maximum available timeout of USB device response after reset.	**20 sec**
Device power-up delay[**Auto**/Manual]	Readiness time of USB device after power supply.	**Auto**
USB Mass Storage Driver Support	Support of USB data storage devices.	**Enabled**

6.3.8 LM87 Device Configuration

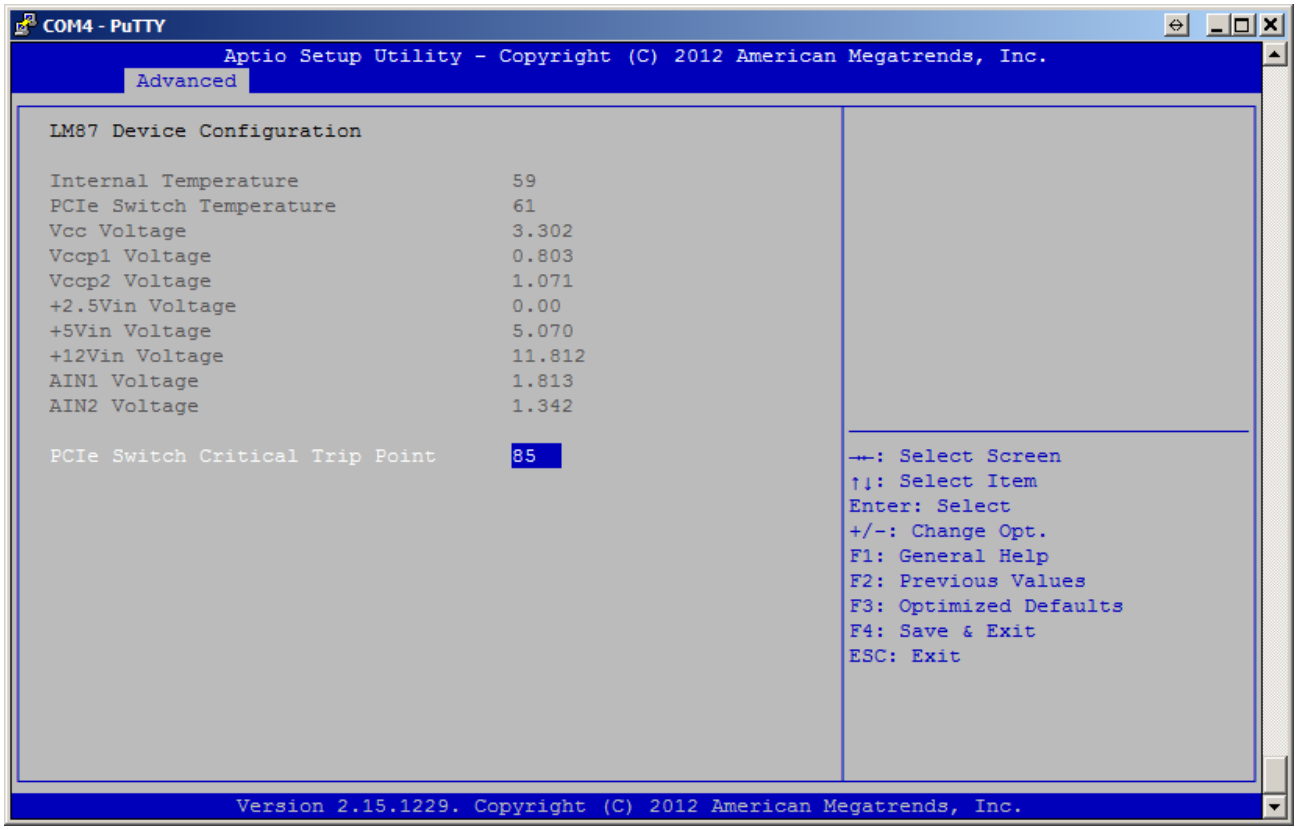


Fig.6-11: View of the "LM87 Device" menu tab

6.3.9 Super IO Configuration

The "Serial port IO Configuration" menu is available when MIC584 is installed.

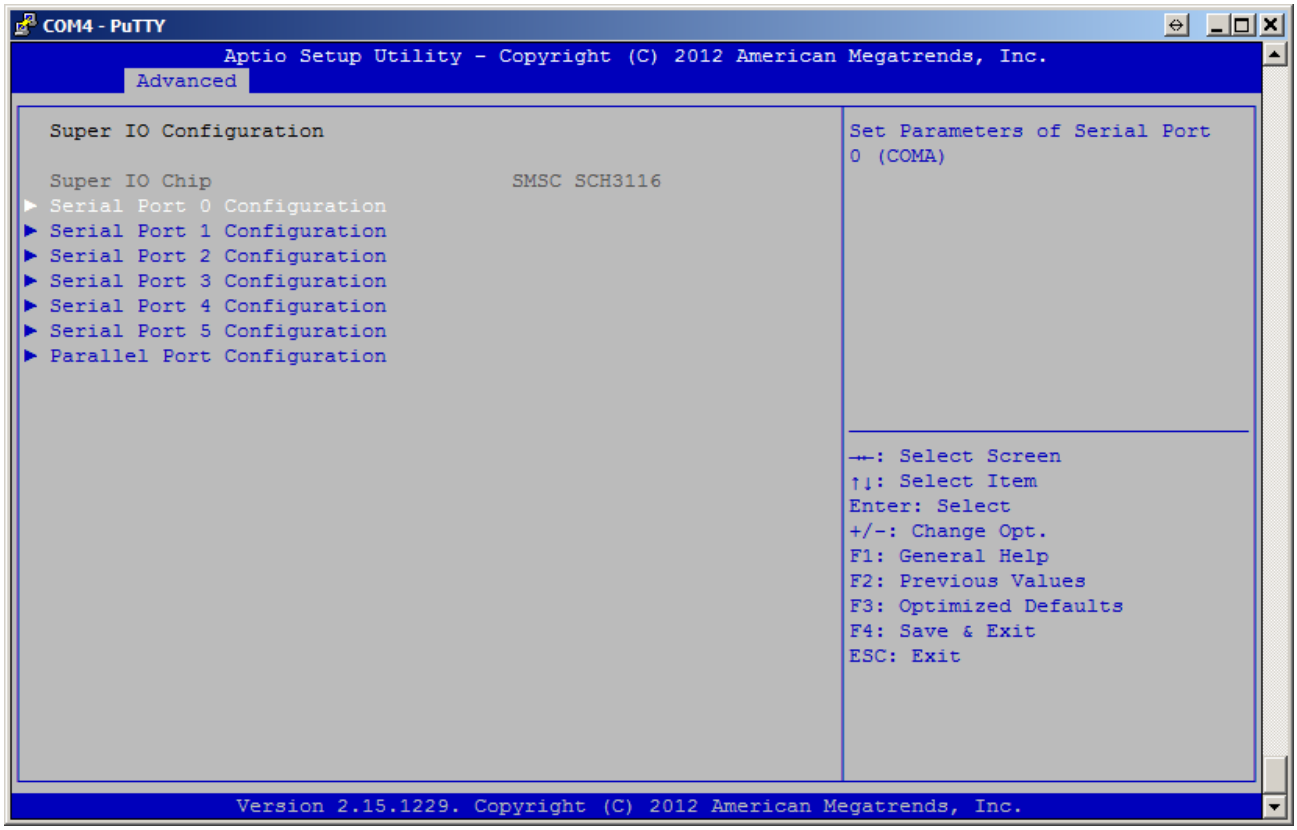


Fig.6-12: View of the "Super IO Configuration" menu tab

Function	Purpose	Default value
Super IO Chip	Super IO microchip.	**SMSC SCH3116**
Serial Port 0/1/2/3/4/5 Configuration	Configuration of serial ports 0/1/2/3/4/5.	-
Parallel Port Configuration	Parallel port configuration	-

Serial port XX configuration:

Fig.6-13: View of the " Serial port XX configuration" menu tab

Function	Purpose	Default value
Serial port [**Enabled**/Disabled]	Possibility to disable serial port.	**Enabled**
Change settings	Selection of available resources for serial port.	-
Device mode[**Standard**/IrDA Mode/ASK-IR Mode]	Mode of serial port operation.	**Standard**

Parallel Port Configuration:

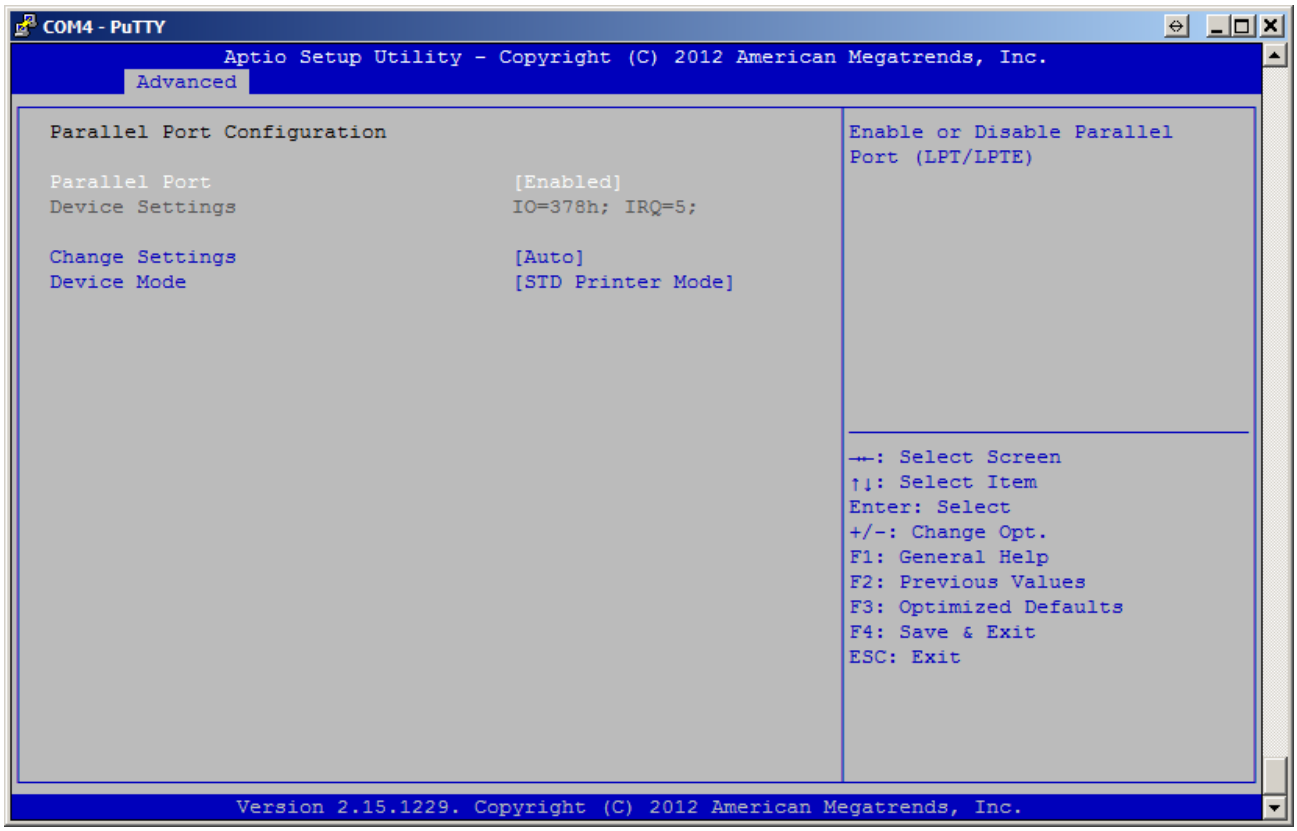


Fig.6-14: View of the "Parallel port configuration" menu tab

Function	Purpose	Default value
Parallel port [**Enabled**/Disabled]	Possibility to disable serial port.	**Enabled**
Change settings	Selection of available resources for serial port.	-
Device mode [**STD Printer Mode**/ SPP Mode/ EPP-1.9 and SPP Mode/ EPP-1.7 and SPP Mode/ECP Mode/ECP and EPP 1.9 Mode/ECP and EPP 1.7 Mode]	Mode of serial port operation.	**STD Printer Mode**

6.3.10 Serial port console redirection

The "Serial port console redirection" menu is available when MIC584 is installed.

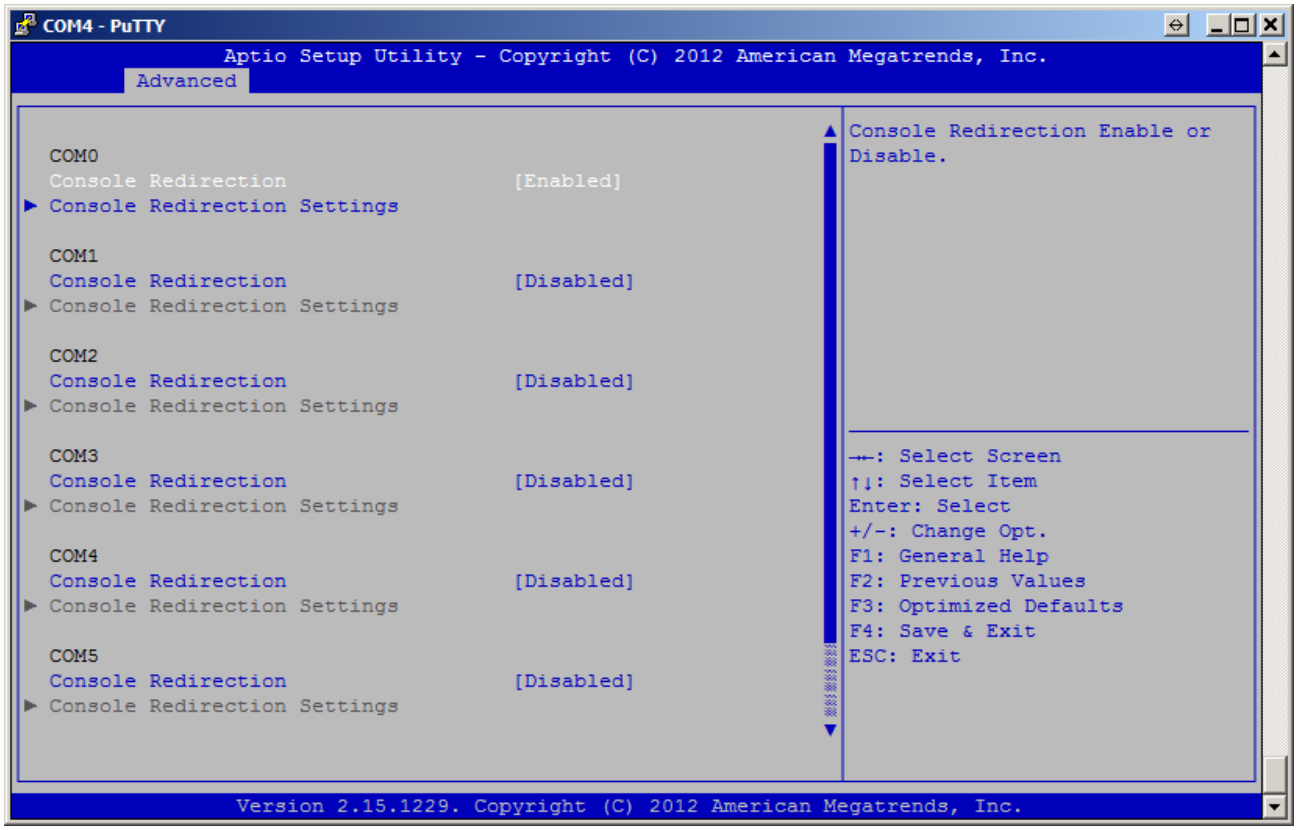


Fig.6-15: View of the "Serial port console redirection" menu tab

Function	Purpose	Default value
COM 0/1/2/3/4/5	COM-port 0/1/2/3/4/5.	-
Console Redirection [**Enabled**/Disabled]	Possibility to disable Console Redirection.	**Enabled**
Console Redirection Settings	Console Redirection	-

6.3.10.1 Console Redirection Settings

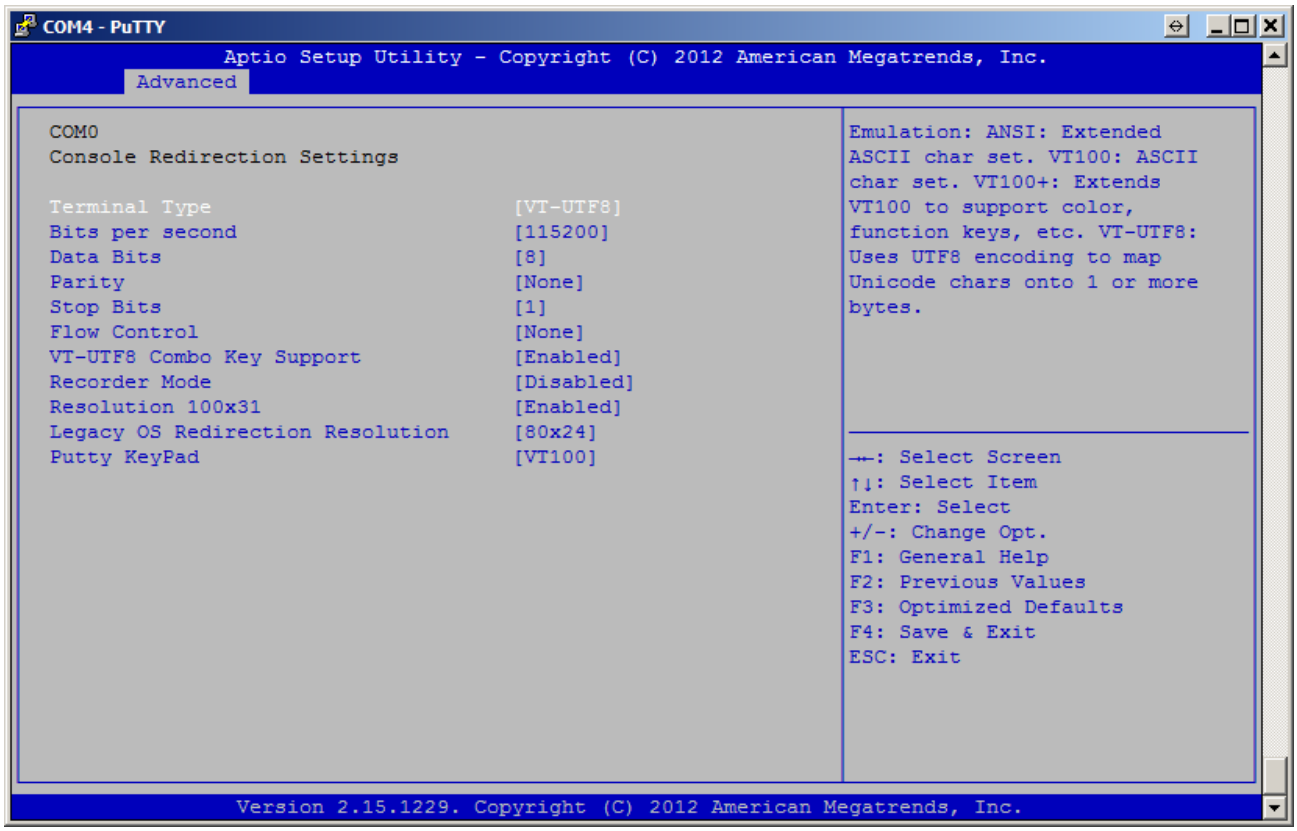


Fig.6-16: View of the "Console Redirection Settings" menu tab

Function	Purpose	Default value
Terminal type[VT100/VT100+/**VT-UTF8**/ANSI]	Type of terminal	**VT-UTF8**
Bits per second [9600/19200/38400/57600/**115200**]	Speed of serial port.	**115200**
Data bits[7/8]	Number of data bits.	**8**
Parity[None/Even/Odd/Mark/Space]	Parity check during data exchange.	**None**
Stop bits[1/2]	Number of stop bits.	**1**
Flow Control[None/"Hardware RTS/CTS"]	Flow control by way of additional signals.	**None**
Recorder Mode[**Disabled**/Enabled]	Transmission of text data only.	**Disabled**
Resolution 100x31[Disabled/**Enabled**]	Installation of extended resolution.	**Enabled**
Legacy OS Redirection Resolution [**80x24**/80x25]	Number of lines and columns at image output.	**80 x 24**
Putty KeyPad	Keyboard type in the Putty terminal	**VT100**

6.3.11 CPU PPM Configuration

CPU PPM Configuration – configuration of CPU energy efficiency modes

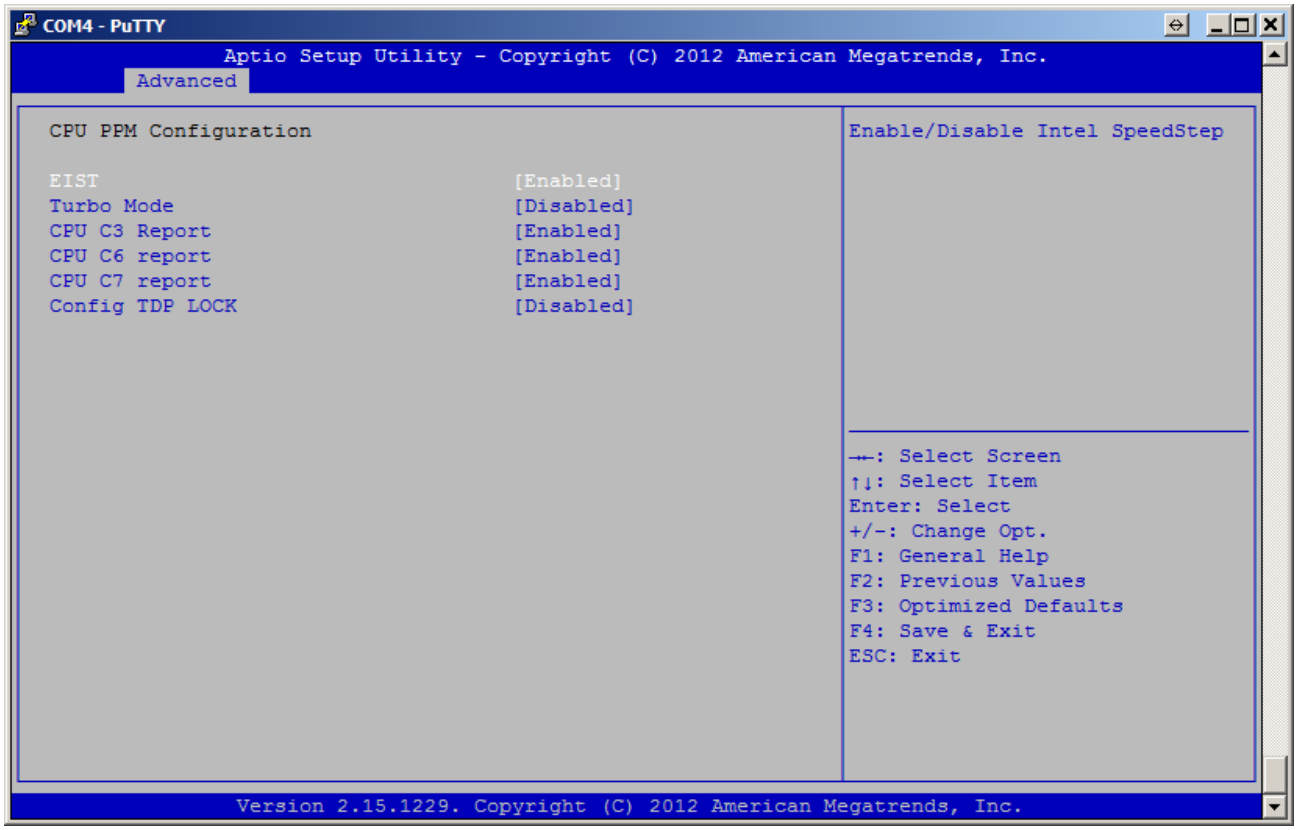


Fig.6-17: View of the "CPU PPM Configuration" menu tab

Function	Purpose	Default value
EIST	Setting of the Enhanced Intel SpeedStep Technology	**Enabled**
Turbo Mode	Turbo mode of CPU	**Disabled**
CPU C3 Report	Power efficiency mode C3	**Enabled**
CPU C6 Report	Power efficiency mode C6	**Enabled**
CPU C7 Report	Power efficiency mode C7	**Enabled**
Config TDP LOCK	Restriction to change TDP settings.	**Disabled**

6.4 Chipset

"Chipset" – configuration of logics system components.

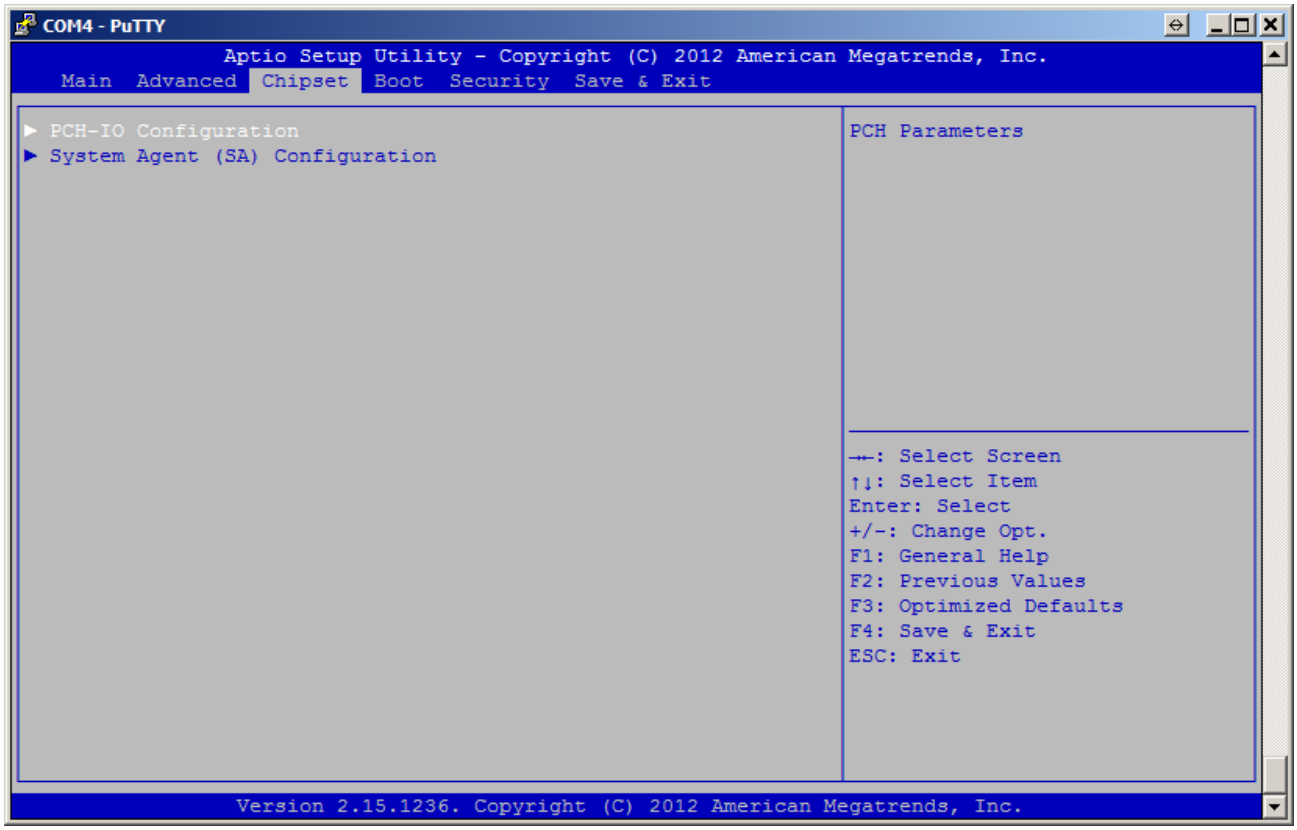


Fig.6-18: View of the "Chipset" menu tab

6.4.1 System Agent (SA) configuration

System Agent (SA) configuration – memory and graphics subsystem configuration.

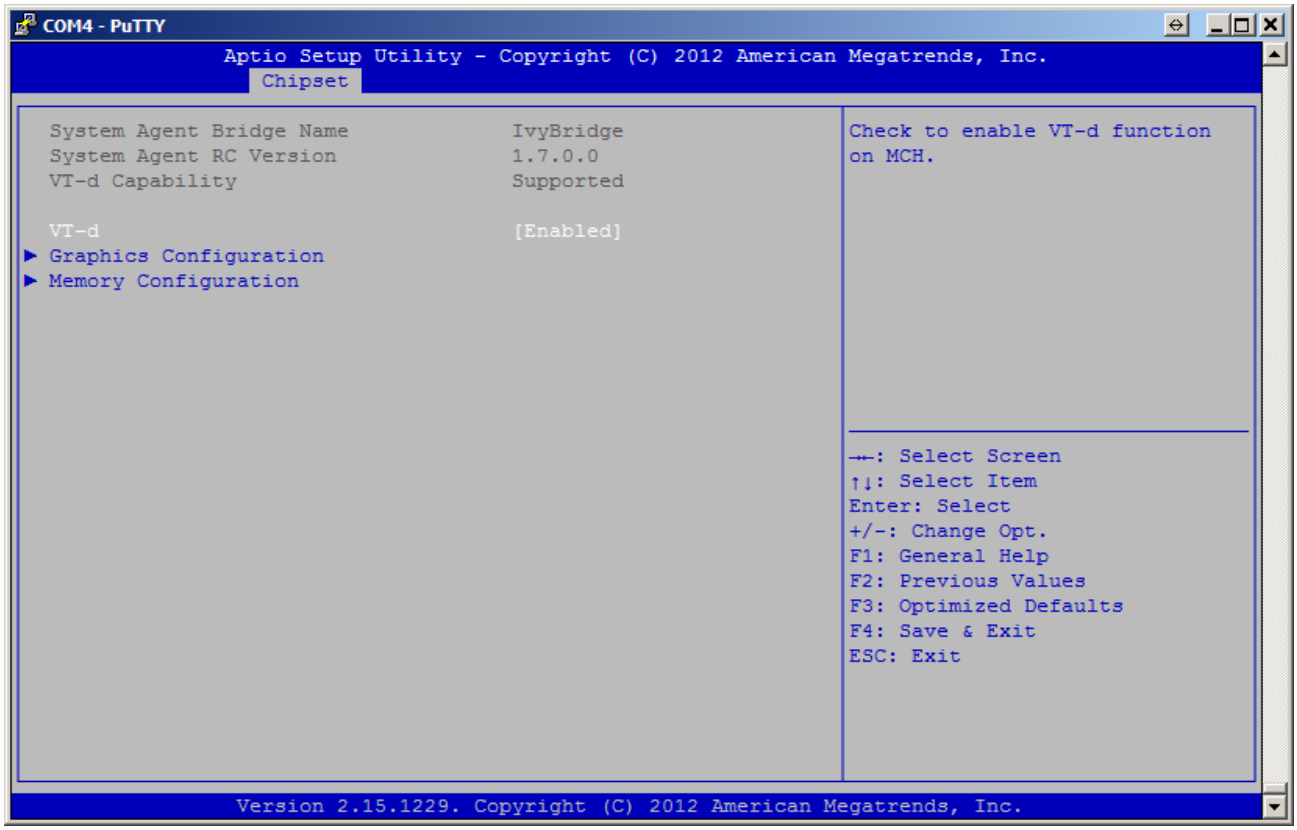


Fig.6-19: View of the "System Agent (SA) configuration" menu tab

Function	Purpose	Default value
System Agent Bridge Name	Name	**IvyBridge**
System Agent RC Version	Version.	**1.7.0.0**
VT-d Capability	Support of VT-d technology.	**Supported**
VT-d [**Enabled**/Disabled]	Verification of VT-d technology support.	**Enabled**

6.4.1.1 Graphics Configuration

Graphics subsystem configuration.

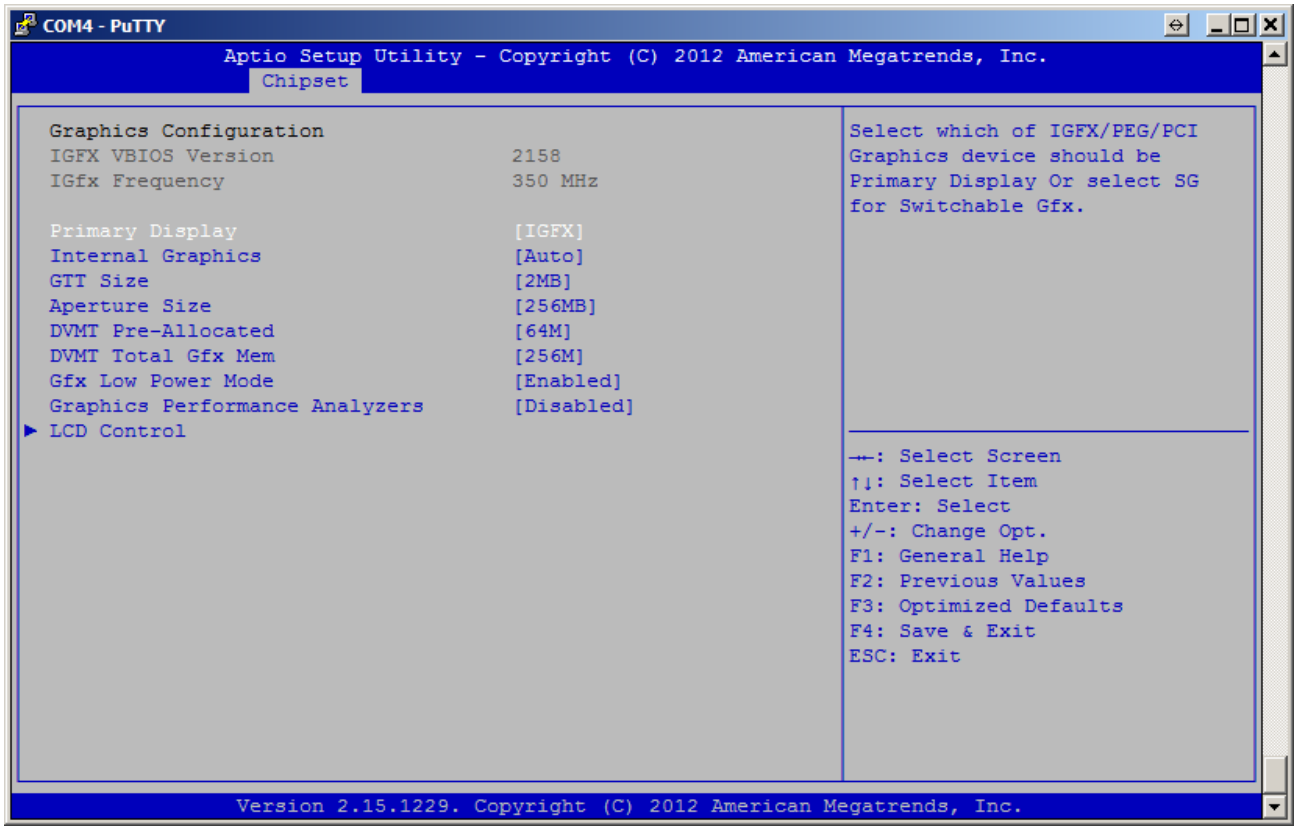


Fig.6-20: View of the "Graphics Configuration" menu tab

Function	Purpose	Default value
Primary Display [Auto/**IGFX**/PEG/PCI/SG]	Selection of the primary graphics card within the system. IGFX – integrated into CPU, PEG/PCI – external graphics devices with PCI or PCI Express bus.	**IGFX**
Internal Graphics [**Auto**/Disabled/Enabled]	Possibility of disabling of the CPU-integrated graphics card. Auto – graphics card is disabled only at switched-on display.	**Auto**
GTT Size[1MB/**2MB**]	Size of the RAM window for direct access by graphics card.	**2 MB**
Aperture Size [128MB/**256MB**/512MB]	Size of RAM, reserved for graphics memory.	**256MB**
DVMT Pre-Allocated [0MB/32MB/**64MB**/96MB/128MB/ 160MB/192MB/224MB/256MB/288MB/ 320MB/352MB/384MB/416MB/ 448MB/480MB/512MB]	Minimum reserved volume of RAM, required for operation of graphics subsystem.	**64 MB**

DVMT total Gfx Mem[128M/**256M**/MAX]-	Maximum available memory capacity used by the video subsystem driver.	**256M**
Gfx Low Power Mode[**Enabled**/Disabled]-	Reducing heat dissipation of the graphics engine due to decline in performance.	**Enabled**

LCD Control – settings of LVDS displays

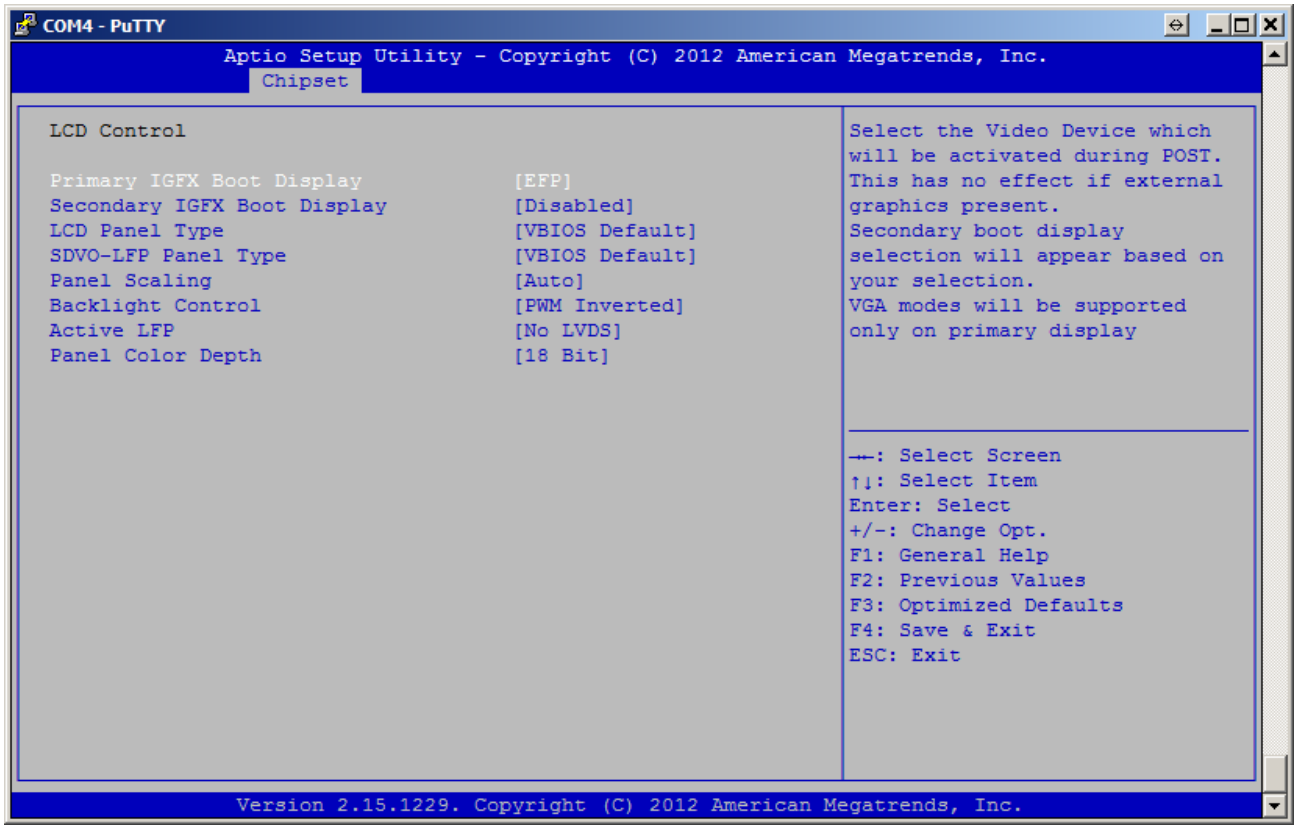


Fig.6-21: View of the "LCD Control" menu tab

Function	Purpose	Default value
Primary IGFX Boot Display [**VBIOS Default**/CRT/EFP/LFP/ EFP3/EF{2/LFP2]	Primary video display unit BIOS POST.	**VBIOS Default**
Secondary IGFX Boot Display	Secondary graphics adapter.	**Disabled**
LCD Panel Type [640x480/800x600/1024x768/ 1280x1024/1400x1050/1600x1200/1366x768/ 1680x1050/1920x1200/1440x900/ 1920x1080/2048x1536]	Resolution of the pluggable panel	**VBIOS Default**
SDVO-LFP Panel Type	Type of the SDVO-LFP Panel.	**VBIOS Default**
Panel Scaling [**Auto**/Off/Force Scaling]	Scaling mode.	**Auto**
Backlight Control	Backlight Control	**PWM Inverted**
Active LFP [**No LVDS**/Int-LVDS/SDVO LVDS/eDP Port-A/ eDP Port-D]	Type of LVDS display connection.	**No LVDS**
Panel Color Depth [**18 bit**/24bit]	Color depth of the display.	**18 bit**

6.4.1.2 Memory Configuration

Memory configuration - information and memory configurations.

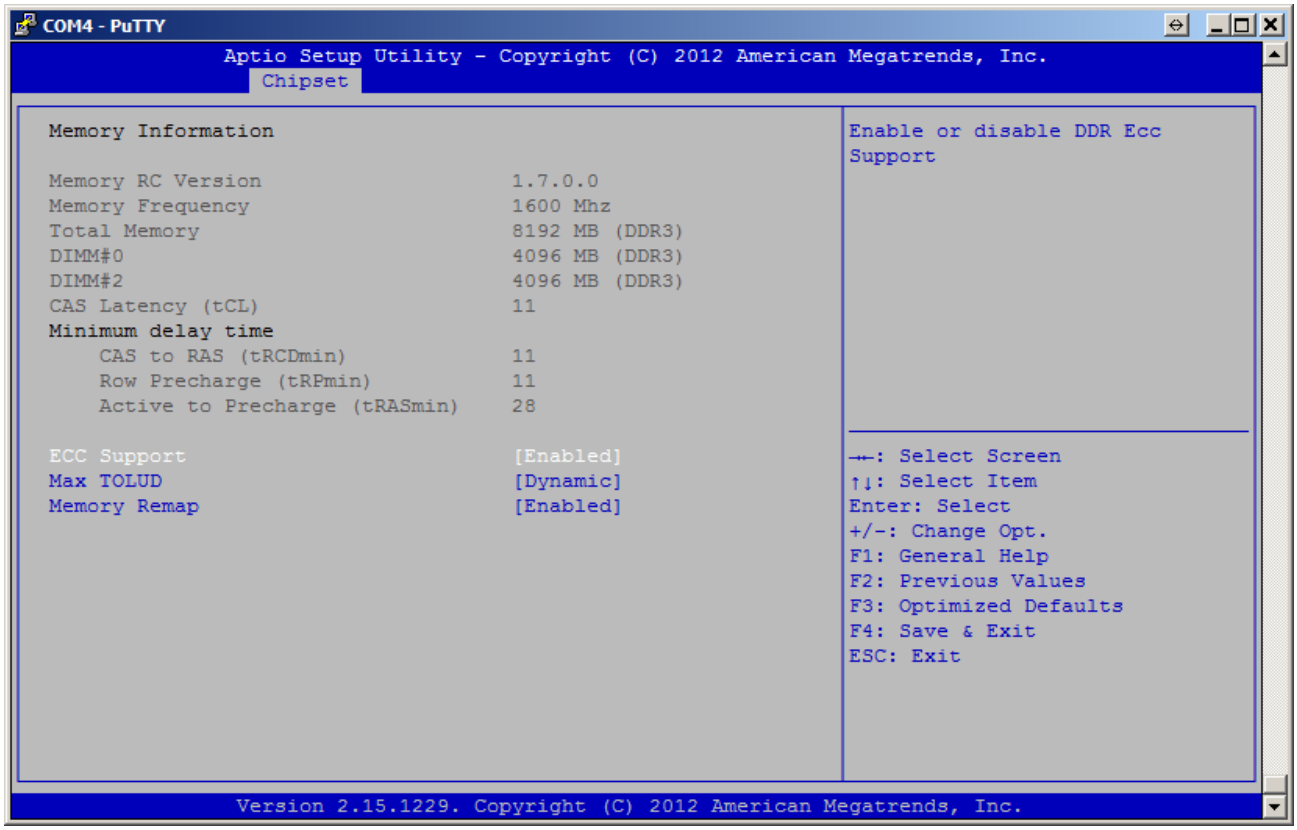


Fig.6-22: View of the "Memory Configuration" menu tab

Function	Purpose	Default value
Memory RC Version	Version.	**1.7.0.0**
Memory Frequency	Frequency	**1600 MHz**
Total Memory	Total Memory	**8192 MB (DDR3)**
DIMM# 0/2	Location and size of the memory installed.	**4096 MB**
CAS Latency (tCL)	Delay in cycles between CAS signal generation and start of data reading.	**11**
Minimum delay time	Minimum delay time	**-**
CAS to RAS (tRCDmin)	Delay time between CAS and RAS signals.	**11**
Row Precharge (tRPmin)	Number of cycles for repeated generation of RAS signal.	**11**
Active to Precharge (tRASmin)	Number of cycles for closing and opening of the same memory bank.	**28**

ECC Support [**Enabled**/Disabled]	Enabling ECC mode.	**Enabled**
Max TOLUD [**Dynamic**/1GB/1.25GB/1.5GB/ 1.75GB/2GB/2.25GB/2.5GB/2.75GB/ 3GB/3.25GB]	Possibility to choose the RAM upper limit.	**Dynamic**
Memory Remap [**Enabled**/Disabled]	Needs to be enabled, if 4 GB or more RAM is installed.	**Enabled**

6.4.2 PCH-IO Configuration

PCH-IO configuration – SouthBridge configuration.

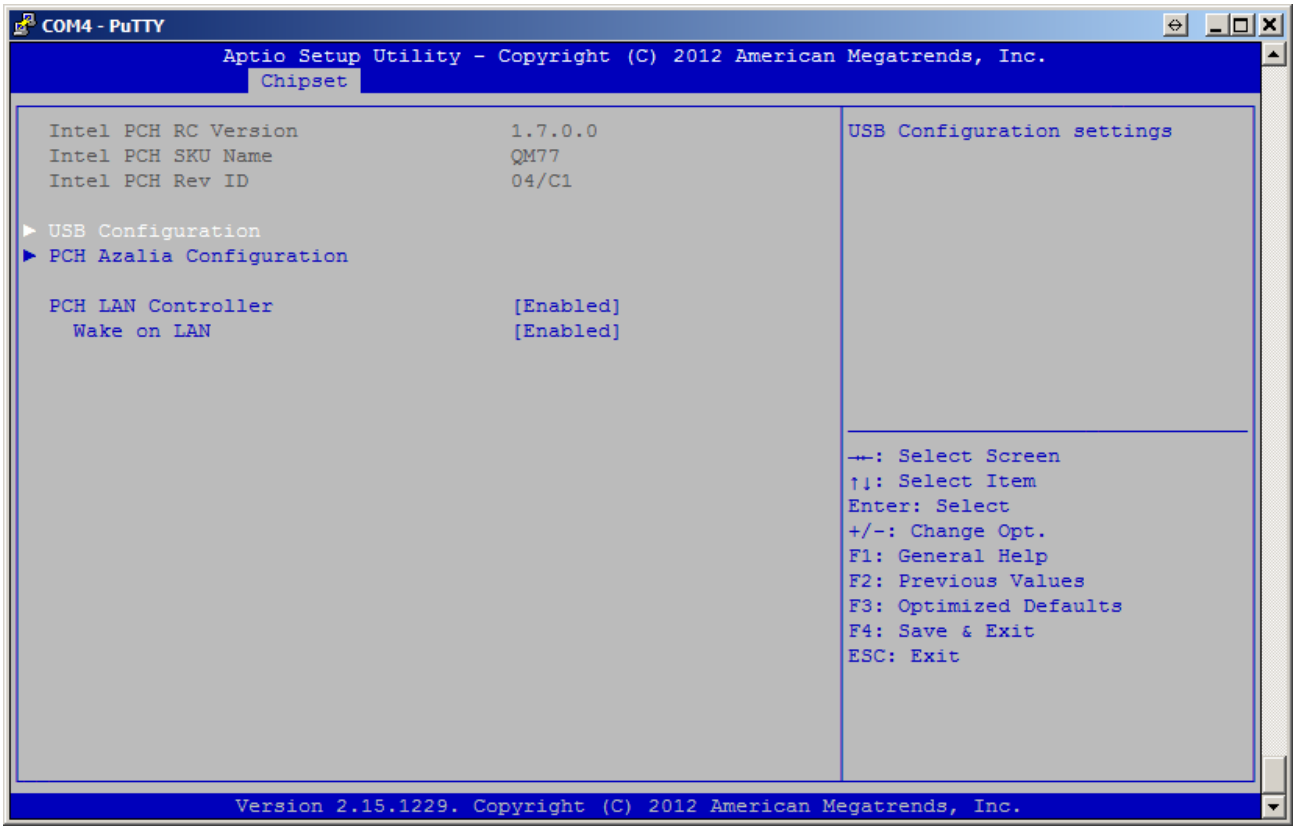


Fig.6-23: View of the "PCH-IO Configuration" menu tab

Function	Purpose	Default value
USB Configuration	USB configuration.	-
PCH Azalia Configuration	Audio codec configuration	-
PCH LAN Controller	Network adapter integrated into the PCH south bridge.	**Enabled**
Wake on LAN	Activation of Wake on LAN function.	**Enabled**

6.4.2.1 PCH Azalia Configuration

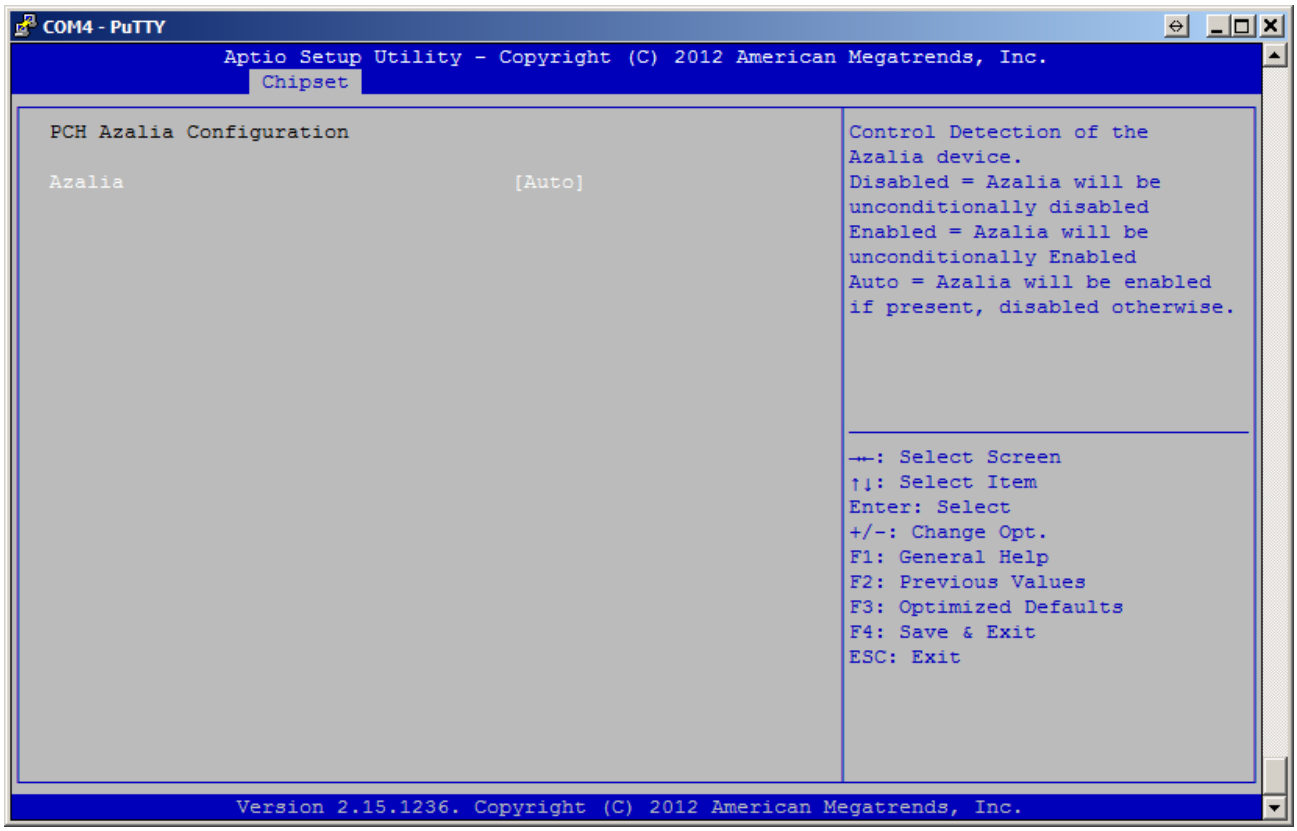


Fig.6-24: View of the "PCH Azalia Configuration" menu tab

Function	Purpose	Default value
Azalia [**Auto**/Enabled/Disabled]	Possibility to deactivate audio codec in MIC584.	**Auto**

6.4.2.2 USB Configuration

USB interface configurations

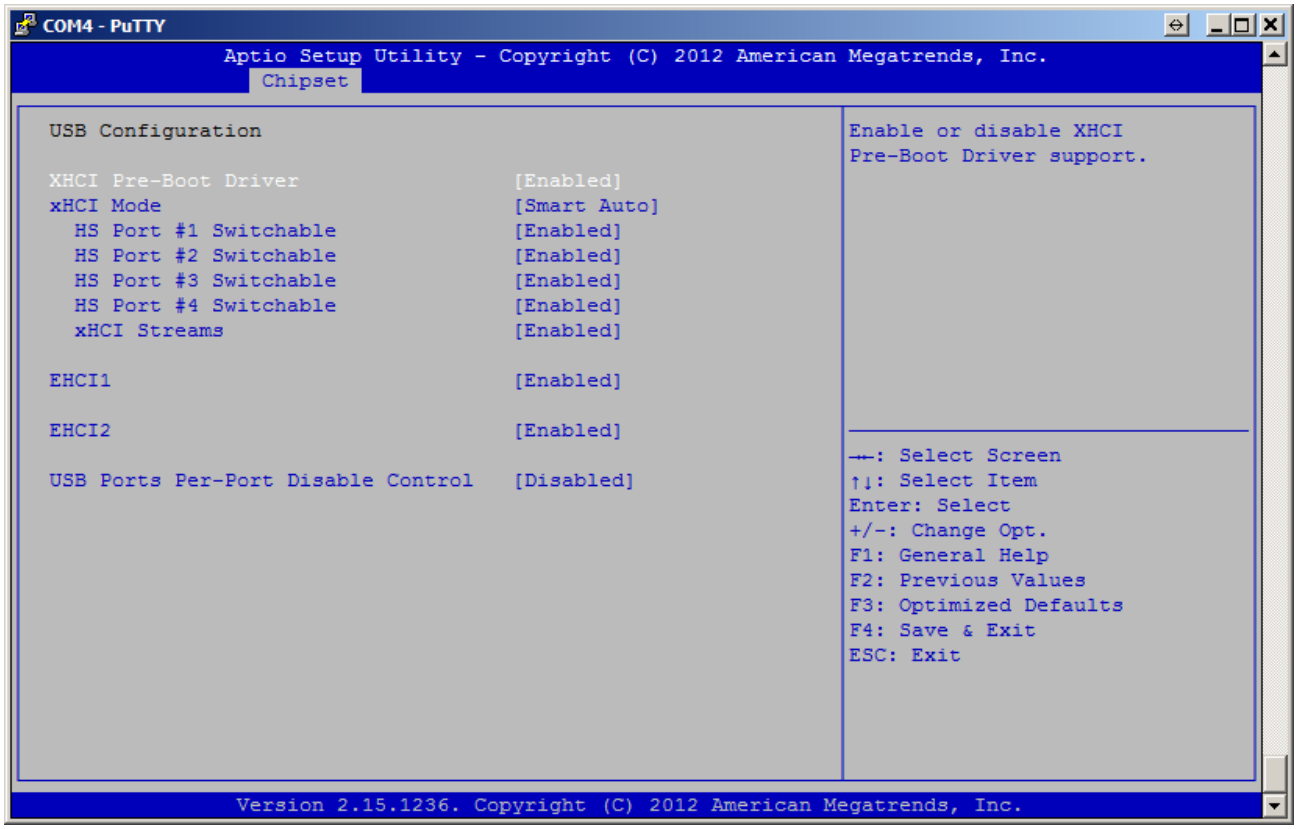


Fig.6-25: View of the "USB configuration" menu tab

Function	Purpose	Default value
XHCI Pre-Boot Driver	Support of USB 3.0 to BIOS level.	**Enabled**
xHCI Mode	Mode of USB 3.0 operation in BIOS: Disabled: All the ports in USB 2.0 mode. Enabled: All the ports in USB 3.0 modes – support of the driver on the side of operating system is required. Auto – USB 2.0 mode at BIOS stage, then USB 3.0 in case of support in the operating system driver. Smart Auto – USB 2.0 mode during cold start. If operating system has USB 3.0 support, the	**Smart Auto**
HS Port #1/2/3/4 Switchable	Individual switching of ports from USB 3.0 mode to USB 2.0 mode.	**Enabled**

xHCI Streams	Support of additional buffering for high-speed USB 3.0 drives.	**Enabled**
EHCI1 [**Enabled**/Disabled]	Possibility to disable the EHCI1 controller.	**Enabled**
EHCI2 [**Enabled**/Disabled]	Possibility to disable the EHCI2 controller.	**Enabled**
USB Ports Per-Port Disable Control [**Disabled**/.Enabled]	Possibility to individually disable USB ports.	**Disabled**

6.5 Boot

Tab for configuration of module boot devices. View of this tab menu is shown in the figure below.

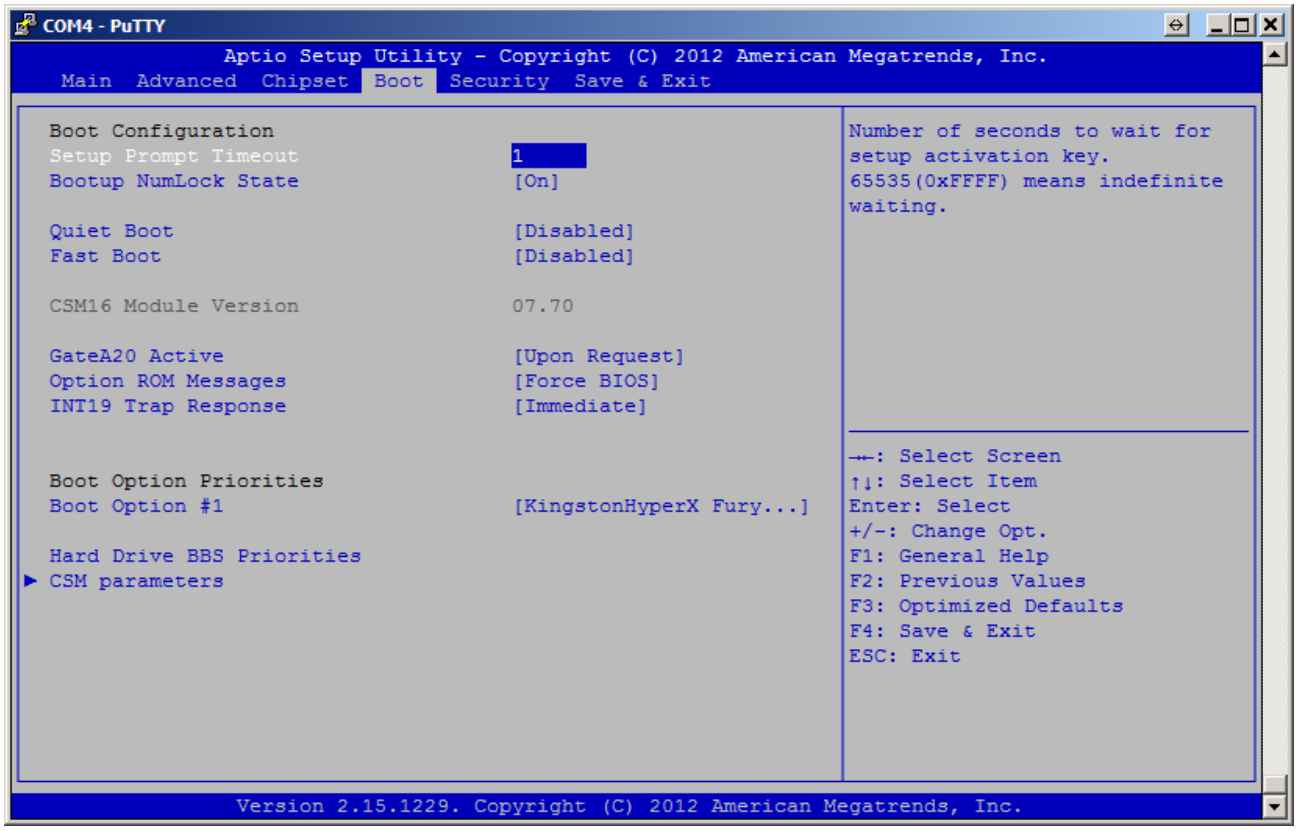


Fig. 6-26: View of "Boot" menu tab

6.5.1 Boot Configuration

This menu item enables you to set separate system properties.

6.5.1.1 Setup Prompt Timeout

Assign the number of seconds for activation waiting. Value 65535 (0XFFFF) means an indefinite wating time.

6.5.1.2 Bootup NumLock State

Setting this value enables to change configuration of the "Number Lock" during booting process. "On" will be an optimal default setting

Option	Description
Off	This option prohibits an automatic mode of "Number Lock" keyboard. In order to use keyboard numeric characters, press the "Number Lock" key, located in the left upper corner of the keyboard digital panel. The "Number Lock" LED on the keyboard is on when the "Number Lock" key is pressed.
On	Use of this parameter enables the "Number Lock" mode on the keyboard automatically during system booting. This enables to directly use digital panel, located in the right part of the keyboard. "Number Lock" LED on the keyboard will be on. This parameter value is a default value.

6.5.1.3 Quiet Boot

Assigning this value makes it possible to change the nature of screen messages during the booting process. An optimal and default parameter is "Disabled".

Option	Description
Disabled	Choose this parameter value to allow the system to give POST messages. This parameter value is a default value.
Enabled	Choose this parameter value to allow the system to give “OEM logo” messages.

6.5.1.4 Fast Boot

Activation of this mode enables speed up the BIOS boot process by skipping initialization of some of the hardware. An optimal and default parameter is "Disabled".

Option	Description
Disabled	Choose this parameter value to disable the Fast Boot mode.
Enabled	Choose this parameter value to speed up the BIOS boot process by skipping initialization of some of the hardware.

6.5.1.5 GateA20 Active

"GateA20 Active" - control of A20 gate.

Option	Description
Upon Request	Upon request: GA20 can be prohibited when BIOS services are in use.
Always	Prohibition of GA20 is not allowed, this option is used when a code higher than 1 MB is executed.

6.5.1.6 Optional ROM Messages

Using this parameter enables displaying "Optional ROM" messages.

Option	Description
Force BIOS	Set this parameter value to allow the system to display "Optional ROM" messages.
Keep Current	Set this parameter value to prohibit the system to display "Optional ROM" messages.

6.5.1.7 INT19 Trap Response

"INT19 Trap Response" - control of Int 19h vector trapping

Option	Description
Immediate	Execute the trapped int 19h immediately.
Postponed	Execute during booting in the legacy mode.

6.5.2 Boot Option Priorities

This submenu item shows priorities of booting options. User can change the priorities by choosing a separate boot option. A boot option marked as #1 will have the highest priority, the next will be #2, then #3 etc.

6.5.3 Hard Drive BBS Priorities

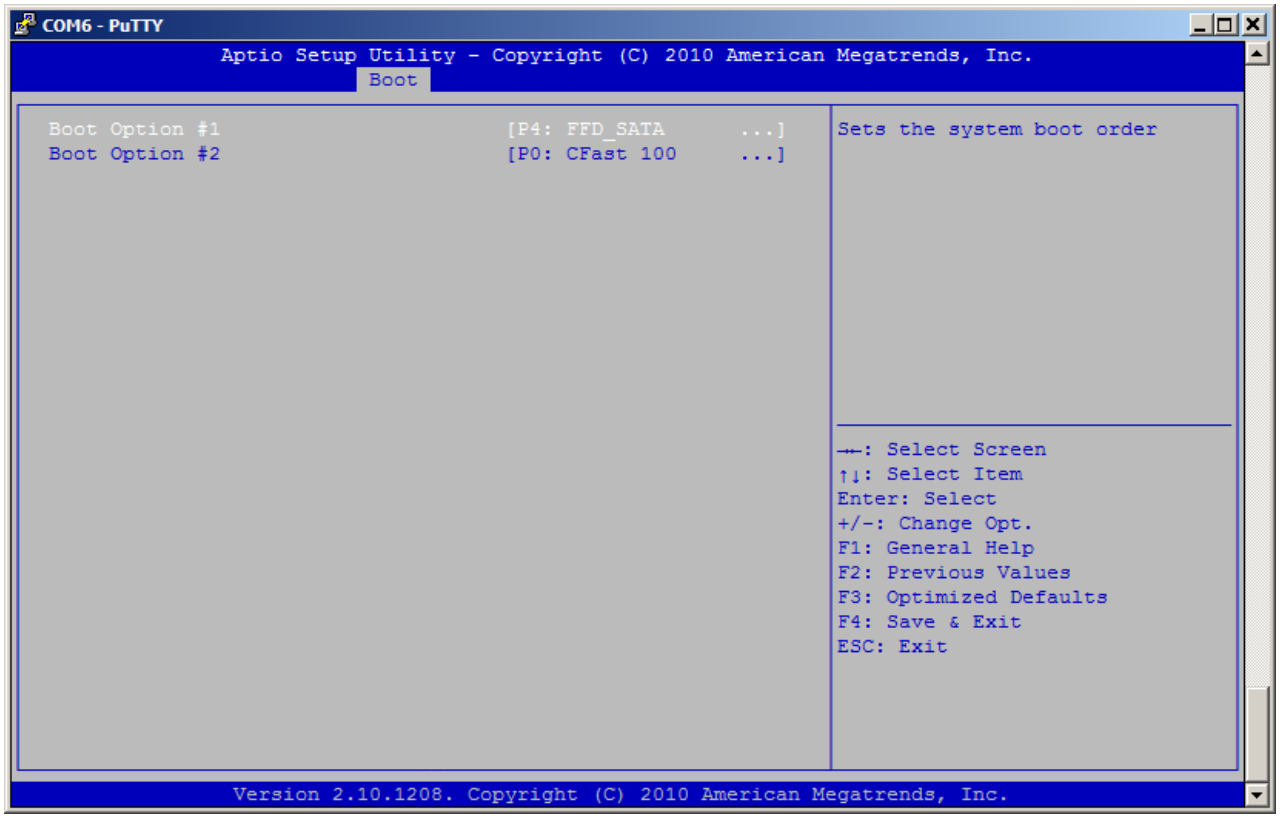


Fig. 6-27: View of the "Hard Drive BBS Priorities" menu tab

This menu item contains the list of devices for determination of the computer booting priority. Boot Option #1 has the highest priority

6.5.4 CSM parameters

This submenu is used for setting additional booting parameters.

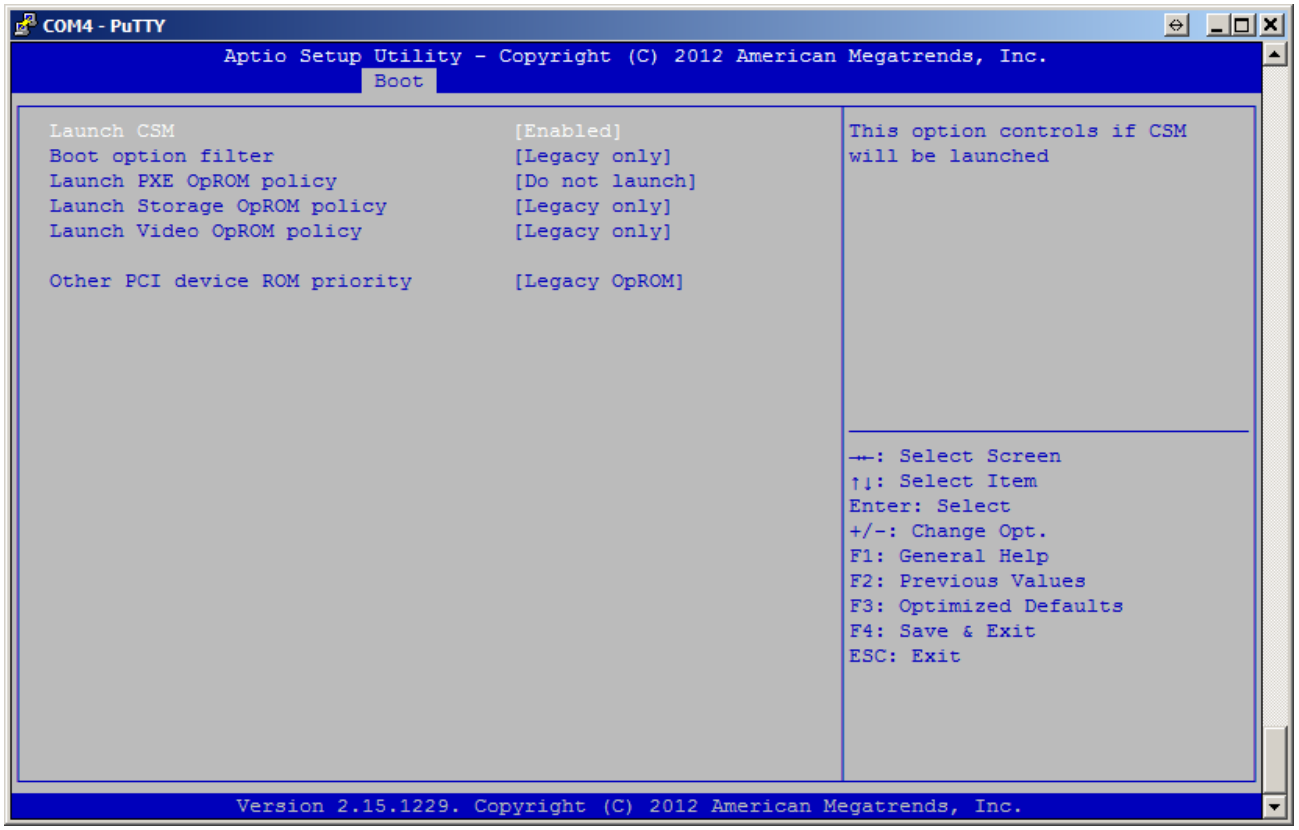


Fig. 6-28: View of the "CSM parameters" menu tab

Function	Purpose	Default value
Launch CSM	Activate compatibility with Legacy BIOS.	**Enabled**
Boot option filter	Supporting boot from UEFI carriers.	**Legacy only**
Launch PXE OpROM policy	Activation of network booting: UEFI or Legacy.	**Do not launch**
Launch Storage OpROM policy	Launching from PCI drives: UEFI or Legacy.	**Legacy only**
Launch Video OpROM policy	Support of UEFI graphics cards: UEFI or Legacy.	**Legacy only**
Other PCI device ROM priority	Initializing OpROM of the installed extension boards: UEFI or Legacy.	**Legacy OpROM**

6.6 Security

This tab is designed for configuration of module protection functions.

6.6.1 Setting password

Two security levels of the password

"Security" settings allow Administrator and User password. If you use both passwords, the Administrator password should be assigned first.

The system should be configured in such a way that all the users could enter password each time the system boots or during "Setup" procedure, using either Administrator or User password.

Administrator and User passwords could have two password protection levels.

If you selected "Password" sub-menu, a message appears that invites you to assign a password from 3 to 20 characters long. Type the password using your keyboard. The password will not be displayed while you're typing. Confirm the password below. If you forget the password, you'll have to reset all BIOS configurations.

6.6.2 Security Setup

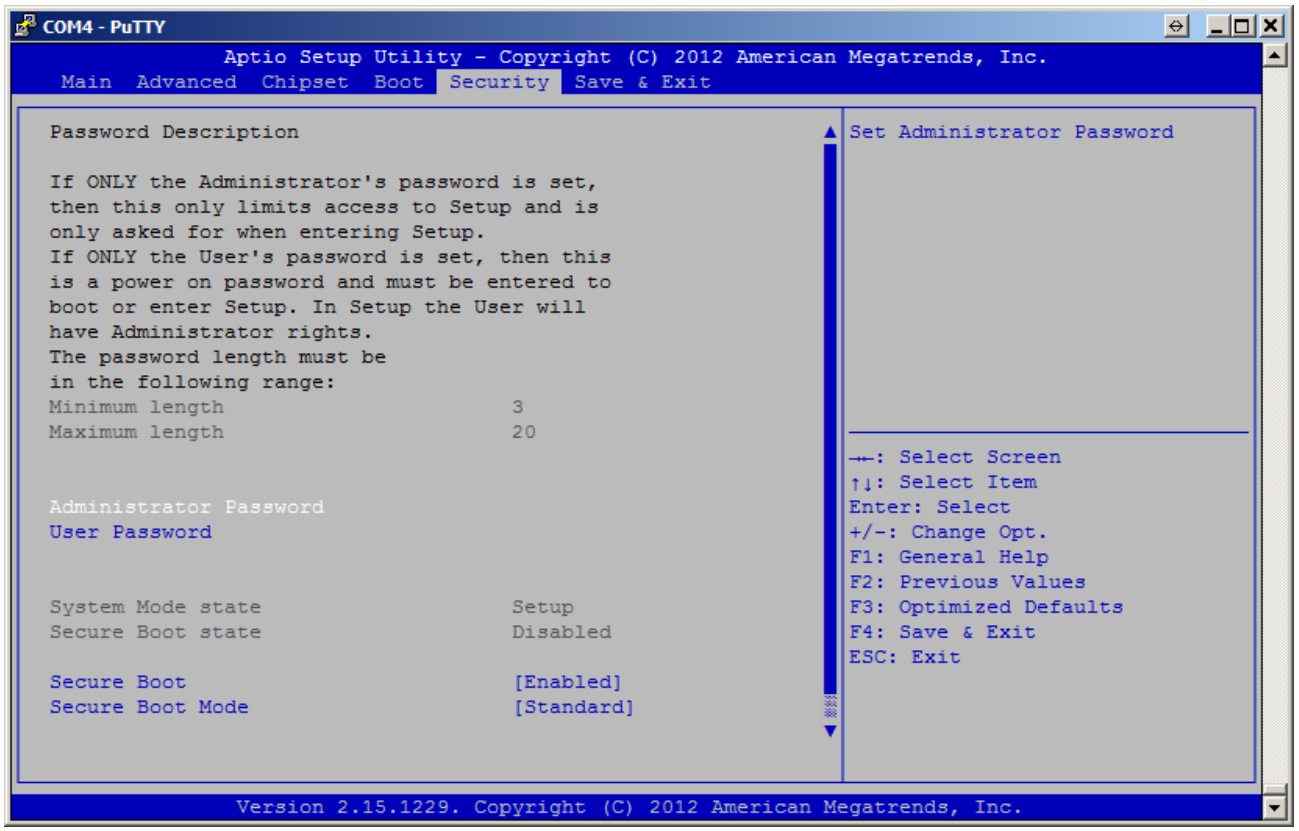


Fig. 6-29: View of "Security" menu tab

Option	Description
Administrator Password	This option enables to set Administrator password for BIOS.
User Password	This option enables to set User password for BIOS.

Function	Purpose	Default value
Minimum Length	Minimum amount of symbols.	**3**
Maximum Length	Maximum amount of symbols.	**20**
Secure Boot	Secure boot protocol.	**Enabled**
Secure Boot Mode	Configuration of the mode operation of the Secure Boot protocol.	**Standard**

6.7 Save & Exit

Tab of the parameters for exiting the BIOS Setup program. View of this menu tab is shown in the figure below.

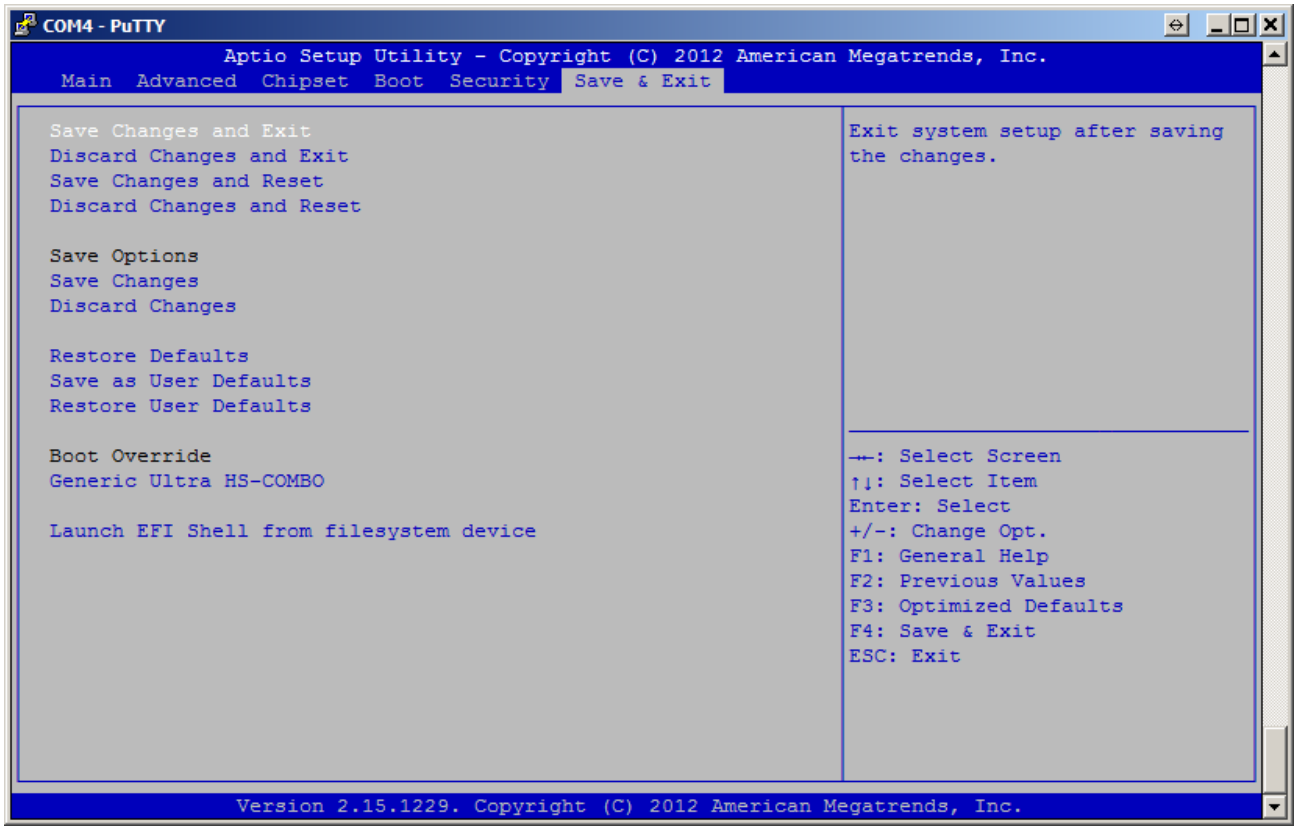
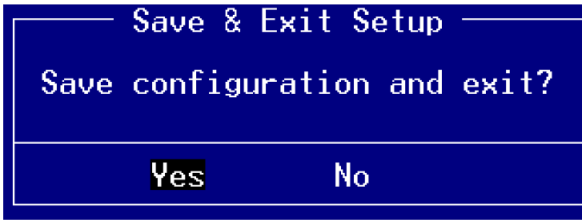


Fig. 6-30: View of the "Save & Exit" menu tab

6.7.1 Save Changes and Exit

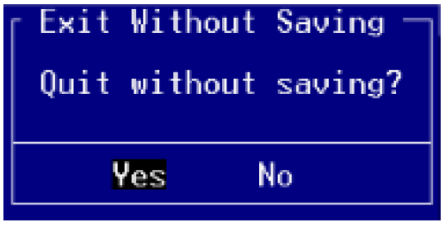
When you made changes in the system, choose this option for saving changes and exiting the AptioTM TSE to ensure these changes to be used in the future. The next window will appear after you choose the "Save Changes and Reset" option:



Choose "Yes" to save the changes and exit the AptioTM TSE.

6.7.2 Discard Changes and Exit

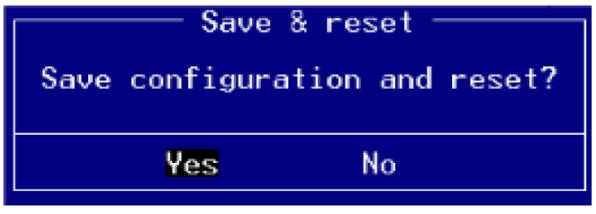
Choose this option to discard changes and exit the AptioTM TSE.
The next window will appear after you choose the "Discard Changes and Reset" option:



Choose "Yes" to discard changes and exit the AptioTM TSE.

6.7.3 Save Changes and Reset

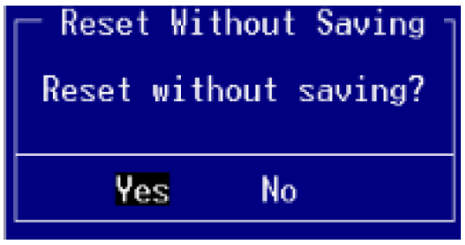
When you made changes in the system, choose this option to save the changes and restart the system in order to subsequently use the new parameter configuration. The next window will appear after you choose the "Save Changes and Reset" option:



Choose "Yes" to save the changes and restart.

6.7.4 Discard Changes and Reset

Choose this option to restart without saving the changes made during configuration process. The next window will appear after you choose "Discard Changes and Reset" option:

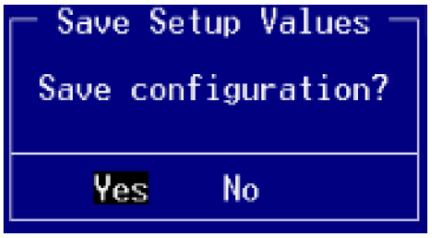


6.7.5 Save Options

Below is a description of options for saving/discarding the changes made.

6.7.5.1 Save Changes

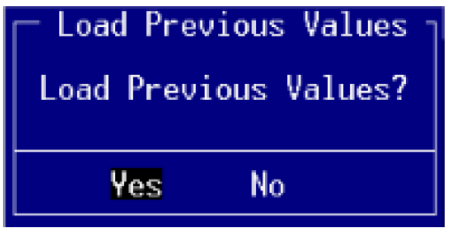
When you have made some changes in the system, choose this option for saving changes when you carry on operations. Some options require system restart in order to allow using the new configuration of parameters.



Choose "Yes" for saving changes when you carry on operation.

6.7.5.2 Discard Changes

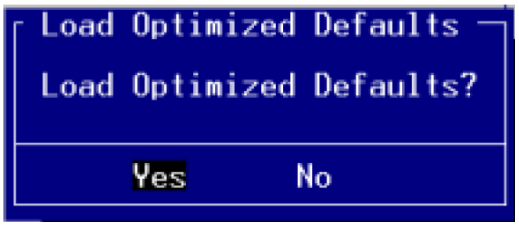
Choose this option to discard the changes made.



Choose "Yes" for booting initial configuration when you carry on operation.

6.7.5.3 Restore Defaults

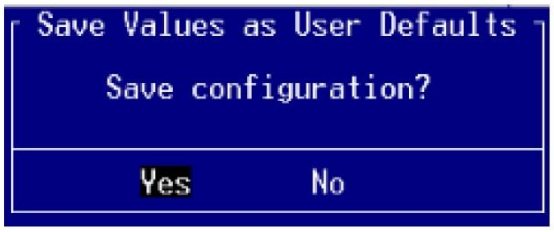
Restoring default configurations for all the options



Choose "Yes" to get back to default configurations.

6.7.5.4 Save as User Defaults

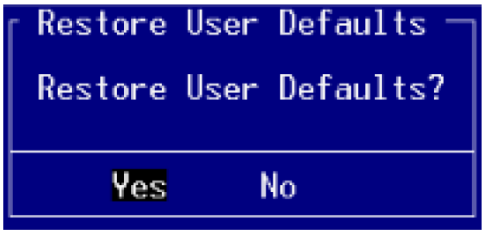
Save changes made as User default settings.



Choose "Yes" for saving changes when you carry on operation.

6.7.5.5 Restore User Defaults

Restoring User defaults for all the options.



Choose "Yes" for restoring User defaults when you carry on operation.

6.7.6 Boot Override

This menu item shows all possible boot options from the "Boot Option List". User can choose a device for booting directly from BIOS SETUP.

7 Additional information

7.1 Temperature mode control

The Intel IvyBridge CPUs operate under severe thermal conditions. This requires special steps to keep the CPU chip temperature within the permitted values. Further paragraphs provide developers of the systems based on CPC512/CPC512RC with information, required for the meeting temperature requirements and specifications.

7.1.1 Temperature passive control

Control structure of the temperature mode of CPC512/CPC512RC can be presented in the form of certain functions, which purpose is to protect processor and reduce its power consumption. Use of thermal control circuits enable CPU to keep a safe operating temperature without any special software drivers and procedures of interrupts processing.

Functions of CPU thermal protection:

1. In case of cooling system failure, the "Catastrophic Shutdown Detector" technology ensures CPU shutdown if processor chip temperature cannot be retained by any passive or active means of temperature control equal to 105°C. This function is always active, in order to ensure CPU protection in any case. After actuation of the "Catastrophic shutdown detector", the CPU module moves to the Soft-Off mode (S5). In order to restart the module it is required to perform the switching on/off power cycle. If in this case the overheating has not been eliminated, the "Catastrophic Shutdown Detector" is actuated again.
2. Enhanced SpeedStep®: when the temperature of the chip core exceeds 100°C, the CPU dynamically switches to the low power consumption mode with the reduced operating voltage of the core and internal multiplication factor.
3. Configurable TDP (Thermal Design Power). TDP parameter, specified in the CPU documentation, describes requirements to the cooling system capacity. Three configurations are available: TDP Nominal - by default, Minimal (TDP Down) and Turbo (TDP Up). At sufficient heat-removal, CPU TDP can be can be increased (TDP Up) and its clock frequency will be increased in the Turbo Boost mode (which is off, by default). To the contrary, if ambient conditions prevent from a complete removal of heat from the CPU, in this case CPU TDP should be reduced (TDP Down).
4. The external temperature monitors (LM87 and LM95235) are designed for gathering information on temperatures: PCI Express of the switch and board surface (LM87), memory chips (LM95235). These data could be used by a control program in order to take reasonable steps.

If CPC512 operates under operating conditions which are considered ordinary for CompactPCI with sufficient air circulation, there will be no need in using the temperature mode control functions. However, when the ambient parameters are not optimal for the module based on Intel IvyBridge, the temperature control mode functions will be activated in order to ensure stable operation. The thermal mode control provides developers with the possibility to create cost-efficient solutions not sacrificing system reliability and integrity.

Warning!

When performing benchmarks and efficiency tests, all the functions for controlling thermal conditions should be switched off. Otherwise, erroneous results could be obtained.

7.1.2 CPC512 cooling system

Specially developed cooling heatsinks ensure the best basis for stable operation and long-term reliability. When they are used together with system enclosure, which ensures adjustable air flow parameters, thermal energy dissipation is guaranteed.

All the versions of CPC512 are equipped with optimally developed cooling heatsinks. Their size, form and design ensure the best values of thermal resistance factors (Rth). In addition, they are designed for active use of the forced ventilation system of the modern CompactPCI Serial systems.

While designing solutions based on CPC512 developer should pay attention to the thermal characteristics of the system, in general. There should be such a system enclosure that will meet the heat removal requirements. During thermal calculations it is necessary to consider contribution which is made by peripheral devices to general system heat-removal.

Peripheral devices, in turn, should have thermal characteristics, corresponding to the operating temperature range of the module and system, in general.

Warning!!!

Due to the fact that Fastwel Group is not responsible for any damages to CPC512 and other equipment, caused by overheating of the system, developers and end users are strongly encouraged to make sure that external environment that surrounds CPC512 meets the specified temperature requirements.

7.1.2.1 Dependence of CPU frequency on temperature

In order to confirm the specified features there were climatic tests of CPC512 CPU modules. Before start of the tests, the crate was equipped with fans that were operating during the entire testing procedure. The tests at positive temperatures were carried out with step changes of temperatures with increment of 10 degrees, starting from +20 degrees. In order to perform the test, there was a package of test programs that loaded computing cores and graphics engine of CPU, floating-point unit as well as RAM and cache memory. Additionally, network controllers and PCI Express switch were loaded. In the filed highlighted with red, 3D functions of the CPU-integrated video controller are switched off, which makes it possible to reduce the released thermal power by 10 W. In this case, the computing core retains its operability at the level of 10-13 W.

Measurements for CPC512-01-i72C1.7-RAM4096-R1-C (IMES.421459.512)

Table 7-1.: Measuring results of CPU module CPC512-01-i72C1.7-RAM4096-R1-C

T of chamber, C	T of core, C	T of printed board	CPU operating frequency, MHz	Throttling, %	Average consumption current, A
20	55	38	1700	-	3.2
30	66	48	1700	-	3.2
40	75	59	1700	-	3.2
50	86	70	1700	-	3.2
60	96	81	1700	-	3.2
70	105	92	800	51	3.2

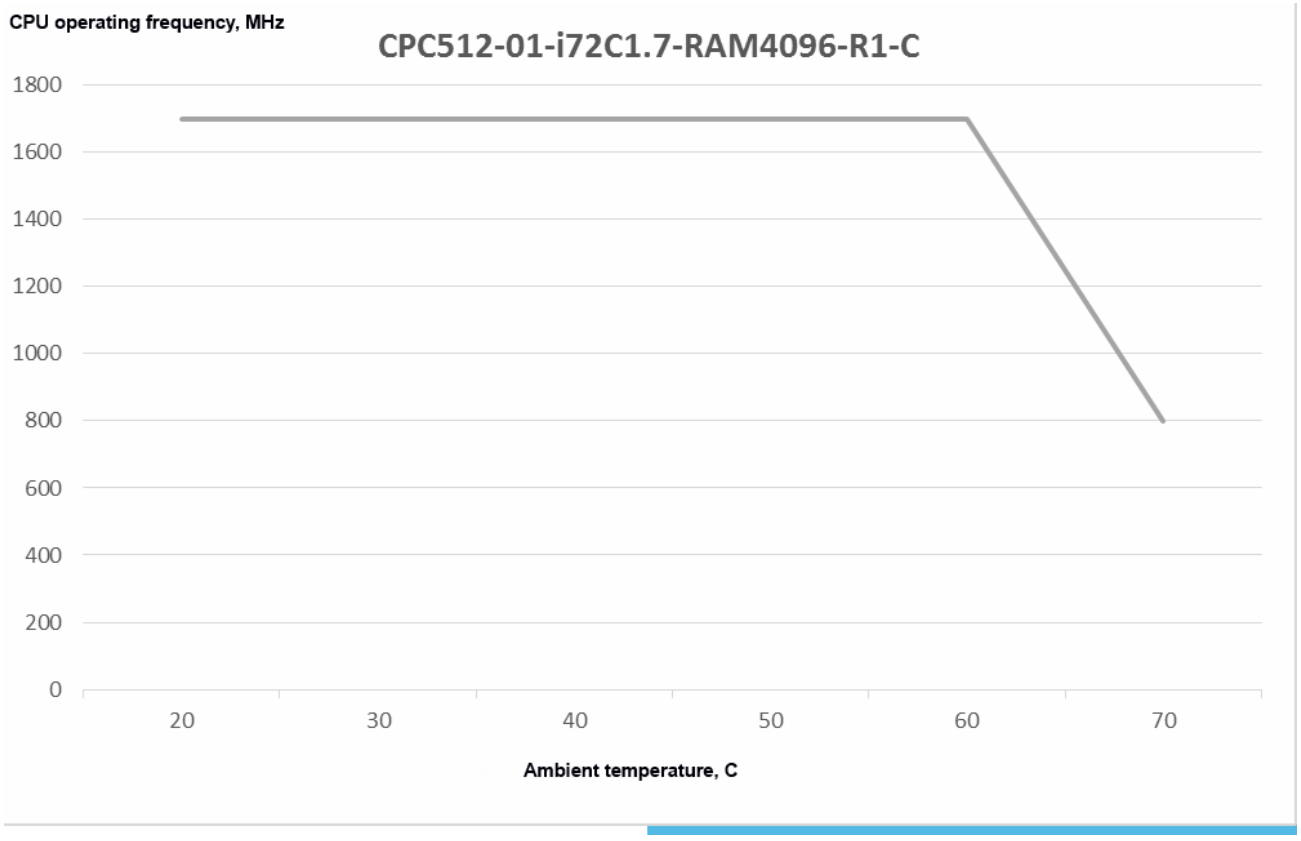


Fig. 7-1: Dependence of CPU frequency on temperature (CPC512-01-i72C1.7-RAM4096-R1-C)

Measurements for CPC512-01-i72C1.7-RAM4096-R2-I (IMES.421459.512-01)

Table 7-2.: Measuring results of CPU module CPC512-01-i72C1.7-RAM4096-R2-I

T of chamber, C	T of core, C	T of printed board	CPU operating frequency, MHz	Throttling, %	Average consumption current, A
20	48	35	1700	-	3.2
30	60	45	1700	-	3.2
40	69	56	1700	-	3.2
50	79	66	1700	-	3.2
60	90	77	1700	-	3.2
70	102	89	1700	-	3.2
85	105	100	800	50	2.3

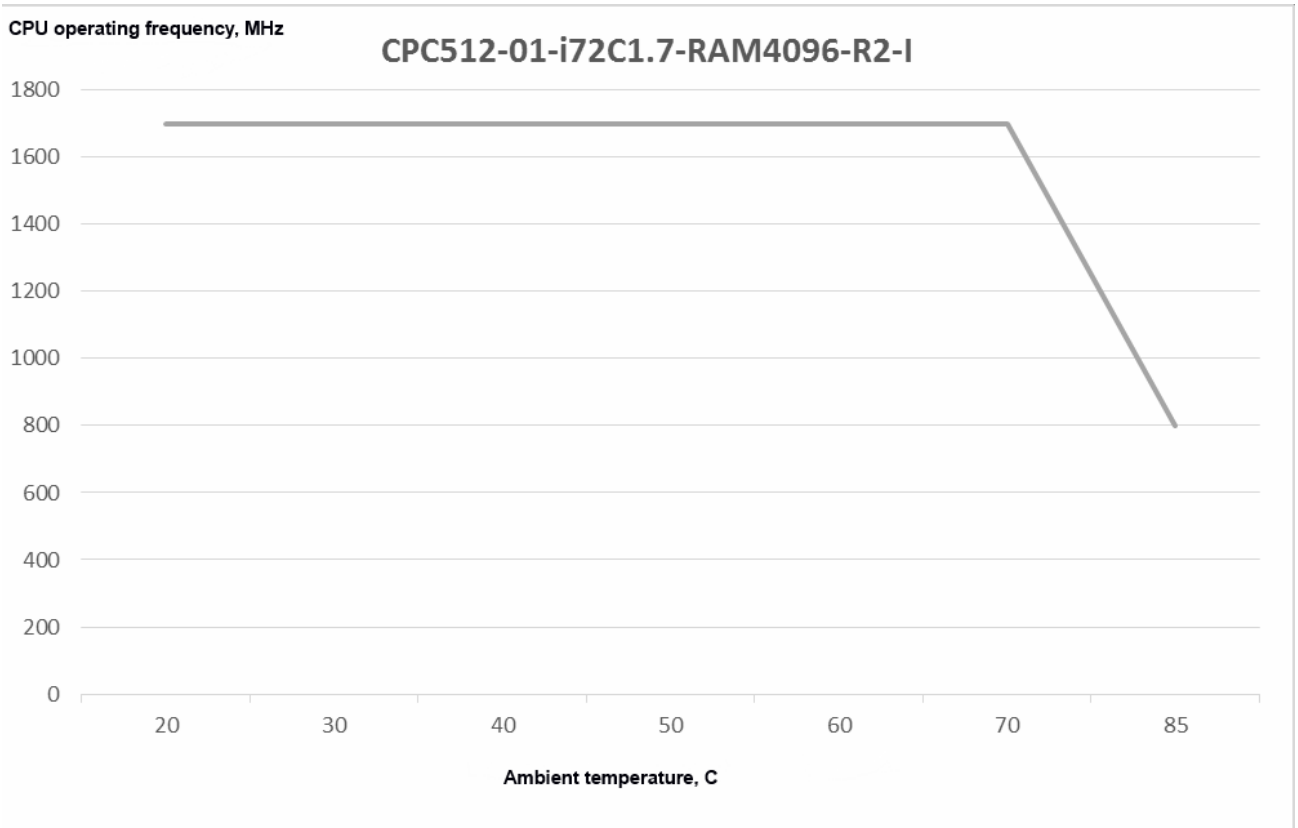


Fig. 7-2: Dependence of CPU frequency on temperature (CPC512-01-i72C1.7-RAM4096-R2-I)

Measurements for CPC512-01-i74C2.1-RAM8192-R2-C (IMES.421459.512-02)

Table 7-3.: Measuring results of CPU module CPC512-01-i74C2.1-RAM8192-R2-C

T of chamber, C	T of core, C	T of printed board	CPU.oper.frequency, MHz	Throttling, %	Average consumption current, A
20	65	39	2090	-	4.5
30	76	50	2090	-	4.5
40	86	61	2090	-	4.7
50	96	74	2090	-	4.8
60	104	84	1890	40	4.8
70	105	90	800	89	3.9

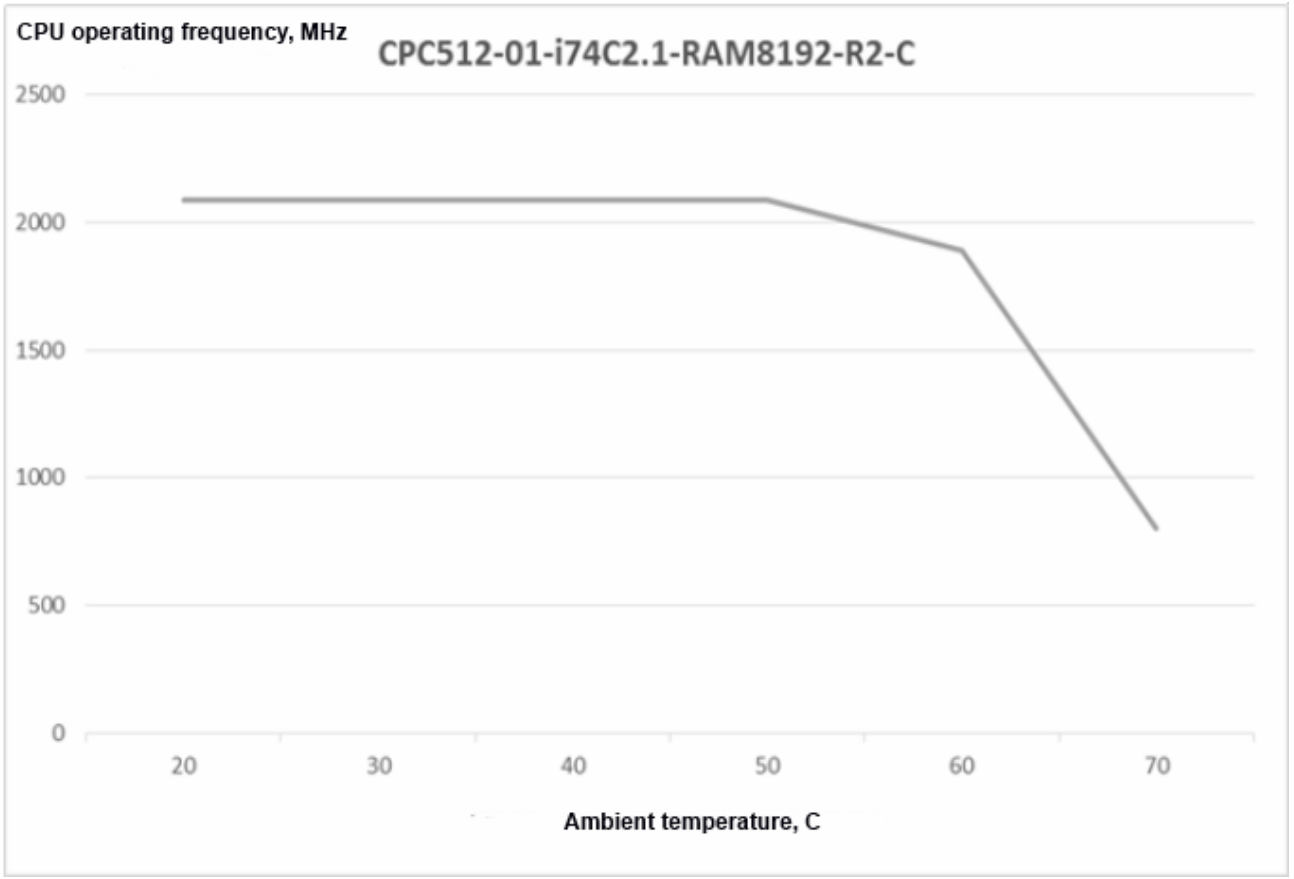


Fig. 7-3: Dependence of CPU frequency on temperature (CPC512-01-i74C2.1-RAM8192-R2-C)

Measurements for CPC512-01-i74C2.1-RAM8192-R1-C (IMES.421459.512-03) with low, all-copper heatsink of an enlarged area.

Table 7-4.: Measuring results of CPU module CPC512-01-i74C2.1-RAM8192-R1-C

T of chamber, C	T of core, C	T of printed board	CPU op. frequency, MHz	Throttling, %	Average consumption current, A
20	73	47	2090	-	4.6
30	82	58	2090	-	4.7
40	91	70	2090	-	4.8
50	100	81	2090	-	4.9
60	105	90	1440	42	4.5
70	104	95	1050	43	3.5

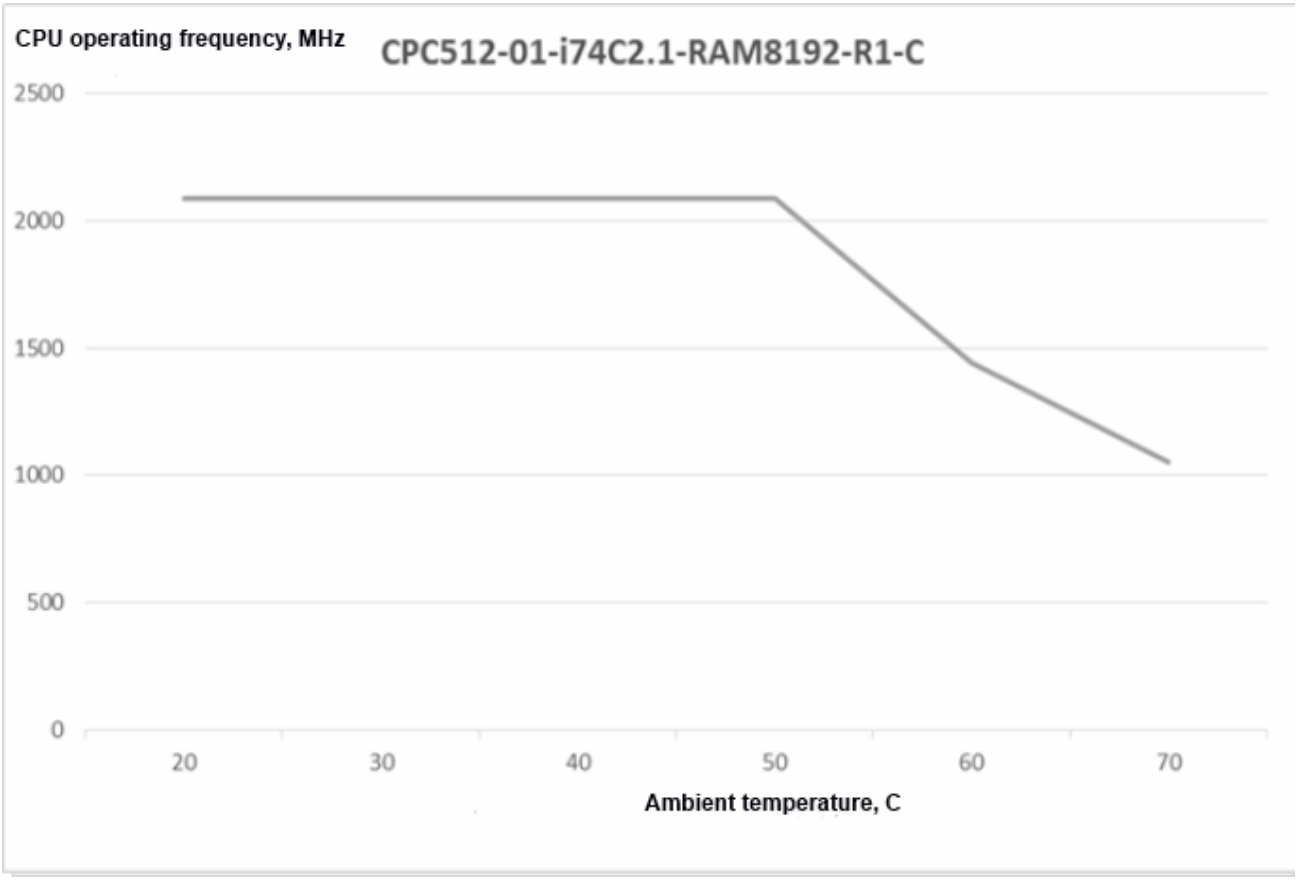


Fig. 7-4: Dependence of CPU frequency on temperature (CPC512-01-i74C2.1-RAM8192-R1-C)

Module cooling recommendations

- Forced cooling is obligatory for all the modules. This is why we highly recommend the users to apply crates with integrated internal space blow-off units for systems based on CPC512 CPU modules.
- Use of Schroff regular crate fans are recommended to be applied within the systems on th basis of CPC512 CPU modules.

7.1.3 Cooling system of CPC512RC module

Unlike CPC512 module, CPC512RC has a different process of heat removal. The basis is contact-type transmission of heat from fuel elements of the module directly to system enclosure. The enclosure, in turn, enables to remove heat either to the environment, using convection method due to the enlarged surface area, or can use a fluid or other type of heat exchange.

Therefore, an overall thermal resistance of the system consisted of the enclosure and module installed into it, is calculated as a sum of all thermal resistances arising during transmission of heat from the sources on the board of CPC512RC to ambient environment around the enclosure (in case of enclosure convection-type cooling). The lower is overall thermal resistance, the better performance can be obtained from the system or in case of the same system performance the upper limit of operating temperature range will be enhanced.

Main contribution to the overall thermal resistance are is implemented by transitions between assembly units of the device.

RΣ= [Rtsource1+Rtsource2+…+RtsourceN] +

Rtcass + Rtencl; where

[Rtsource1+Rtsource2+…+RtsourceN] – sum of thermal resistances between N thermal sources, placed on the board of CPC512RC and heatspreading cassette;

Rtкcass – thermal resistance of the transition "heatspreading cassette - enclosure; Rtencl –

thermal resistance "enclosure - ambient environment";

Other additions due to the structure of enclosure or by other reasons are also possible.

Thermal resistance Rtsource is minimized by design of heatspreading cassette specially developed by manufacturer of CPC512RC, using heat pipes and highly heat-conductive materials.

Thermal resistance Rtcass depends on the area and quality of contact between heatspreading cassette and enclosure, as well as materials used for their production. In order to minimize Rtcass, enclosure design of the system could use high thermal conductivity materials (e.g. copper), as well as increase the closeness of contact by using a thermal grease. The quality of heat removal from heatspreading cassette to the enclosure directly influences on both temperature inside the cassette and temperature of the in-vessel volume.

In order to perform the correct thermal calculation of enclosure parameters, as an upper limit of the operating temperature range of CPC512RC the technical specifications indicate a maximum temperature at the reference point of heatspreading cassette (see Fig. 7-5) instead of the ambient temperature.

Fig. 7-5: Location of temperature monitoring reference point on heatspreading cassette of CPC512RC

The specified temperature corresponds to the fully loaded operation mode of CPC512RC-01 without the loss of capacity (modes of passive adjustment of module's power supply are switched off), CPC512RC-02 at this temperature has a reduction of capacity by a value less than 10%.

Therefore, selection of parameters for enclosure thermal calculation should be carried out in accordance with the requirement to ensure maximum temperature at the reference point of the heatspreading cassette, not higher than the one specified in the technical specifications for this version of CPC512RC (see Table 7-5).

Table 7-5.: Range of operating temperatures of CPC512RC in accordance with IMES.469555.002 TS

CPC512RC CPU Module	CPC512RC	CPC512RC-01	Dual Core CPU 1.7 GHz, 17 W, 4GB RAM, temperature range **- 50 ÷ + 85 °C**
		CPC512RC-02	Quad Core CPU 2.1GHz, 35 W, 8GB RAM, temperature range **- 50 ÷ + 85 °C**

7.2 Power consumption of CPC512/CPC512RC

Power supply voltage +5 V_Standby voltage +12 V.

Consideration should be given to certain requirements, which are essential for ensuring stability and reliability. The table below contains values of the maximum allowable voltages on power lines, which if exceeded, could lead to module damages. Power supply sources, which are to be used with CPC512 or CPC512RC, should be checked in order to meet these requirements.

Table 7-6.: Power consumption parameters of CPC512/ CPC512RC

Voltage (V)	Minimum (V)	Maximum (V)	Consumption current MAX (A)
+5 V_standby	4.75	5.25	2
+12	11.4	12.6	6

If power supply voltage exceeds the specified limits, module functionality is not guaranteed.

The backplane should ensure optimum allocation of power supply voltages. It is recommended to use only those backplanes that have two power planes for each of the voltages.

Connections of power supply lines and the backplane should ensure minimum losses and guarantee stability of performance capabilities. Avoid long feeding lines, light-section conductors and high-resistance connections.

If possible, use power supply sources with voltage control function. This could also require using a relevant backplane.

The power supply source should have enough capacity to consider possible deviations of electronic components characteristics.

Module starting and average consumption currents

During the tests, module's maximum starting and maximum average consumption currents were measured

Table 7-7.: Results of measuring maximum starting and average currents

Module	Maximum starting (short-time) current (+12V) **	Maximum average current (+12 V) *
CPC512-01-i72C1.7	4.2 A	3.5 A
CPC512-01-i74C2.1	4.2 A	4.7 A

** Values derived from the lab test records for consumption currents.*
*** Estimated values of maximum consumption current are given*

7.3 Compliance of CPC512/CPC512RC to safety requirements

CPC512 corresponds to the general safety requirements imposed on IT equipment in accordance with the GOST R IEC 60950-2002 (for equipment, connected to the mains with the

voltage up to 600 V).

7.4 Operation conditions of CPC512

The device retains operability under the following climatic and mechanical effects:

Table 7-8.: Parameters of climatic and mechanical effects (CPC512)

Type of effect	Parameter name	Parameter value	Document
Temperature change	Low temperature	- 40 (0*) °C	GOST 28209 Nb Testing
	High temperature	+ 85 (+70*) °C	
Humidity	Relative humidity	Up to 80% without condensation	GOST 28209
Damp heat (+55) (for coated surfaces) **	Relative humidity	Up to 93%	GOST 28209 Nb Testing
Sinusoidal vibration	Frequency range (Hz)	10...150	GOST 28203
	Acceleration, g	2	
Single shocks	Peak acceleration, g	50	GOST 28213
	Duration, ms	11	
Multiple shocks	Peak acceleration, g	25	GOST 28215
	Duration, ms	6	
	Number of shocks	1000	

** For the version with commercial temperature range*

*** Only for /COATED versions. Only device resistance to damp heat is guaranteed*

Table 7-9.: Electromagnetic compatibility requirements (CPC512)

Type of requirement	Regulatory document
Man-made interferences from Information Technology Equipment. Test standards and methods	GOST R 51318.22-99 Class A (CISPR 22-97)
Resistance of computing and information technology equipment to electromagnetic interference. Test requirements and methods	GOST R 51318.24-99 (CISPR 24-97)

Note

The tested devices correspond to reported requirements to mechanical loads provided that the following conditions are met: additional fastening of USB devices is required (e.g. fastening with the use of mastic compound).

7.5 Operation conditions of CPC512RC

The device retains operability under the following climatic and mechanical effects:

Table 7-10.: Parameters of climatic and mechanical effects (CPC512RC)

Type of effect	Parameter name	Parameter value	Document
Elevated operating temperature	-	See Table 7-10	IMES.469555.002 TS
Elevated limit temperature	-	+90 ^{0}C	IMES.469555.002 TS
Reduced operating temperature	-	- 55 ^{0}C	GOST RV 20.57.306-98
Reduced limit temperature	-	- 65 ^{0}C	GOST RV 20.57.306-98
Temperature change	-	From reduced limit to elevated limit	GOST RV 20.57.306-98
High humidity	-	98% at 35 ^{0}C	
Atmospheric precipitations	-	15 mm/min	
Static dust	-	5 g/m3 at the air speed of 1 m/sec	
Dynamic dust	-	5 g/m3 at the air speed of 15 m/sec	
Sinusoidal vibration	Range of frequencies (Hz)	1-500 Hz	GOST RV 20.57.305-98
	Acceleration, g	6g	
Single shocks	Peak acceleration, g	75g, duration 1-5 ms	GOST RV 20.57.305-98
Multiple shocks	Peak acceleration, g	15g, duration 5-15 ms	GOST RV 20.57.305-98
	Number of shocks	10000	

Table 7-11.: Electromagnetic compatibility requirements (CPC512RC)

Type of requirement	Regulatory document
Man-made interferences from Information Technology Equipment. Test standards and methods	GOST R 51318.22-99 Class A (CISPR 22-97)
Resistance of computing and information technology equipment to electromagnetic interference. Test requirements and methods	GOST R 51318.24-99 (CISPR 24-97)

Note

The tested devices correspond to reported requirements to mechanical loads provided that the following conditions are met: additional fastening of USB devices is required (e.g. fastening with the use of mastic compound).

7.6 Requirements to cooling system of CPC512

The CPU module should be working in the reported temperature ranges with forced ventilation within the construct. The total maximum power, dissipated by CPU and the south bridge is ~50 W. In addition, the heatsink removes heat from PCI Express switch. It is recommended to perform preliminary thermal calculation of the cooling system.

Table 7-12.: Dissipation power and chip limit temperature for module's main microcircuits

Microcircuit	Dissipation power(W)	Chip limit temperature (°C)
IvyBridge CPU	17(25)(45)*	105**
PCI-E Switch	10	125
Gigabit Ethernet Controller	2	110
PantherPoint PCH	4.5	110
DDR3-1600 8GB ECC	12	(Tcase = +85) ***

**Power at maximum frequency and maximum load of CPU is specified*
***Limit temperature of processor chip prior to SpeedStep activation is specified.*
****In case of excess of temperature Tcase +85 degrees, refreshment rate is doubled*

7.7 Requirements to cooling system of CPC512RC

In addition to the heat-dissipation sources specified in p.8.6, the conduction-type cooler for CPC512RC module can efficiently remove heat from all the active components of module elements unit with heat extraction of more than 300 MW. This enables to retain the temperature of the inside cassette volume at the accepted level.

Colling of the "hottest" components of module elements unit of CPC512RC: of CPU and PCI Express switch is carried out via special heat pipes installed inside the heat-spreading cassette.

For proper operation of the heat-spreading cassette, the enclosure structure should ensure such heat dissipation that the temperature in the cassette reference point doesn't exceed the one specified in the Technical Specifications IMES.469555.002 TS (see Table 7-5).

Location of reference point is determined in accordance with Annex C Technical specifications of IMES.469555.002 TS (see Fig. 7-5).

8 Transportation, unpacking and storage

8.1 Transportation

The module should be transported in a separate packaging box (transport packaging) of the manufacturing facility, which consists of an individual antistatic bag and a cardboard box, in the closed transport (automobile, railway, air transportation in heated and pressurized compartments) in storage conditions 5 defined in the GOST standard 15150-69 (IEC 721-2-1 standard) or in storage conditions 3 during sea transportation.

It is possible to transport modules, packaged in individual antistatic packages, in multiple packaging (transport packaging) of the manufacturing facility.

The packaged modules should be transported in accordance with the shipping rules, operating with this particular type of transport.

During handling and transportation operations, the packaged modules should not undergo sharp pounding, falls, shocks and exposure to atmospheric precipitation. The packaged modules should be stored in a carrier vehicle in such a manner which will prevent their moving.

8.2 Unpacking

Prior to unpacking, before transportation at subzero temperature of ambient air the modules should be kept within 6 hours under storage conditions 1 defined in the GOST standard 15150-69 (IEC 721-2-1 standard).

It is prohibited to place the packaged module close to the heat source, prior to unpacking.

While unpacking, it is required to comply with all safety precautions, which ensure its safety, as well as marketable condition of consumer packaging of the manufacturing company.

At the time of unpacking it is required to check the module that it has no external mechanical damages after transportation.

8.3 Storage

Module storage conditions for group 1 are defined in the GOST standard 15150-69 (IEC 721-2-1 standard).

Annex A

Useful abbreviations, acronyms and shortcuts

Term	Value
ACPI	Advanced Configuration and Power Interface -
AGP	Accelerated Graphics Port -
AGTL	Advanced Gunning Transceiver Logic -
BIOS	Basic Input-Output System -
BMC	Baseboard Management Controller -
CRT-display	Cathode Ray Tube Display - -
DAC	Digital-Analog Converter -
DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory -
DMA	Direct Memory Access -
DMI	Direct Media Interface -
DVMT	Dynamic Video Memory Technology -
ECC	Error Correction Code -
EEPROM	Electrically Erasable Programmable Read-Only Memory -
EHCI	Enhanced Host Controller Interface (Universal Serial Bus specification)

Term	Value
EIDE	Enhanced Integrated Drive Electronics -
EOS	Electrical Overstress -
ESD	Electrostatically Sensitive Device . Electrostatic Discharge
FSB	Frequency System Bus -
FWH	Firmware Hub - -
GMCH	Graphics and Memory Controller Hub -
I^2C™	Inter Intergrated Circuit -
LCD	Liquid crystal display -
LPC	Low Pin Count -
LVDS	Low Voltage Differential Signal - -
MDI	Media Dependent Interface -
PC	Personal Computer -
PIO	Programmed Input/Output -
PLCC	Plastic Leaded Chip Carrier -
PM	Peripheral Management Controller -
POST	Power On Self Test -
PSB	Processor System Bus -

Term	Value
PWM output	Pulse-Width Modulation - -
RAMDAC	Random Access Memory Digital-to-Analog Converter -
RTC	Real Time Clock -
SMB	System Management Bus -
SMBus	System Management Bus -
SODIMM	Small Outline Dual In-Line Memory Module
SoM	System on a module -
SSD	Solid State Disk -
TFT	Thin Film Transistor -
TTL	Transistor-Transistor Logic -
UART	Universal Asynchronous Receiver-Transmitter
UHCI	Universal Host Controller Interface -
USB	Universal Serial Bus -
UTP	Unshielded Twisted Pair

ANNEX B DISCLAIMER

This Disclaimer contains special operating conditions of Fastwel in the following areas: intellectual property, warranty policy, conditions of the order and delivery.

1 INTELLECTUAL PRORETY

1.1 If any infraction, interference, improper use, illegitimate exploitation and/or violation of the industrial and/or intellectual property rights of any third party and/or property, exploitation during the use of Fastwel Embedded Module will take place – Fastwel does not guarantee to replace the materials, computer programs, procedures or equipment affected by the complaint and under no circumstances doesn't bear responsibility in any form for possible refusal in case of such a replacement.
1.2 Use of the Fastwel products as well as the objects of intellectual property containing in them, in the ways and for the purposes, not provided by the present user manual and datasheet isn't allowed without preliminary written approval of Fastwel.
1.3 Fastwel is not responsible for possible incidents and losses, related to the operation of end devices, in which the original Fastwel equipment is used.

2 WARRANTY POLICY

2.1 When the detected flaws in an element can be corrected without decreasing the foreseen technical features and functionality for it, User may demand Fastwel the urgent correction of the failures in additionally agreed period and an increasing of the period of the guarantee of the element equal as the time elapsed from the formal request to repair the failures, until the receipt of the repaired element. All costs associated to the correction of failures, included those of assembly, dismantle, transport, tests, etc, if they exist, shall be prosecuted according the Warranty Policy of Fastwel.

3 ORDER AND DELIVERY CONDITIONS

3.1 The general rule is that all Fastwel equipment prices are determined with due consideration of delivery under the EXW terms and conditions (Incoterms 2010). Delivery of the products under other terms and conditions should be preliminary agreed and stated in writing between the parties.
3.2 Unless otherwise expressly agreed with Fastwel, all the deliveries of Fastwel equipment will be carried out only after the official purchase order is obtained and provided that the ordered products have been prepaid in full. Other terms and conditions of cooperation should be made in writing.
3.3 Any delivery of Fastwel electronics is submitted with the right package in accordance with the current rules and standards in the Member States of the European Economic Area. The purchaser independently bears all risks regarding the compliance of package and marking of Fastwel products with legislation requirements being in effect at the place of purchased products destination (in the buyer's country). The specified condition excludes unequivocally any liability of Fastwel for possible non-compliance of package and marking of products with the requirements of legislation of the country of products destination.
3.4 In general, all components of the supply are properly protected with respect to freight, in order to avoid any damage to the supply, third parties, environmental damages or unrelated goods, as consequence of wrong packaging.
3.5 Each package unit is labeled on the exterior area with the indications of product's Part Number and Serial Number.
3.6 The support documents for the order should be made either in English or in Russian unless otherwise agreed between parties in writing.
3.7 Fastwel does not pay penalties and does not cover costs associated with delay in the delivery of the products caused by actions of the third parties, force-majeure etc. - Fastwel doesn't bear any responsibility for non-execution or inadequate execution of the obligations in a case when it is caused by actions of the third parties (for example producers or suppliers of accessories), force majeure etc.
3.8 Fastwel declares that independently and at any time without damage, it has an exclusive right to define and change functionality architecture, bill of materials of its products without any preliminary coordination and approvals of the third parties.

4 OTHER CONDITIONS

4.1 Fastwel has the obligation to respect the current Russian legislation (including, but not limited to environmental, labor, social laws) in each moment and to apply it to its embedded electronics considering all and each execution phase, that is to say, from the design until the commissioning and subsequent maintenance. In this regard Fastwel is not liable to the user or other persons in connection with possible changes of the company's rules (including, but not limited to warranty, ordering policy) caused by changes of the Russian legislation.
4.2 Unless otherwise expressly agreed in writing, Fastwel provides no training for assembly\installation\adjustment\operation of its equipment.